December 13, 2010

RT0926
Engineering Technology pages

Research Report

Development of Vacuum Underfill Technology for 3-D Chip Stack

Katsuyuki Sakuma, Sayuri Kohara, Kuniaki Sueoka, Yasumitsu Orii, Mikio Kawakami, Kazuo Asai, Yoshikazu Hirayama, and John U. Knickerbocker

IBM Research - Tokyo
IBM Japan, Ltd.
1623-14 Shimotsuruma, Yamato
Kanagawa 242-8502, Japan

Research Division
Almaden - Austin - Beijing - Haifa - India - T. J. Watson - Tokyo - Zurich

Limited Distribution Notice
This report has been submitted for publication outside of IBM and will be probably copyrighted if accepted. It has been issued as a Research Report for early dissemination of its contents. In view of the expected transfer of copyright to an outside publisher, its distribution outside IBM prior to publication should be limited to peer communications and specific requests. After outside publication, requests should be filled only by reprints or copies

of the article legally obtained (for example, by payment of royalities).

Development of Vacuum Underfill Technology for 3-D Chip Stack

Katsuyuki Sakuma[1*], Sayuri Kohara[1], Kuniaki Sueoka[1], Yasumitsu Orii[1], Mikio Kawakami[2], Kazuo Asai[2], Yoshikazu Hirayama[2] , John U. Knickerbocker[3]

[1]IBM Research – Tokyo, Yamato, Kanagawa, 242-8502, Japan
[2]Toray engineering, Otsu, Shiga, 520-2141, Japan
[3]IBM T.J. Watson Research Center, Yorktown Heights, New York, 10598, USA

Email: sakuma2@jp.ibm.com

Abstract

We developed a vacuum underfill technology for 3-D chip stacks and for flip chips in high performance system integration. We fabricated a 3D prototype chip stack using the vacuum underfill technology to apply the adhesive. The underfill was injected into each 6-µm gaps in a 3-layer chip stack and no voids were detected in acoustic microscopy images. Electrical tests and thermal reliability tests were used to measure the resistance of the vertical interconnections and the impact of the underfill. The results showed there was minimal difference in the average interconnection resistance of the chip stack with and without underfill.

1. Introduction

Three-dimensional (3D) integration is a promising technology for high performance and high circuit density applications, since it reduces global interconnection lengths and increases device density by using high density vertical connections without further shrinking dimensions for transistors and other components [1,2,3]. Fig. 1 shows a schematic cross-section of a 3D chip stack. The processes needed for 3D integration include the formation of through-silicon-vias (TSVs) [4,5] and micro-bumps, wafer thinning, backside processing, bonding [6], and underfill encapsulation that enhances the stacked chip's bonds and prevents contamination. The underfill encapsulation in 3D integration is a challenge due to it's thin gaps less than 10 µm and fine pitch interconnections.

Conventional underfill encapsulation using a flow via capillary action has limitations, especially as the chips become larger in size and as the standoff gaps is reduced.

Two alternate assembly approaches are no-flow underfill [7] and wafer-level underfill [8,9]. No-flow underfill provides flux to the solder during bonding and eliminates the extra processing steps such as flux residue cleaning required for a capillary process. This is rapid process suitable for mass production, but one of the challenges is to avoidable inclusions of filler particles in the solder joints, which can affects the reliability of these connections. The wafer-level underfill approach has the potential of being a fast and low cost operation since the underfill is precoated on the wafer before it is diced into chips for the joining processes [8,9]. This technology approach must overcome challenges such as trapped air bubbles, poor wetting to the solder bumps, or poor alignment because the underfill material may cover up the alignment marks.

Vacuum underfill can be considered as an extension of capillary underfill process where the filled adhesive flow is enhanced using gas pressure. In this approach, an underfill is dispensed around the 3D stacked chip or flip chip under reduced pressure in a vacuum chamber. When the vacuum is released, the pressure within the chips is now lower than the external atmospheric pressure. The pressure difference assists the insulating underfill material in penetrating into the narrow gaps between the stacked chips. To date there have been few experimental studies on the application of underfill with vacuum assistance for 3D chip stacks. T. Matsumoto et al. proposed an adhesive injection method for 3D LSI [10]. However, their process requires a wall around the target area to create a pressure difference and the wall must be designed as part of the layout design. The vacuum underfill technology does not need any wall, which makes this process more suitable for manufacturing.

This paper describes and discusses the results for vacuum underfill technology in 3D integration. No voids were found in flip chips or 3-layer chip stacks when using the vacuum underfill technology.

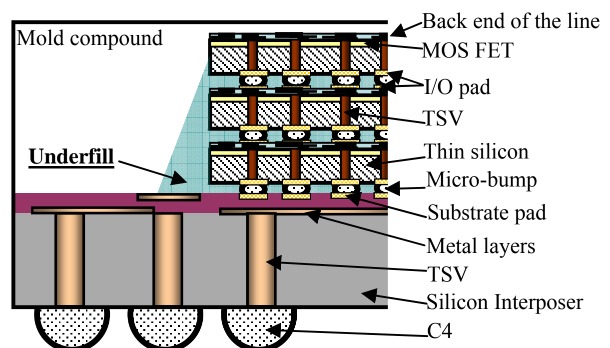


Fig. 1. Schematic cross-section of three-dimensional chip stacking.

2. Experimental Methods of Vacuum Underfill Technology

Fig. 2 shows a comparison of standard capillary underfill deposition with the vacuum underfill process for 3D chip stacks. Table 1 summarizes the vacuum underfill dispensing conditions. For the vacuum underfill process, the stacked chips were placed in the vacuum chamber before dispensing the underfill material. The stage temperature of the vacuum underfill tool was controlled and set to 90°C. This temperature depends on the properties of the underfill material. The vacuum chamber includes a dispensing device for the underfill material. After placing the sample on the stage in the vacuum chamber, the chamber is evacuated. Then the underfill material is dispensed around each stacked chip on the substrate, and the vacuum is released. When the vacuum is filled with air at normal atmospheric pressure, the underfill, which is dispensed all around each stacked chip, is injected by air pressure into the narrow gaps between each chip.

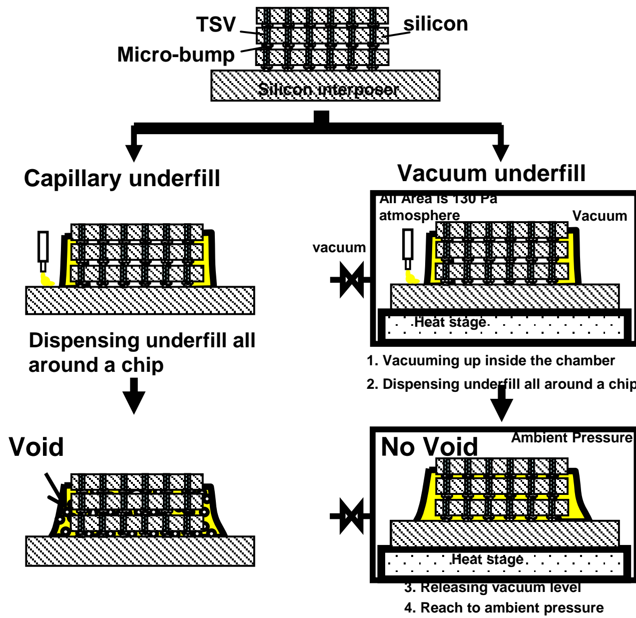
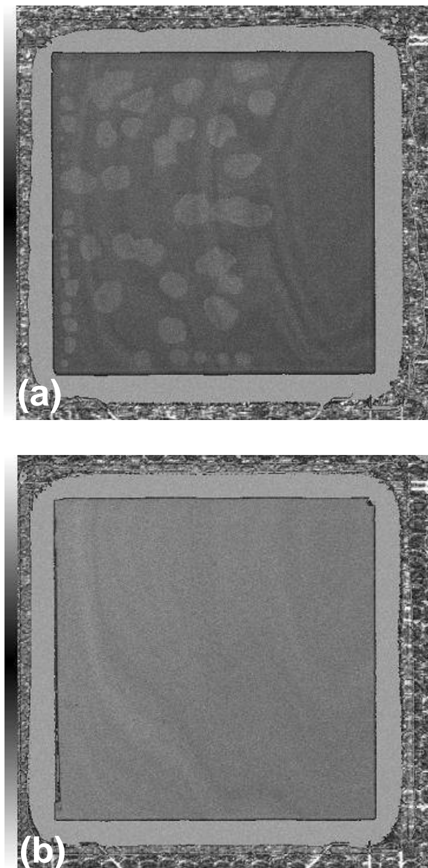


Fig. 2. Comparison of standard capillary underfill deposition with vacuum underfill process for 3D chip stack.

Table I. Vacuum underfill dispensing condition and underfill property.

Dispensing condition	Stage temp [°C]	90 - 100
	Drawing pattern	Square
Underfill property	Filler content [wt%]	55
	Filler size (ave. / max.) [μm]	0.3 / 1
	Viscosity [Pa.s]	60

First, we evaluated the vacuum underfill technology by using a flip chip sample. We used a scanning acoustic microscope (SAM) to search for voids between the chip and the substrate after the vacuum underfill process. Fig. 3 shows acoustic microscope images of samples with underfilling done with the conventional capillary fill method and with the vacuum underfill method. The chip size is 9.6 mm × 9.6 mm. In the chip, there is a peripheral Au bump patterns. The diameter of each Au bump is 60 μm and the pitch is 150 μm. From Fig. 3(a), it can be seen with small voids left by the conventional capillary fill method. Fig. 3(b) is the SAM image when the underfill material was added by using the vacuum underfill technology. There are no voids made visible in the underfill of this chip. The 14-μm gap is completely filled with the underfill (Fig. 3(c)). These results show that the vacuum underfill process is an effective method for a large chip and small gaps.



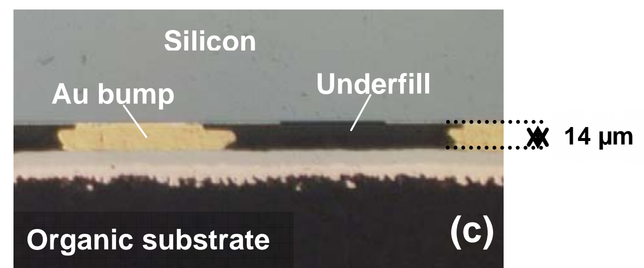


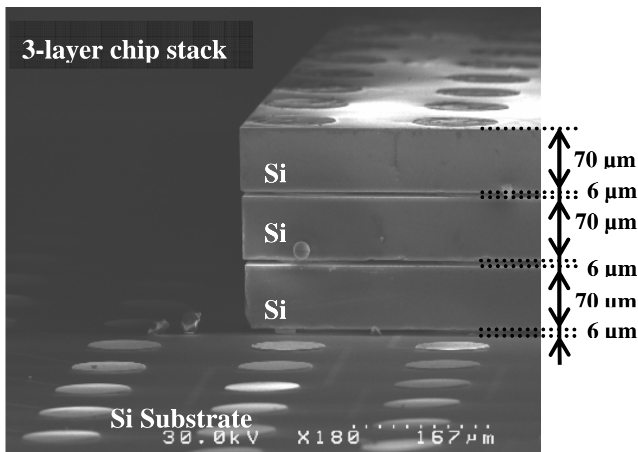
Fig. 3. Acoustic microscope images (a) using standard capillary flow, (b) using vacuum underfill technology, and (c) cross-section SEM of the micro-bump of the flip chip.

We also evaluated this technology for 3D chip stacks. A primary electrical test vehicle for the 3D chip stack was designed. The test vehicle consisted of wired daisy chains. An annular tungsten via structure was used, since this is easily integrated into a standard CMOS back-end-of-the-line (BEOL) process flow and has been shown to give high yield and low resistance [2,4].

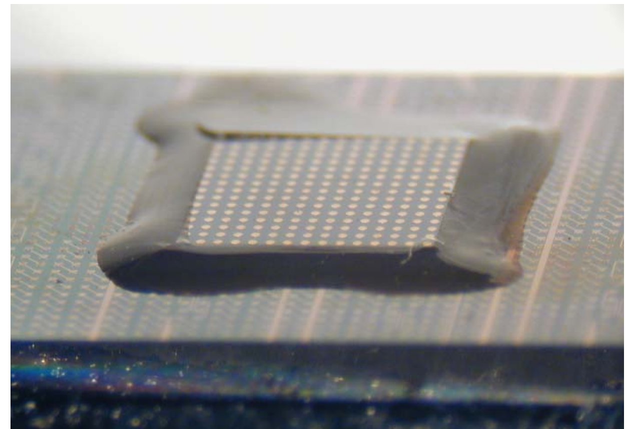
The three-layers were vertically stacked by using a low-cost, high throughput cavity alignment method, which also supports high precision automatic positioning [11]. With this technique, all of the chips are stacked in one step. Each layer is electrically connected by tungsten TSVs and Cu/Sn micro-bumps. The thickness of each stacked chip is approximately 70 μm, and the micro-bumps are 100 μm in diameter with a pitch of 200 μm and a height of 6 μm. The bonding was done with a controlled bonding temperature, time, pressure, and ambient by using the cavity alignment method. Fig. 4(a) shows a SEM image of a 3-layer chip stack on a silicon substrate. Fig. 4(b) shows an optical microscope image of the chip stack with underfill. We used an underfill that includes filler particles. The underfill should completely fill the gaps between each stacked thin chip and its substrate. The objectives for this underfill study included good adhesion, no voids, and the formation of fillets around the stacked chips. As shown in the picture, this process forms a well-shaped fillet around the chip stack. Fig. 4(c) shows a X-ray image of the 3-layer chip stack with underfill. This figure shows that the stacked chips appear to be in good alignment and the TSVs and micro-bumps are connected vertically. Fig. 4(d) shows a SAM image of the 3-layer chip stack with underfill after 1,000 deep thermal cycles(DTCs). This indicates there are no delaminations or large voids in the underfill of the chip stack.

3. Reliability Results

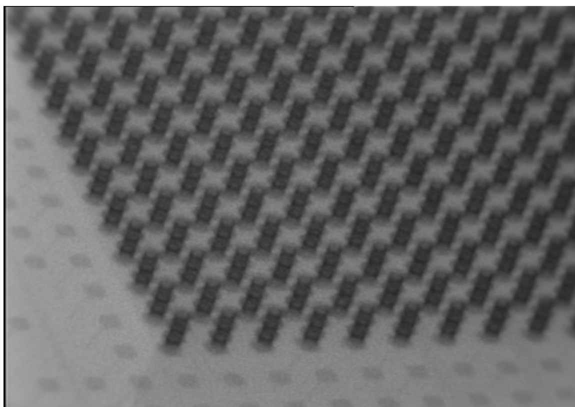
Electrical tests were done to measure the resistance and yield of each vertical interconnection of the 3-layer chip stacks with underfill. The results showed the average resistance of a single TSV and micro-bump was around 75 mΩ and no failures occurred in any of the chains. To study in more detail the thermal stresses generated in the micro-bumps with and without underfill, finite element modeling (FEM) was used to model a 1-layer TSV stack on a silicon substrate. The simulation was done by two steps: 1/4 model of the stacked chip and the submodel of the critical bump (Fig. 5). The relative maximum von Mises stress on the micro-bumps for the DTC condition for a chip stack with underfill is only 8% lower than that without underfill (Fig. 6). To investigate the thermal reliability of the stacked chip, 1-layer TSV stacks



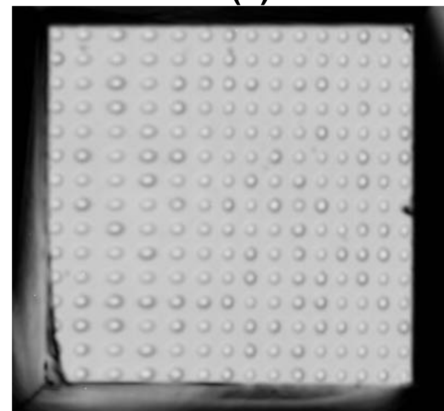
(a)



(b)



(c)



(d)

Fig. 4. A 3D chip-stack sample before and after vacuum underfill process: (a) 3-layer chip stack without underfill, (b) with underfill. Fillet formed around the chip stack, (c) x-ray image after vacuum underfill process. (d) SAM image after vacuum underfill process.

on silicon substrates with and without underfill were subjected to the following reliability test conditions:

1. JEDEC level-3 moisture preconditioning

1-1: 125°C bake for 24hours, 1-2: 30°C at 60% Relative Humidity for 192 hours, 1-3: Three times at 260°C peak reflow.

2. Deep Thermal Cycle: from -55°C to 125°C at a rate of two cycles per hour.

Fig. 7 is a summary of the thermal reliability results up to 1,500 cycles for the stacked chips. There was minimal change in the average resistances between the chip stacks with and without underfill. The simulation results were consistent with the thermal reliability results and this suggests the 3D chip stacks with and without underfill pass the thermal reliability tests for both structure and materials in the TSVs and micro-bumps.

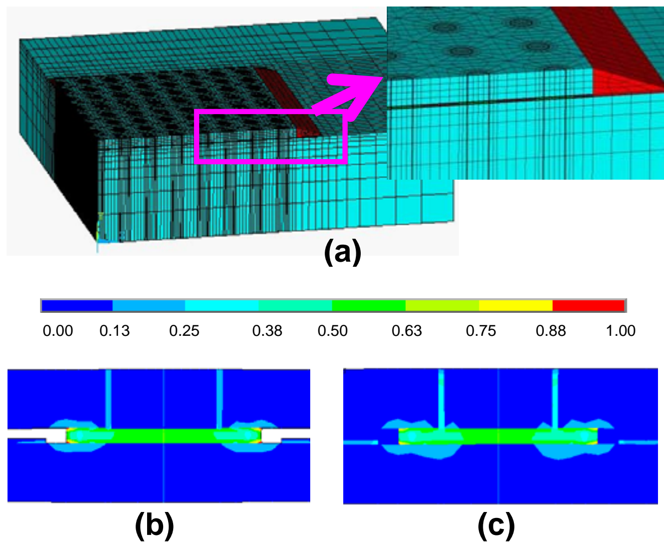


Fig. 5. FEM simulation results: (a) 1/4 model, (b) von Mises stress without underfill, (c) von Mises stress with underfill.

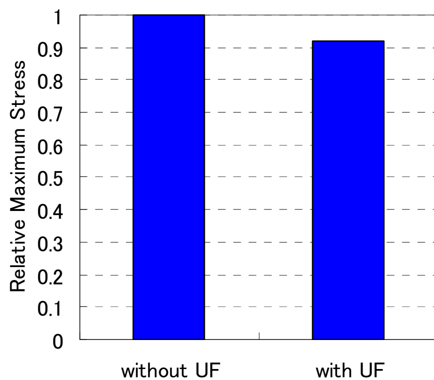


Fig. 6. Relative maximum von Mises stress on the Cu/Sn micro-bump joint for the DTC condition.

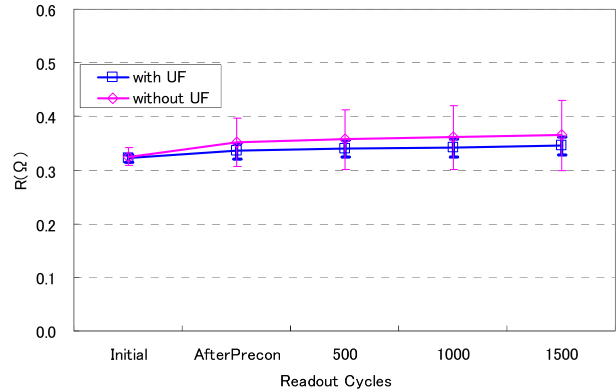


Fig. 7. DTC results for the chip stack with and without underfill. 4pt resistance of the paired TSVs and micro-bumps (including the wiring in 1-layer chip stack).

4. Conclusion

In conclusion, we demonstrated a new 3D integration technology using a vacuum underfill method. We confirmed that the underfill was uniformly injected into the 6 µm gaps between 3-layer stacks of 70-µm chips and no voids were observed in any of the gaps. The thermal reliability test results showed that the resistances of the chip stack interconnections with tungsten TSVs and Cu/Sn micro-bumps with and without underfill were acceptable. Future work on vacuum underfill technology for advanced packaging will include development of new underfill materials suitable for larger chips and narrower gaps than we have studied to date..

Acknowledgements

The authors would like to sincere thank to T. Aoki of IBM Japan and P.S. Andry, C.K. Tsang, B. Dang, and J. Maria and T.C. Chen of IBM T.J. Watson Research Center.

References

1. J. Knickerbocker, P. Andry, K. Sakuma, et al.: in *Integrated Interconnect Technologies for 3D Nanoelectronic Systems*, (Artech House Inc., 2008) Chap. 14. pp.421.
2. K. Sakuma, P. S. Andry, B. Dang, J. U. Knickerbocker, et al. “3D chip-stacking technology with through-silicon vias and low volume lead-free interconnections,” *IBM J. Res. & Dev.* 52. No. 6, pp. 611-622 (2008).
3. M. Koyanagi, H. Kurino, K. Sakuma, K. W. Lee, N. Miyakawa, and H. Itani, “Future System-on-Silicon LSI chips,” *IEEE MICRO*, **18** (1998) 17.
4. P.S. Andry, C.K. Tsang, J.U. Knickerbocker et al. “A CMOS-compatible Process for Fabricating Electrical Through-vias in Silicon,” *Proceedings of the 56th Electronic Components and Technology Conference*, San Diego, CA, 2006, pp. 831-837.
5. K. Sakuma, N. Nagai, M. Saito, J. Mizuno, and S. Shoji, "Simplified 20-um pitch vertical interconnection process for 3D chip stacking" , *IEEJ Transactions on Electrial and Electronic Engineering*, vol. 4 issue 3, pp.339-344, 2009

6. K. Sakuma, J. Mizuno, N. Nagai, N. Unami, and S. Shoji, "Effects of Vacuum Ultraviolet Surface Treatment on the Bonding Interconnections for Flip Chip and 3-D Integration," *IEEE Transactions on Electronics Packaging Manufacturing*, Vol. 33, No.3, July 2010.
7. R. Agarwal, W. Zhang, P. Limaye, W. Ruythooren, "High Density Cu-Sn TLP Bonding for 3D Integration", *Proceedings of the 59th Electronic Components and Technology Conference*, 2009, pp.345-349.
8. C. Feger, N. LaBianca, M. Gaynes, et al., *Proceedings of the 59th Electronic Components and Technology Conference*, 2009, pp.1502-1505.
9. L. Nguyen, H. Nguyen, A. Negasi, Q. Tong, S.H. Hong, "Wafer level underfill – processing and reliability," proc. *SEMI/IEEE IEMT*, 2002, pp.53-62.
10. T. Matsumoto, M. Satoh, K. Sakuma, H. Kurino, N. Miyakawa, H. Itani, and M. Koyanagi, "New Three-Dimensional Wafer Bonding Technology Using the Adhesive. Injection Method", *Jpn. J. Appl. Phys*. **37** (1998) 1217.
11. K. Sakuma, P.S. Andry, C.K. Tsang, et al. "Die-to-Wafer 3D Integration Technology for High Yield and Throughput," *Materials Research Society (MRS)*, Vol. 1112-E04-03, Boston, December, 2008, pp. 201-210