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Abstract

The measured temperature and supply voltage dependences of a bandgap reference circuit first published by Gilbert [1] and implemented in IBM's SiGe BiCMOS process agree well with model predictions. The plot of V_{BGR} vs. temperature exhibits less curvature than predicted elsewhere for SiGe BGR's [2].

Introduction

A voltage reference is an essential building block in many types of analog circuits, such as A/D and D/A converters, smart sensors, etc. Applications such as portable wireless data communications require such circuits to operate with a low supply voltage and low power dissipation. In addition, the high-speed portion of such applications requires a high-performance technology such as SiGe. A simple, low-voltage reference implemented on the same SiGe IC with the high-speed section is thus an attractive building block. To demonstrate the feasibility of such a circuit in SiGe, a simple bandgap reference (BGR) previously published by Gilbert [1] was implemented and the results found to agree well with model predictions.

SiGe HBT BiCMOS Process Technology

The BGR was implemented in IBM's 200-mm SiGe BiCMOS technology without any process modification. This three-level-metal technology features a Si/SiGe HBT with an emitter width of 0.5µm and a cutoff frequency (f_T) and maximum oscillation frequency (f_{MAX}) in excess of 45 GHz and 60 GHz, respectively, NMOS and PMOS devices with a nominal L_{eff} of 0.35µm, polysilicon and diffused resistors, high-density MOS and high-Q metal-insulator-metal (MIM) capacitors, varactor diodes and inductors [3].

Bandgap Reference Design

A schematic of the BGR is shown in Fig. 1. In a BGR, the near-zero temperature coefficient of the reference voltage is achieved by summing the negative temperature coefficient of the base-emitter voltage (V_{BE}) of a bipolar transistor and the positive temperature coefficient of the difference between the V_{BE}'s (ΔV_{BE}) of two bipolar transistors having different emitter areas. In Fig. 1, this reference voltage output is the sum of the V_{BE} of Q_2 and the ΔV_{BE} across the resistors R_3 and R_4. The emitter areas of transistors Q_2 and Q_1 are in the ratio of 52:1, implemented by placing 53 devices, each with an 0.5µm x 2.5µm emitter, in a single rectangular layout block and wiring 52 of these devices in parallel. This layout technique of wiring identical minimum-emitter-width devices in parallel to achieve a larger emitter area for Q_2, rather than placing a single Q_2 device with a longer emitter width or length than Q_1 [2], provides improved matching of the characteristics of Q_1 and Q_2 and also improved agreement with the model predictions, since the minimum-emitter-width device is typically used most often in high-speed designs and is thus the focus of modeling efforts, more so than the other emitter widths available in the technology. The technology features a polysilicon resistor with a near-zero temperature coefficient of resistance [4]; this resistor is used for all four resistors in the circuit (although circuit simulations with a higher TCR resistor give nearly identical results). A 20-pF MOS capacitor on the output serves to filter out high-frequency noise.

Unlike a classical BGR such as the circuit by Brokaw [5], the circuit implemented here uses no opamp or active loads to force the collector currents of transistors Q_1 and Q_2 equal (i.e. $I_1 = I_2$, in Fig. 1). This design choice avoids possible spurious oscillation of the BGR due to a low-bandwidth opamp or PNP/PMOS active load in the same feedback loop with high-bandwidth HBT's, eliminates the power dissipation and chip area of an opamp and eliminates the need for a startup circuit. One disadvantage of such a scheme is the reduction of the power supply rejection ratio (PSRR) of the BGR, which would be increased by the opamp or active load feedback loops. Also, since I_1 and I_2 are not forced equal, the equation for I_1 and I_2 (Eq. 1) remains transcendental in these two variables, thus complicating the analysis of the circuit.

$$\frac{kT}{q}\ln M\left(\frac{I_1}{I_2}\right) = I_1 R_2 + I_2 R_3 \qquad (M=52) \qquad (1)$$

To study these design tradeoffs further, a version of this BGR using PMOS loads and a startup circuit has been designed and is presently in fabrication.

Measurements and Discussion

The untrimmed BGR output voltage (V_{BGR}) was measured on-wafer as the temperature was varied from -50°C to 150°C and the positive supply V_{CC} was varied from 2V to 4V with the negative supply at 0V. Fig. 2 shows V_{BGR} over temperature at V_{CC} =2.5V and 4.0V; the curvature of V_{BGR} vs. temperature, typical of BGR circuits, is clearly evident at 2.5V. The temperature drift at 2.5V is ±25.1ppm/°C from 0 to 75°C and ±36.5ppm/°C from -50 to 150°C. At V_{CC} = 2.5V and 25°C, the supply current of 0.675mA gives a power dissipation of 1.7mW; the supply current has a temperature coefficient of 1.6μA/°C. The power supply rejection ratio (PSRR) at 0 Hz is 26 to 20 dB from -50 to 150°C. The PSRR is expected to improve to 60-70dB in the PMOS-load version of the BGR, currently in fabrication as noted earlier.

The proprietary HSpice models for the SiGe BiCMOS technology provide excellent agreement with these measured results over the entire temperature range from -50 to 150°C. Fig. 3 shows the difference between the simulated and measured values of the bandgap reference output, expressed as an error percentage of the V_{BGR}, over temperature at V_{CC} = 2.5V and 4.0V. An error of less than 1% is observed, using a value of 2.2 for the Spice bipolar transistor model parameter XTI, which controls the deviation from linearity of the transistor's V_{BE} vs. temperature characteristic.

Table 1 summarizes the performance of the BGR at V_{CC} = 2.5V.

References

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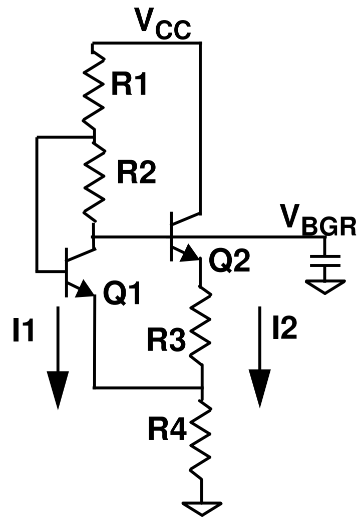

Fig. 1. Schematic of the bandgap reference circuit.

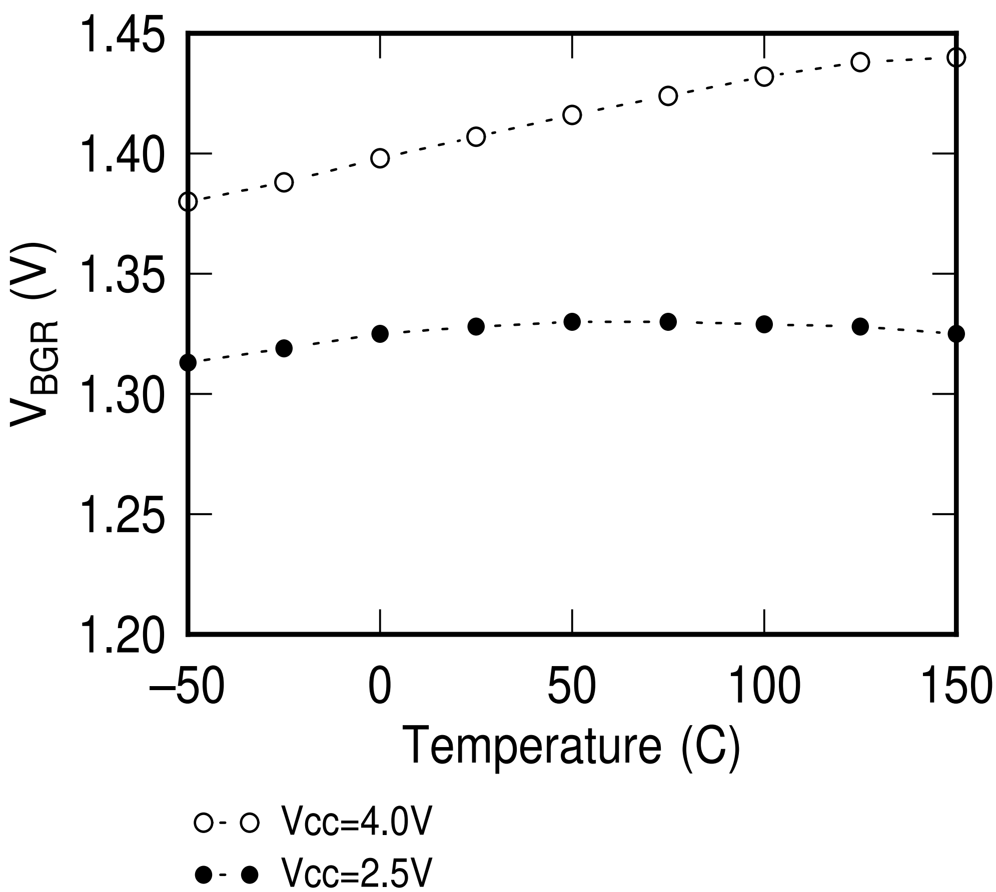

Fig. 2. Measured BGR voltage over temperature and V_{CC}.

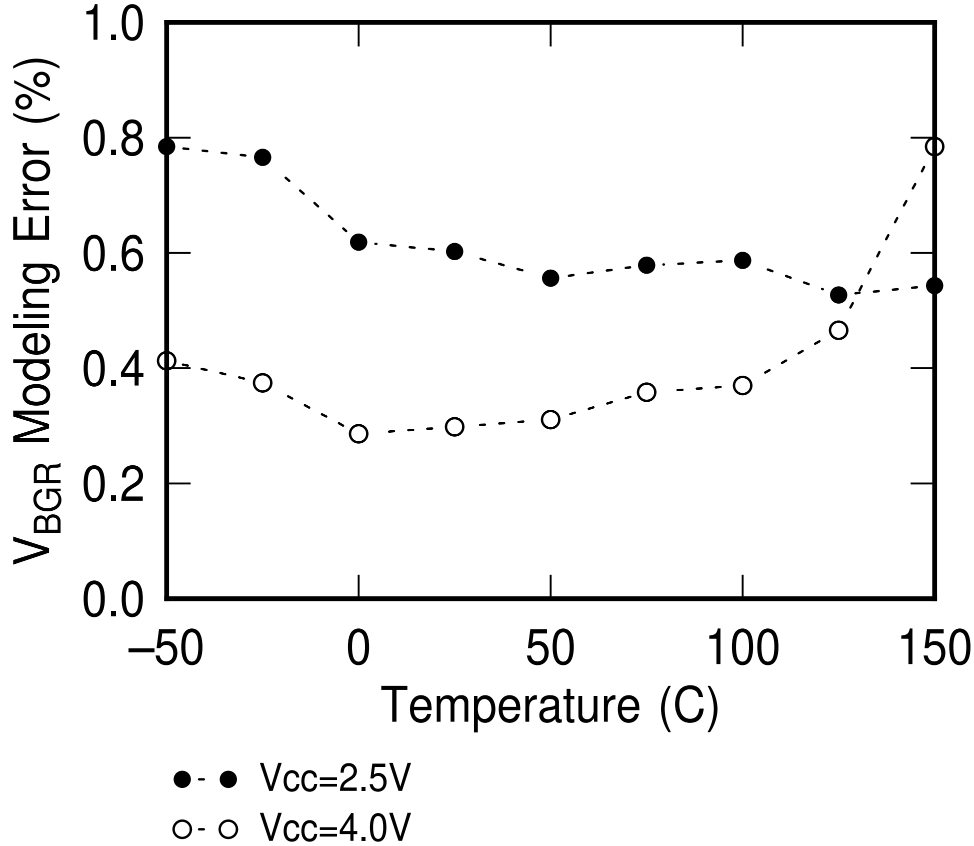

Fig. 3. Simulated minus measured $V_{BGR,}$ expressed in percent.

Table 1: Summary of the bandgap reference circuit.

Parameter	Measured	Simulated	Units
Output Voltage	1.328	1.336	V
Supply Current	0.675	0.664	mA
Temperature Drift	±25.1	±22.5	ppm/°C
PSRR(DC)	23.5	23.7	dB

Technology: 0.35µm SiGe BiCMOS, 3-level metal

Supply Voltage: 2.0 to 4.0 V

Area: 300µm x 150µm