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A 5.5-GHz Low Noise Amplifier in SiGe BiCMOS

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Abstract

A 5.5-GHz low-noise amplifier (LNA) with switchable gain and temperature and supply-voltage compensation implemented in SiGe BiCMOS is presented. The LNA gain (S_{21}) and 50-Ω noise figure are 14.1 dB and 2.4 dB, respectively, at 25°C. An on-chip proportional-to-absolute temperature (PTAT) current reference reduces the variation in S_{21} and $NF_{50\Omega}$ to 0.35 dB and 0.5 dB, respectively, from 0 to 100°C. The input third-order intermodulation intercept is +1.4 dBm. The circuit consumes 4.7 mA total current from a 2.5-V supply.

1. Introduction

Portable wireless data applications place stringent requirements on the design of the low-noise amplifier, a critical component of the wireless receiver. Desirable LNA features include low manufacturing cost, low power dissipation (to extend battery life), high gain, low noise figure, low sensitivity to ambient temperature and supply voltage, and the ability to switch to a low-gain state in the presence of a high received signal strength.

This paper presents a monolithic LNA for the emerging wireless bands at 5-6 GHz. The circuit features 14.1 dB of gain and a 2.4 dB noise figure at 5.5 GHz, with a 3-dB bandwidth of 2 GHz. It has an on-chip proportional-to-absolute-temperature current source which minimizes the dependence of gain and noise figure on temperature and supply voltage. It also features a high/low gain switch, with a 20X difference between the high and low gains. To achieve high performance at low cost and low power, the LNA is implemented in IBM's SiGe BiCMOS process.

2. SiGe BiCMOS Process Technology

The LNA was designed in IBM's 200-mm SiGe BiCMOS technology. This three-level-metal (Al) technology, with a substrate resistivity of 10-20 Ω-cm, features a Si/SiGe HBT with an emitter width of 0.5µm and a cutoff frequency (f_T) and maximum oscillation frequency (f_{MAX}) in excess of 45 GHz and 60 GHz, respectively, NMOS and PMOS devices with a nominal L_{eff} of 0.35µm, polysilicon and diffused resistors, high-density MOS and high-Q metal-insulator-metal (MIM) capacitors, varactor diodes, and inductors [1].

3. Low-Noise Amplifier Design

The LNA is comprised of two sections: the amplifier core and the PTAT reference. The amplifier core schematic is shown in Fig. 1. This circuit consists of two parallel cascode amplifier stages ($Q_{1,2}$ and $Q_{3,4}$)[2]. The gain in the $Q_{3,4}$ branch is set to be 20 times greater than that in the $Q_{1,2}$ branch, through the use of 20 devices in parallel in $Q_{3,4}$ and the biasing of both Q_1 and Q_3 from the same PTAT bias node, which sets the collector current in $Q_{3,4}$ to 4mA nominal. A PMOS switch P_1 combines with these parallel gain paths to provide a high/low gain switch, as follows. In the high-gain state, external input V_{CON} is set to V_{CC} to disable P_1. The input signal is then amplified by both parallel cascode amplifiers and directed to the output. In the low-gain state, V_{CON} is set to 0V to enable P_1 and shunt Q_4. The input signal is then amplified only by $Q_{1,2}$, and the gain is thus 1/20 of that in the high-gain state.

The on-chip inductor L_1 and on-chip MIM capacitor C_1 comprise a tuned load to provide a peak in the gain at 5.5 GHz. The on-chip inductor L_2 in the emitters of the input devices $Q_{1,3}$ provides input impedance matching.

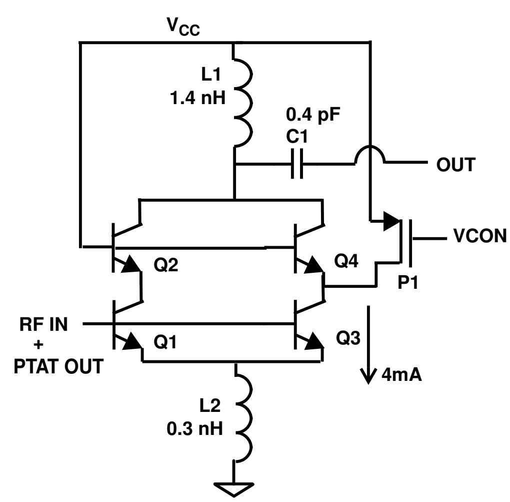

Figure 1. Amplifier core schematic

The spiral inductors are implemented using a 2µm thick top wiring level, which gives a low series resistance for the inductors and an inductor quality factor Q of about 8 at 5.5 GHz. The total dielectric thickness under the top metal is about 5.2µm, which provides a very high self-resonance frequency (above 20 GHz) for the inductors.

A 0.5x2.5μm^2 emitter geometry is chosen for the NPN cell, to give a base resistance of about 180 Ω. The input device Q_3 is constructed of 20 of these cells in parallel, for a base resistance of about 9 Ω at the input. This low base resistance reduces the overall LNA noise figure.

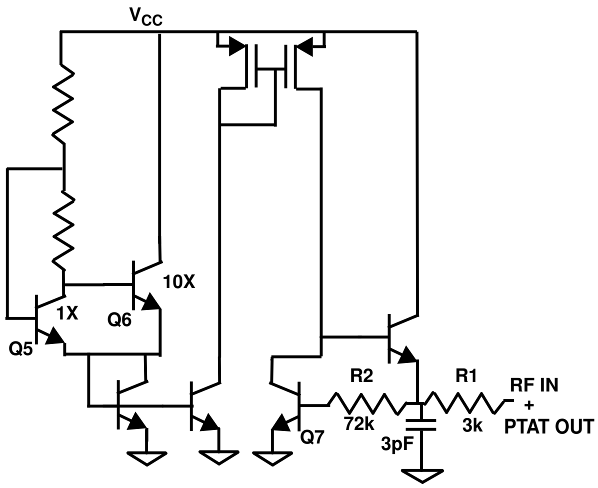

Figure 2. PTAT bias circuit schematic

The PTAT bias circuit schematic is shown in Fig. 2. The circuit uses the positive temperature coefficient of the difference between the base-emitter voltages (V_{BE}) of two NPN transistors having different emitter areas (Q_5 and Q_6, with Q_6 10X larger than Q_5) to generate a PTAT current to bias the NPN base input of the amplifier core. The motivation for using a PTAT bias in the LNA is as follows. The gain of the LNA is proportional to the transconductance $g_m = qI_C/kT$ of the amplifying transistors Q_1 and Q_3, where I_C is the collector current of the transistor and T is absolute temperature. If the transistors were biased at constant I_C, the gain would decrease with temperature. Instead, the PTAT biasing increases I_C with temperature to keep the gain roughly constant over temperature.

Resistor R_1 in Fig. 2 isolates the PTAT from the RF input, to maximize the transfer of RF signal to the LNA and minimize signal transfer into the PTAT. Resistors R_1 and R_2 set the current gain ratio between the LNA current (I_{C1}+I_{C3}, in Fig. 1) and the PTAT current (I_{C7}, in Fig. 2) to be approximately R_2/R_1.

4. Measurements and Discussion

The LNA scattering parameters and noise figure are measured on-wafer from 2 to 10 GHz using an ATN Microwave automated measurement system. The gain

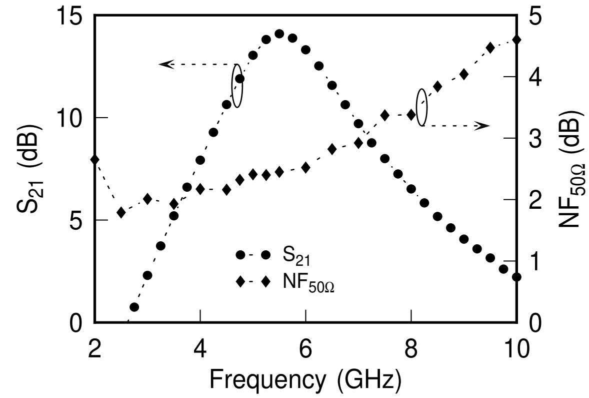

Figure 3. Measured S_{21} and $NF_{50\Omega}$ at 2.5V, 25°C

and 50-Ω noise figure at the nominal 2.5-V supply and 25°C are shown in Fig. 3. At 5.5 GHz, S_{21} = 14.1 dB and $NF_{50\Omega}$ = 2.4 dB. The corresponding available gain (G_a) and minimum noise figure (NF_{min}) are 15.8 dB and 2.1 dB, respectively. The S_{21} and S_{11} in the high and low gain states are shown in Figs. 4 and 5, respectively. The 24.5 dB difference in gain is close to the 26 dB (20X) ratio set by the emitter areas of Q_3/Q_1 in Fig.1. The cor-

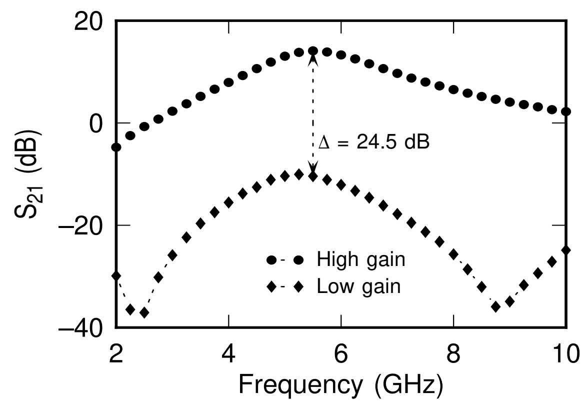

Figure 4. Measured S_{21} at 2.5V, 25°C

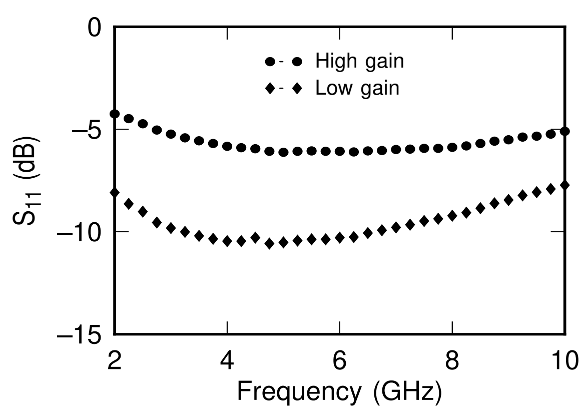

Figure 5. Measured S_{11} at 2.5V, 25°C

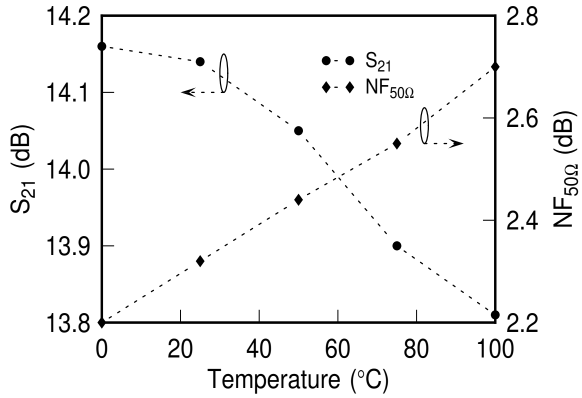

Figure 6. Temperature dependence of S_{21} and $NF_{50\Omega}$

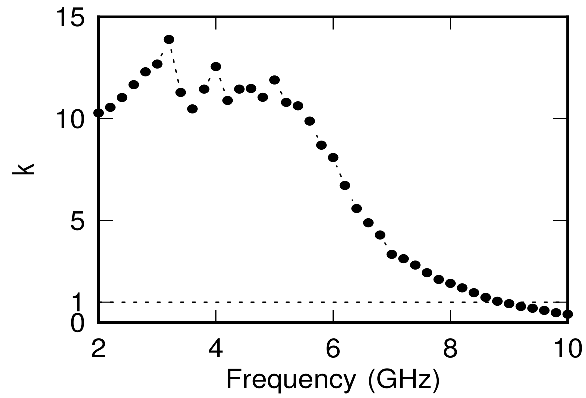

Figure 8. Rollett stability factor at 2.5V, 25°C

responding S_{22} and S_{12} in the high/low gain states at 5.5 GHz are -8.9/-12.6 dB and -44/-46 dB, respectively.

The gain and noise figure stabilization provided by the PTAT biasing is shown in Figs. 6 and 7, which plot the variation in S_{21} and $NF_{50\Omega}$ over temperature at 2.5V, and over V_{CC} at 25°C, respectively. We see that the temperature coefficients of gain and noise figure are -0.0035dB/°C and +0.005dB/°C, respectively. The voltage coefficient of S_{21} is about +1dB/V, and that of $NF_{50\Omega}$ is near 0. The total supply current has a temperature coefficient of +0.016mA/°C. The normalized temperature coefficient of an ideal PTAT current (I=aT, a=constant) is 1/T. This ideal value (i.e. 1/298) is very close to the value of 1/294 (0.016mA/°C/4.7mA@25°C) measured for this circuit, thus indicating the high linearity of the PTAT circuit. The supply current has a voltage coefficient of +2.0mA/V. A version of this LNA using PMOS loads and a start-up circuit in the PTAT biasing is presently in fabrication and is expected to exhibit improved power supply rejection.

The linearity of the LNA is measured by applying two RF signals at frequencies f_1=5.50 and f_2=5.51 GHz and measuring the power levels of the third-order intermodulation products at $2f_1$-f_2 = 5.49 GHz and $2f_2$-f_1 = 5.52 GHz. At 2.5-V supply and 25°C ambient temperature, the measured input third-order intermodulation intercept point (IIP_3) is +1.4 dBm in the high-gain state and +1.1 dBm in the low-gain state. The 1-dB gain compression point (P_{-1dB}) is -12 dBm in the high-gain state and -13 dBm in the low-gain state. These linearity results vary less than 1dB over the range of supply voltages from 2.5V to 3.3V.

Figure 8 shows the Rollett stability factor k of the LNA, computed from the measured S-parameters at 2.5V and 25°C. A network with a value of k>1 is unconditionally stable; thus Fig. 8 shows the LNA is unconditionally stable over the frequency range of interest. The value of k remains >1 over the measured temperature and supply voltage ranges.

Figure 9 shows the microphotograph of the LNA. The total chip area is 700 x 700μm^2 including the pads, with an active circuit area of roughly 400 x 400μm^2. A first level metal ring under the pads provides a solid ground with six large substrate contacts. This metal-1 ring also isolates the RF pads on the top-level metal from losses in the substrate. The input and output RF pads use a ground-signal-ground configuration and are located on opposite sides of the chip to improve the isolation.

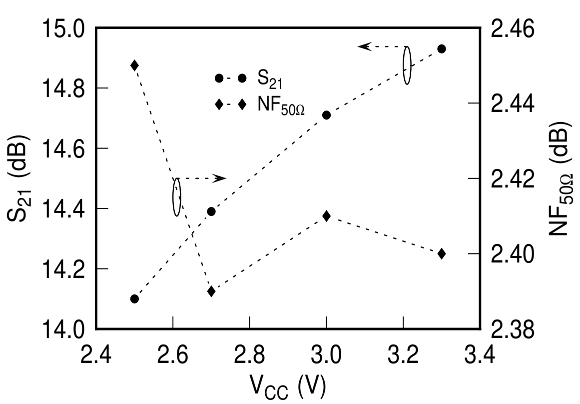

Figure 7. Supply dependence of S_{21} and $NF_{50\Omega}$

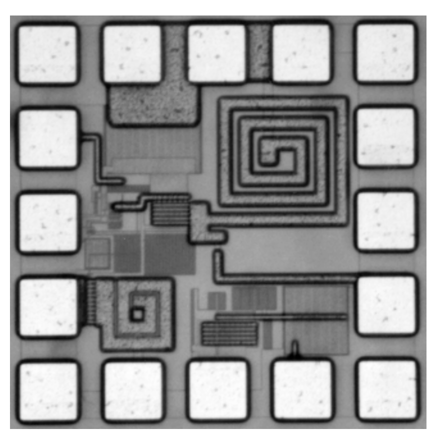

Figure 9. Chip microphotograph

Table 1 summarizes the performance of the LNA. These measured results, especially gain, noise figure, and temperature stability, are comparable with those of other recently-published LNA's which feature temperature compensation and switchable gain but operate at lower frequencies, e.g. 2.5 GHz [3].

Table 1: Summary of the 5.5-GHz LNA

Parameter	Value	Units
S_{21}	14.1	dB
$NF_{50\Omega}$	2.4	dB
IIP_3	+1.4	dBm
S_{21} Temp. Coeff.	-0.0035	dB/°C
$NF_{50\Omega}$ Temp. Coeff.	+0.005	dB/°C
Supply Current	4.7	mA
Supply Voltage	2.5	V

Table 2 compares the measured values to recently published C-band LNA results in other technologies. The figure of merit is defined as the ratio of peak S_{21} to the product of $NF_{50\Omega}$ and DC power consumption, P_{DC}, where $NF_{50\Omega}$ is measured at the frequency of peak S_{21} (5.5 GHz, 5.8 GHz, 5.8 GHz and 5.0 GHz for the SiGe, Si bipolar, GaAs MESFET and GaAs HBT circuits, respectively). It should also be noted that the other LNA's referenced in Table 2 have neither switchable gain nor temperature-compensated biasing.

Table 2: Figures of merit for recent 5-6 GHz LNA's

Technology	S_{21} (dB)	$NF_{50\Omega}$ (dB)	P_{DC} (mW)	Fig. of Merit (mW^{-1})
SiGe HBT (this work)	14.1	2.4	11.8	0.50
Si bipolar [4]	7.5	4.5	7.7	0.22
MESFET [5]	16.5	3.6	10	0.46
GaAs HBT [6]	18.2	2.4	72	0.11

5. Conclusion

A 5.5-GHz LNA with switchable gain and on-chip temperature and supply voltage compensation, implemented in a SiGe BiCMOS technology, is presented. The LNA gain and noise figure are 14.1 dB and 2.4 dB nominal, with temperature coefficients of -0.0035 dB/°C and +0.005 dB/°C. The LNA dissipates less than 12 mW from a 2.5-V supply at 25°C.

6. Acknowledgments

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7. References

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