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BiCMOS Process Integration and Device Optimization: Basic Concepts and New Trends

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BiCMOS Process Integration and Device Optimization: Basic Concepts and New Trends

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Contents:

The process integration issues and the aspects of CMOS and bipolar transistor optimization in BiCMOS technology are reviewed in this article. In one section, a sample BiCMOS fabrication process is discussed to provide an entry to the subject for readers who are not familiar with the details and the nomenclature of semiconductor technology. The remainder of the paper deals with questions related to state-of-the-art BiCMOS and addresses new directions in BiCMOS processing. The convergence of the structural requirements for the bipolar and CMOS devices with miniaturization and the modular concepts of current BiCMOS are described and highlighted by various examples. The prospects of BiCMOS in the fast evolving broadband and wireless communications markets are addressed.

BiCMOS-Prozeßintegration und Bauelementoptimierung: Grundlegende Konzepte und neue Trends

Übersicht:

Problemstellungen der Prozeßintegration und der CMOS- und Bipolartransistoroptimierung in BiCMOS-Fabrikationstechnologie sind in diesem Aufsatz zusammengefaßt und diskutiert. In einem Abschnitt wird ein exemplarischer BiCMOS-Prozeß beschrieben, um Lesern, die nicht mit den Verfahren der Halbleitertechnologie vertraut sind, einen leichteren Einstieg in die weiteren Diskussionen zu bieten. Der Hauptteil des Artikels behandelt gegenwärtige Fragen und neue Richtungen der BiCMOS-Fabrikationstechnologien. Die Konvergenz struktureller Anforderungen für CMOS und bipolare Bauelemente im Zuge der Miniaturisierung, sowie die modulare Gestaltung moderner BiCMOS-Prozesse, sind beschrieben und durch Beispiele belegt. Die Entwicklungschancen für BiCMOS im Bereich der drahtlosen und der Breitband-Kommunikationstechnik werden angesprochen.

1 Introduction

The basic idea of BiCMOS, that means the integration of planar bipolar and metal-oxide-semiconductor (MOS) transistors on the same silicon chip, reaches as far back as 1969 [1]. But it was not until about 1985 that this integration concept was employed by the industry. The large number of photolithographic masks required for BiCMOS was certainly one of the reasons for this time delay, until the introduction of step-and-repeat photolithographic systems with automatic overlay registration made the photolithography process more comparable in cost to the other fabrication steps. Another, probably more important reason for the interest in BiCMOS came from circuit design. CMOS has its strength in integration density, but its weakness is the poor load driving capability because of the square-law relationship between current and voltage [2]. This relationship is exponential for a bipolar transistor which makes it a fast switching device even under heavy loading conditions. The weakness of the bipolar transistor is that the emitter-base voltage drop does not scale with device size so that the power density increases as the transistor area is reduced [3]. That means that for a given maximum power density the distance between devices on the chip, relative to the transistor area, has to increase with miniaturization. Consequently, the circuit speed cannot improve in proportion with the device scaling. It becomes obvious that the strength of CMOS is the weakness of bipolar, and vice versa. A digital integrated circuit (IC), which uses CMOS to implement the logic functions and bipolar transistors in the output stage to transfer the output signal to another, distant circuit without significant delay, can therefore be the basis for static random access memories (SRAMs) with shorter access time or microprozessors with higher logic speed compared to pure CMOS or bipolar designs.

BiCMOS has not only been applied to fast logic circuits and SRAMs, but also to smart power and mixed-signal circuits. A large number of papers describing the various applications and processes are compiled in the reference list of this paper [4] - [44]. Table 1 shows a subset sorted by company and with information on publication dates and process characteristics. This summary illustrates already at first glance that there is not one unique BiCMOS integration process for all those applications. In the one extreme we find processes which are strictly CMOS-based and have a bipolar transistor added at the expense of only a few additional photolithographic masks. In the other extreme BiCMOS processes provide a high-performance npn device, thin-film transistors (TFTs) for ultra-dense SRAMs, or special passive components and pnp transistors for analog and mixed signal applications.

In this paper we will not discuss the various circuit design techniques for BiCMOS and address them only very briefly where necessary. The following sections will solely deal with the fabrication processes for BiCMOS and the associated aspects and trade-offs in device design. In

Section 2 we will describe a basic BiCMOS integration process and illustrate the principles of coordinated CMOS and bipolar transistor optimization for those readers who are not familiar with the concepts and nomenclature of BiCMOS process design. In Section 3 we will first discuss the design of CMOS and bipolar devices independently and review afterwards the trade-offs for device design in balance with the overall BiCMOS process complexity. Section 4 is devoted to new directions in BiCMOS integration and to new applications. A summary and conclusions will follow in Section 5.

2 BiCMOS Integration Principles and Trade-offs

The art of developing a BiCMOS integration process is to combine MOS devices, which have a lateral current flow, and bipolar transistors, which have a vertical current flow, on the same chip without sacrificing the performance of either device. The difficulty lays in the fact that the thermal cycles during processing affect the doping concentration profiles of both devices and that some doped regions and material layers are shared. In many cases, as Table 1 illustrates, a BiCMOS process was derived from a core CMOS or bipolar process, which can be desirable to save development time. But the danger can be that the added device ends up to have sacrificed performance, or otherwise the total mask count can become much higher compared to a balanced BiCMOS process. Besides these performance issues, it is also important to achieve a high integration density, in particular for BiCMOS-SRAMs.

In Fig. 1 we have sketched an exemplary BiCMOS process to be able to highlight the most important integration issues. The starting substrate is a low-doped, p-type silicon wafer (p^--Si). The substructure of the CMOS and bipolar devices is shown in Fig. 1a. First, a zero-level mask is used to recess the silicon in a region away from the devices in order to provide a first alignment mark for photolithography. Then, a heavy dose of arsenic is implanted in selected regions by using another mask level. A high dose of boron is implanted blanket into the wafer surface to dope the silicon p-type outside of the n^+-regions, but the dose is kept low enough so that the n^+ regions cannot be compensated by the boron. Otherwise an additional mask level would be required. Next, an undoped epitaxial layer is grown onto the wafers. This forms buried n^+-layers under the npn and pMOS devices and a p^+-layer under the nMOS transistor. A patterned field oxide is grown or deposited with windows for the nMOS, the pMOS, the npn emitter-base, and the npn collector contact by using another mask. It is obvious that the zero-level mask is needed to be able to align the n^+-regions to the oxide isolation; the n^+-region itself is not detectable by the alignment system of the photolithographic stepper. A reach-through contact to the npn subcollector is then implanted using a mask. Two masks are used to implant medium

doses of phosphorus and boron which form n- and p-wells for the CMOS and the n-collector for the npn sites. Next, the gate oxide is grown and then removed from the npn windows by using a block-out mask before the combined gate and emitter polysilicon film is deposited. Usually a thin polysilicon film is deposited onto the gate oxide before patterning in order to protect the oxide/polysilicon interface [45]. The cross-section of the structures up to this point are shown in Fig. 1a. The fabrication process continues with a shallow boron implant for the intrinsic base region of the npn transistor, which requires a block-out mask. A thicker polysilicon film is then deposited to complete the gates of the CMOS devices and to form the npn emitter. Two block-out masks are used to dope the polysilicon of the n^+- and p^+-CMOS gates and the n^+ emitter. The polysilicon is then patterned at minimum lithographic line width. During this etch the silicon on the npn side is somewhat recessed. Dielectric spacer sidewalls are formed along the CMOS gates and the npn emitters. The cross-section of the devices at this stage is shown in Fig. 1b. Two block-out masks are then used to implant high doses of arsenic or antimony and of boron to form the source and drain junctions (S/D) of the CMOS devices and the extrinsic base contacts of the bipolar transistor (Fig. 1c). A dielectric film is then deposited for isolation, and contacts are opened. Because of the different depths of the contacts to the gates and emitter and to the S/D, base and collector contacts, sometimes two contact masks are used. Otherwise the dry etch process for the contacts needs to have a very high selectivity to avoid excessive overetch into the gate and emitter polysilicon. The metal via contacts are then formed by depositing tungsten (W) and by applying a chemical-mechanical planarization process. Finally, aluminum-copper (AlCu) lines are formed by a similar technique, which requires another mask. The completed BiCMOS structure at first metal level is shown in Fig. 1d. The total mask count adds up to 16, which increases by multiples of 2 for additional metal levels.

The description of this sample BiCMOS integration process showed that various doped regions are part of both the CMOS and the bipolar transistors. They have therefore to be tailored for several device parameters. That is particularly the case for the p^+ buried layer. It is introduced to suppress latchup, to compensate for arsenic autodoping effects, and to avoid punchthrough between adjacent n^+ buried layers: Latchup is a result of a thyristor action between the sources of the CMOS transistors due to the parasitic npnp structure. This effect can be suppressed if the current gains of the imbedded npn and pnp transistors, which form the four-layer substructure, can be kept as small as possible. It is obvious that this is achieved by raising the doping levels underneath the CMOS, i.e. by forming retrograde well doping profiles [46]. Another reason for the formation of the p^+-buried layer is that lateral autodoping from the n^+-layer during epitaxy needs to be compensated by a higher boron doping [47]. Among the electrical considerations, punch-through effects between closely spaced n^+ regions call for high boron doping but the required breakdown voltage at the n^+/p^+-junctions sets an upper limit. Another trade-off comes

with the choice of the thickness and doping concentration of the epitaxial layer which forms both the collector of the npn and the n-well of the pMOS device. Doping level and epi thickness on the npn side define the maximum current density (knee current density), the collector-base capacitance (C_{CB}), and the breakdown voltage of the device. A thin epi layer, however, increases the drain junction capacitance of the pMOS which is the weaker device in CMOS. This is one of the critical design parameters for which a decision has to be made towards a high-performance bipolar or CMOS device in the BiCMOS process. High-performance design for both devices is to some extent possible by investing an additional mask to form separate n-well and collector doping profiles, but the epi thickness remains to be a compromised parameter in the design.

A second significant trade-off results from the shared polysilicon layer for CMOS gates and npn emitter and the shared dielectric spacer-sidewall. The spacers thickness needs for one to be designed for the right amount of lateral diffusion from the S/D contacts, so that sufficient link to the channel under the CMOS gates is achieved. But the same degree of lateral diffusion on the npn side would result in severe peripheral tunneling currents due to the close proximity, or even the merger, of the p^+ extrinsic base and the n^+ emitter diffusions [48],[49]. To circumvent this tunneling problem, a certain amount of overetch is usually added to the gate etch so that a silicon recess is achieved on the npn side (no overetch on the CMOS side due to the gate oxide and etch selectivity). In that way, the extrinsic base is shifted below the emitter-base junction and the mentioned peripheral effects are suppressed. The overetch, however, must not become too large because otherwise the link between the extrinsic base contact and the intrinsic base region becomes very resistive and the npn performance is degraded [50],[51]. There are many more trade-offs in BiCMOS process optimization but the two issues discussed are illustrative examples on how some degree of the device performance may have to be sacrificed for the benefit of a cost-performance optimized BiCMOS technology. The independent modification of process elements can allow to design the devices closer to their optimum performance but such process improvements come always at the price of a higher mask count. In the next section we will first discuss the various structural design options for stand-alone CMOS and bipolar transistors (the "core" technologies) before we discuss the different generic BiCMOS integration processes.

3 CMOS and Bipolar Transistor Design and BiCMOS Process Options

(A) CMOS Structural Design

CMOS optimization follows strictly the scaling principles for this device family [2], and three stages of CMOS scaling are shown in Fig. 2a-c. For minimum channel length down to about 0.8

μm, CMOS can be designed as illustrated in Fig. 2a. A single-workfunction gate conductor, an n-well for the pMOS, and S/D contacts without extensions (also called lightly-doped drain (LDD)) are sufficient at this gate length. p^+-substrates with p-doped epitaxial layers are used to suppress latchup. For device isolation, a recessed oxide (ROX) is sufficient to achieve the required integration density [1]-[12],[18]-[44]. The total mask count for the described part of this simple CMOS process is only 5. For channel lengths at and below 0.8 μm it is desirable to provide also a p-well for the nMOS transistor to maintain control of the threshold voltage of that device (shown in Fig. 1b) [52]. At 0.5 μm, dual workfunctions are required to be able to design for symmetric threshold voltages, which increases the mask count by another mask. It is common practice to save block out masks for the polysilicon gate formation by sharing the implants for the poly with those of the S/D junctions (Fig. 2b). Beyond 0.35 μm, the formation of S/D extensions becomes indispensable to ensure small short-channel effects [52], [53], good channel length control, and adequate device reliability [54]. Shallow trench isolation will have to replace ROX at this scaling stage for density reasons [17], [55]. The mask count for the discussed part of the CMOS process is then increased to 9 (Fig. 1c), i.e. a factor of 1.8x compared to the simple CMOS process in Fig. 1a. For the transition of the structure in Fig. 1c to BiCMOS, the p^-/p^+-substrate has to be replaced by low-doped wafers with n^+- and p^+-buried layers in order to provide a subcollector for the npn transistor but still maintain latchup suppression. This process change requests two additional masks, one for the n^+-buried layer and one for a zero-level mask (see Section 2). For CMOS-based BiCMOS processes, the additional cost for the added low-performance bipolar decreases relatively with scaling the CMOS. A prominent example is the fact that Intel uses a BiCMOS process for the fabrication of the Pentium chip with only little added complexity to the core 0.35 μm CMOS. In light of the projected market volume in broadband and wireless communication technology, the demand for BiCMOS processes with an ultra-high performance bipolar is at the horizon. Next we will therefore discuss the generic bipolar transistor structures in detail.

(B) High-Performance Bipolar Transistor Design

As already mentioned, the main differences in the BiCMOS processes listed in Table 1 are in the choice of the bipolar device structure. From the published data on BiCMOS processes it becomes obvious from Fig. 3 that the f_T of npn transistors in CMOS-based processes is generally smaller than for bipolar-based technologies where major emphasis is put on the optimization of the bipolar transistor. While the bipolar performance scaled roughly with CMOS channel length for most of the data in Fig. 3, the very recent developments focus very strongly on maximizing bipolar speed in a BiCMOS process. This trend is related to the evolving interest in

RF&Microwave technologies based on silicon, which will be discussed in more detail in Section 4. The lower f_T for the CMOS-based technologies relates to design penalties for the bipolar if it is integrated with a core CMOS. Using an n-well, which is optimized for the CMOS, as collector region always limits the maximum current density and thus causes that the f_T depends strongly on the device parasitics, in particular the emitter-base capacitance (C_{EB}) and C_{CB}. Sharing the poly-emitter doping with the n^+-S/D implant and exposing it to the thermal cycle of the S/D anneal results in a relatively deep emitter diffusion, which degrades the npn transistor as well. But the f_T indicates only the trade-offs which were made for the npn device in terms of vertical doping profile. Of similar importance for the npn device performance in a BiCMOS circuit are the transistor parasitics which depend on the structure used for transistor integration. Four generic bipolar device structures are shown in Fig. 4a-d. All transistors are drawn with silicided extrinsic base contacts because silicidation is a standard process feature in CMOS and is therefore available in BiCMOS for bipolar transistor integration [56]. The first three structures (Fig. 4a-c) have been frequently used in BiCMOS. A good figure-of-merit for the bipolar circuit performance is the ECL gate delay. A summary of the ECL gate delays as a function of nFet channel length and with indication of the transistor structure used is shown in Fig. 5 (from Table 1). The improvement of bipolar transistor performance with lithography generation is obvious, but there is no apparent dominance of any particular structure. This would at first not be expected, because for pure bipolar technologies one would assume the Inside-Spacer (IS) transistor to perform better than the Outside-Spacer-type (OS). Both IS and OS structures should clearly outperform the Non-Self-Aligned (NSA) devices. There are several reasons that this is not necessarily the case for ECL results based on BiCMOS processes. A comparison of ECL gate delays is only meaningful if they are achieved at the same switch current density, but the design points e.g. in BiCMOS-SRAMs compared to BiCMOS for RF&Microwave applications are quite different. Also, the use of a self-aligned transistor in SRAMs may in the first place be motivated by density aspects (e.g. [20],[24],[26],[57]), while for mixed-signal or high-speed analog and logic applications the driving force is mainly performance (e.g. [4],[9],[15],[18]). That means that self-aligned integration of a bipolar transistor can have advantages in terms of achieving maximum performance, minimum power for a given performance, or in making the bipolar device dimensions compatible to that of the CMOS devices [57]. It is therefore worthwhile to discuss the structure options for bipolar transistors in more detail.

Integrating a bipolar transistor perfectly would mean to contact the internal, one-dimensional npn device without generating any additional resistances and capacitances. But with the challenge to contact a vertically operating device in a planar process, this goal can only be achieved to a certain extent. The dominant device parasitics, the base resistance (R_B), the collector-base capacitance, and the collector-substrate capacitance (C_{CS}), will always have a considerable effect

on the circuit performance. Their qualitative impact on the ECL gate delay is illustrated in Fig. 6. It is obvious that the capacitances dominate the transistor performance at low current, while the circuit delay is limited at high power by R_B [58]. The abruptness of the intrinsic doping profile is represented by the base transit time (τ_B) which is the dominant component in f_T. While C_{CS} can be independently addressed by the choice of the transistor isolation structure, R_B and C_{CB} depend on the lateral design of the emitter-base regions. In the non-self-aligned structure in Fig. 4a, one lithographic overlay has to be considered between emitter and base contacts, which leads to a comparably large collector area and thus a high C_{CB}. The required overlay results also in a considerable space between the low-resistive extrinsic base contact and the active base region (R_{bx1} + R_{bx2} and R_{bi} in Fig. 7). That increases the base link resistance (R_{bl} in Fig. 7) and thus leads to a high R_B. The NSA transistor has therefore a relatively high R_B *and* C_{CB}. The base resistance can be considerably reduced by fabricating an OS transistor which allows for a very close proximity of the silicided extrinsic base to the emitter-base junction due to self-alignment (Fig. 4b). This structure also naturally integrates with the CMOS devices (Fig. 1) which makes it attractive for CMOS-based BiCMOS processes. The base contact, however, has to be placed within the silicon area so that C_{CB} is still relatively large. C_{CB} is reduced significantly in the IS structure which is shown in Fig. 4c. This device has polysilicon base contacts formed over the field oxide, which allows to shrink the collector window considerably. It is possible to implant the collector doping self-aligned through the emitter window in the base polysilicon, which reduces C_{CB} even further. The emitter is self-aligned to the extrinsic base contact through the formation of an inside sidewall-spacer [59]. The inside-spacer leads to a sublithographic emitter width which helps to reduce the intrinsic base resistance component of the transistor. If integrated as part of a BiCMOS process, the IS transistor requires additional mask levels and a second polysilicon layer for the emitter formation, and is therefore preferred in high-performance BiCMOS processes. It has the advantage that the emitter formation can be separated from the nMOS-gate doping. Even though the R_{bi} of the device can be small, the total base resistance may be high because a large part of the extrinsic base contact cannot be silicided (R_{bx2} in Fig. 7). Recently, a novel self-aligned bipolar transistor structure, which combines the merits of the OS *and* the IS structures, was introduced [60]. The fabrication process starts similar to that of the IS device so that C_{CB} can be minimum (Fig. 4d). It uses a chemical-mechanical planarization technique which converts the structure after emitter formation to an OS device, so that R_{bx} is minimum as well. The structure uses an epitaxially grown intrinsic base which can be designed for very low base resistance so that the total R_B can become extremely small. During the epitaxial growth polysilicon is deposited self-aligned to the edges of the collector window for the extrinsic base contacts [61]. The detailed fabrication process for this device is described in [60]. For BiCMOS integration of this device it is preferable to use an implanted polysilicon process for the emitter formation instead of the in-situ doped poly used for the high-performance bipolar

process in [60]. This issue will be readdressed somewhat later.

From the discussion of the different bipolar device structures in Fig. 4 it becomes clear that using the IS or the OS/IS structure in a BiCMOS process would mean to move up in process complexity. But in result of this effort it is possible to achieve very high bipolar device and circuit performance. In fact, a few of the record breaking results in bipolar technology over the past years were demonstrated in BiCMOS processes [9],[15],[31].

Such high performance can only be achieved if, besides the mentioned structural aspects of device optimization, the thermal cycles in the bipolar part of the fabrication process can be optimized largely independent from the CMOS. Special care has to be taken in the design of the base link region near the edges of the emitter-base junction. The intrinsic base is usually very thin, to reduce the base transit time at the price of a high sheet resistance. R_{bi} becomes smaller in operation due to resistance modulation effects [62], but the thin base region next to the emitter edge (R_{bl} in Fig. 7) can easily be the cause of a very high base resistance. R_{bl} can be tailored by diffusing the heavily doped extrinsic base contact closer to the emitter edge [63]. Attention has to be paid that the diffusion fronts of extrinsic base and emitter do not overlap, in order to avoid a parasitic increase of the base Gummel number at the emitter edge. This would reduce the current gain and degrade the speed of the device [48]-[51]. The high doping levels at the emitter periphery also lead to high leakage currents in reverse bias [64],[65], which is a concern in BiCMOS circuits for logic and SRAMs [66].

It is also important to consider that the lateral extrinsic base diffusion leads necessarily to a deeper collector-base junction in the extrinsic base region. For a high performance transistor, in which the collector epitaxial layer is thin in order to permit a high current density [62], the consequence may be a significant increase of the extrinsic collector-base capacitance (C_{cbx} in Fig. 7). It becomes obvious that the extrinsic base contact diffusion in a high-speed bipolar transistor has to be carefully designed in a tradeoff between C_{CB} and R_B. A weak or strong base link was found to have a profound effect on bipolar circuit performance at high or low current density, respectively [67].

The last issue which should be discussed is the design of the polysilicon emitter. The vertical doping profile of a high-performance bipolar transistor requires the formation of an extremely shallow emitter junction. In-situ doped poly emitters have therefore been introduced to ultra-high-speed technologies [60],[68]-[70]. For BiCMOS these in-situ doped poly emitters can be impractical because they require an additional mask and may cause problems in poly film removal outside of the bipolar device. The use of ion-implantation for doping the emitter-poly

remains still to be the favorable process in BiCMOS because it allows to share the undoped polysilicon film with the CMOS or other devices, and to dope it locally as required. But with the formation of very shallow emitters by using implanted polysilicon it was found that the edges of the polysilicon emitter were insufficiently doped so that the peripheral emitter-base junction became too shallow (as illustrated in Fig. 7). This had deleterious effects on the ideality of the base current [71]. It is therefore important that the emitter doping and anneal can be adjusted independently in a high-performance BiCMOS process in order to minimize these effects.

With the accomplished in-depth understanding of the design issues for the CMOS and bipolar transistors it is now possible to return to the discussion of BiCMOS integration processes and the associated design trade-offs.

(C) Options for BiCMOS Processes Integration

The paradigm for BiCMOS process design has shifted through the different technology generations. The early BiCMOS approaches exploited the parasitic bipolar device which was derived from CMOS, thus no process complexity was added [72]. The 1.2 μm through 0.5 μm BiCMOS generations either pursued a low-mask-count design while compromising the bipolar performance, or processes were designed for high-performance of both CMOS and bipolar devices, though accepting an increased complexity. The 0.35 μm and 0.25 μm technologies, which are currently in development, can take advantage of the fact that the structural requirements for high-performance CMOS and bipolar transistors tend to converge [73]. More detailed discussion is necessary to understand these arguments.

Four generic BiCMOS processes, which represent different technology generations, are illustrated in Fig. 8. BiCMOS-A represents a strictly CMOS-based process in the 1.2 μm to 0.8 μm regime. Highly-doped p^+-substrates with a blanket p-type epitaxial layer are used like in core CMOS. The n-well of the pFet serves also as the collector of the bipolar transistor. The npn device is significantly degraded because the CMOS-optimized n-well is deep and no low-resistive subcollector is formed, so that the high current-drive capability of the bipolar transistor, and thus its speed, are limited. BiCMOS-A requires 2 additional masks to add the bipolar to the core CMOS. With addition of a subcollector and a reach-through contact, the npn speed can be significantly improved. Neglecting the difference in cost between the p^+/p^--wafers and the buried layer formation, the added mask count for bipolar device integration is 3 (BiCMOS-B, including a zero-level mask). Such a bipolar transistor will still not perform as well as its core bipolar counterpart because the emitter is common with the n^+-S/D formation, and thus relatively deep.

The n^+-subcollector forms a retrograde n-well which helps to suppress latchup in the CMOS. Since the n-autodoping during epitaxy is usually severe [47], a p-well is formed by counterdoping the n-epi. The B-type process applies about to the 0.8 μm to 0.5 μm generations. BiCMOS-C is a typical process for the 0.5 μm and 0.35 μm technologies. To satisfy density requirements, a p^+-buried layer is formed through a self-aligned implant after the n^+-layer is in place. The doping level of the p^+-layer must be judiciously chosen to balance punchthrough and avalanche effects, and to minimize the capacitance between the highly doped buried layers. Shallow trench isolation will replace the conventional recessed oxide for density reasons [17],[55]. Twin-well formation is used to have good control on both doping levels and to avoid well formation by counterdoping which degrades the carrier mobility [52]. The CMOS devices have dual workfunctions which can be formed together with the S/D implants. The npn's emitter is implanted independent of the n^+-S/D, and has a different dose, so that the bipolar performance is improved. The npn performance is further increased by using a self-aligned structure (the OS structure as an example in Fig. 8). A self-aligned silicide is used to lower the sheet resistances of S/D, gates, and the npn base contacts. The total mask count for this type of process is 15, with 4 additional masks for the bipolar. BiCMOS-D is suited for the 0.25 μm generation. The bipolar transistor has deep-trench isolation to reduce C_{CS}. Two additional masks are invested for the CMOS to form S/D extensions, also called lightly-doped drain (LDD). The total mask count for BiCMOS-D is 18. The bipolar transistor addition requires here 5 additional masks.

At this point we shall return to the hypothesis from the beginning of this Section. In the four processes which we just discussed, several structural elements are utilized in both types of devices. The higher the process complexity is (BiCMOS-A → BiCMOS-D), the more structural elements are shared. Key shared features are the n^+-buried layers, the sidewall-spacers used for the CMOS gates and the npn emitter, and the silicide on S/D and base contacts. It may also be possible to exploit the bipolar's deep trench isolation to reduce the sidewall capacitance between p- and n-wells [73]. The additional process complexity due to adding a bipolar transistor to the CMOS is about 30-35% for the four sample BiCMOS processes. That means that the additional investment for BiCMOS compared to core CMOS remains about constant with scaling, while the performance of the bipolar becomes closer to that of a pure bipolar technology.

The mask count tends to increase with device scaling, but for the same technology generation the number of masks can differ significantly depending on the application. Two examples will be given here. The process NEC I in Fig. 9a and Table 1 belongs to the 0.35 μm generation, yet requiring only 11 masks to first metal [26]. This is a process which has been rigorously developed towards mask savings. MeV ion implantation has been used to form the buried layer and well with the same photo mask [74]. The collector reach-through contact was formed as a

W-plug together with the contacts to M1. The S/D extensions, which are required at this channel length and which usually add two masks, have been formed by oblique rotating ion implantation. Finally, the intrinsic base implant is blanket, saving another mask. The mask count of the NEC I process is extremely low at the price, however, of very unconventional process steps. The other extreme is Northern-Telecom's process (Table 1, [29],[30]) which has a mask count up to 27 (Fig. 9b). This process had evolved from a 1.2 µm CMOS process with 14 masks to a 0.8 µm BiCMOS with 19 masks (to metal 3). Up to 8 more masks can be added to provide a vertical pnp, a TFT, a high-ohmic polysilicon resistor, polysilicon fuses, a linear polysilicon resistor, high-voltage FETs, and a dual-poly capacitor. The key feature of the process is its modular concept, i.e. features can be added or subtracted without altering the other device characteristics.

The modular design of the complex BiCMOS processes and the convergence of the structural requirements have another advantage: such BiCMOS processes can be easily directed towards new applications without major modifications. One can simply recompose the technology elements which are already in place to design new devices. A good example are the BiCMOS smart power technologies [22],[75],[76]. The BiCMOS process Motorola IIb (Table 1, [22]) was obviously adopted from an existing BiCMOS technology designed for logic and microprocessor applications (Motorola IIa, [21]). Due to the advanced process design of the 0.5 µm BiCMOS, twin-well structures ,implanted into a epitaxial layer, were used for the CMOS devices. That epi layer was ideally suited to serve in the designs of Lateral Diffused MOSFETs (LDMOS) and Lateral Insulated Gate Bipolar Transistors (LIGBT) as the blocking region for the high voltage. Only one self-aligned p-implant for the drift regions of the power transistors had to be added to establish a versatile smart power BiCMOS.

In spite of the benefits in modularity and structural convergence, the high process complexity of submicron BiCMOS remains a concern. BiCMOS technology scaling puts certain demands in process investment for the CMOS and bipolar transistors, as sketched in Fig. 10. The process complexity of the CMOS increases rapidly beyond 0.5 µm channel length, when twin-wells, shallow-trench isolation, S/D extensions, and dual workfunctions become a requirement. The investments for the bipolar transistor become significant when deep-trench isolation is introduced or further out when epitaxial Si or SiGe base formation becomes indispensable to arrive at cutoff-frequencies beyond 50 GHz with a low base sheet resistance. The development of BiCMOS does not necessarily follow exactly the directions indicated in Fig. 10. Some processes lean more towards the CMOS axis and avoid major investments for the bipolar part, such as Intels process for the Pentium chip [17]. Other processes are strictly bipolar-oriented, like IBM's SiGe-BiCMOS process which has been developed for single-chip solutions in RF&Microwave and telecommunication applications [16].

4. New Directions and Alternative Concepts of BiCMOS

(A) Complementary BiCMOS Technologies

The npn integration process in BiCMOS provides a lateral pnp transistor without any additional steps, but the performance of this device is poor. Performance similar to the npn can only be achieved by expanding the fabrication scheme and add a vertical pnp transistor [19],[21]-[23],[29],[39],[44],[77]-[80]. The pnp cutoff-frequency could be increased by about a factor of ten to beyond 1 GHz with vertical pnp's compared to the lateral structure, but in none of the mentioned CBiCMOS technologies it exceeds 5 GHz. For further optimization of the pnp, the process flow will have to be rearranged so that it is possible to approach an optimum design point for both the pnp and the npn transistors. That applies especially to the design of the buried-layer and collector designs, as well as to the base and poly-emitter formation of the pnp [81]. In bipolar-only complementary technologies it has been demonstrated that f_T's far beyond 10 GHz are feasible for the pnp without compromising the npn transistor [82]-[84]. Much higher performance for the pnp is in principle possible by investing into a SiGe complementary technology. f_T's as high as 55 GHz have been demonstrated for SiGe-pnp transistors [85]. The presently evolving market for portable wireless communications systems may in future require such high-performance CBiCMOS technologies, but it remains to be seen if the product volume can justify this enormous investment in process technology.

(B) BiCMOS on Silicon-on-Insulator Substrates

It became obvious in the previous sections that a large part of a BiCMOS process applies to the device isolation. Some of the technology elements, such as p^+/p^--epi substrates, deep trenches, and buried layers, are cost intensive and have to be assessed besides the mask count to get a realistic estimate of the total process cost. CMOS on silicon-on-insulator (SOI) substrates is gaining rapidly in interest because this type of CMOS technology is inherently free of latchup, has higher device speed and a steeper reverse-subthreshold slope, and it simplifies the processing. Consequently, SOI provides also an opportunity for BiCMOS process simplification. Some technologies simply replace the silicon substrate by SOI and maintain the vertical structure of the bipolar transistors [9], while others take advantage of the process simplification by fabricating both the CMOS and the bipolar devices in a thin SOI layer [23],[86]. The bipolar transistors are lateral transistors in the latter case, which, however, have a much higher performance than the parasitic lateral pnp's mentioned earlier due to the reduced parasitic capacitances on SOI. A 0.5 μm-CBiCMOS technology on SOI has been reported with f_T's of npn and pnp transistors of 14

GHz and 9 GHz respectively [23]. This type of technology is certainly very attractive for low-power applications, but the potential of increasing the bipolar device performance significantly beyond that is small due to the difficulty to form a thin lateral base. The power handling capability of the bipolar transistors is limited since the buried oxide of the SOI wafers has a three-times smaller thermal conductivity than silicon. It would be desirable to have SOI substrates with different SOI thicknesses on the wafer. Thin-SOI would be required for the CMOS while the SOI for the bipolar transistor should be thick and have a thermal path to the silicon to allow to fabricate a high-performance vertical bipolar device with high current drive. Such a SOI isolation structure has been developed and studied [87]. A combination of selective epitaxial growth (SEG) and chemical-mechanical polishing (CMP) was used to form full-SOI regions for the CMOS devices and partial-SOI regions for the bipolar transistors on the same wafer. Fig. 10 shows the isolation structure which can be described as divided into three sections, the Levels I through III as indicated in the figure. The n^+-subcollector of the bipolar transistor is formed with a reach-through contact over thick oxide in Level I. Compared to deep-trench isolation, there is no peripheral component of C_{CS} and the area component is reduced to a small region under the active device. C_{CS} is therefore only 30% of that achievable with deep trench isolation. An epi pedestal is formed in Level I on the CMOS side to obtain a planar wafer surface after device fabrication and prior to metallization. In Level II, the collector-base region is formed for the bipolar transistor while in parallel thin SOI is grown on the CMOS side [88]. The thin SOI regions on the bipolar side, adjacent to the collector window, allow for a very tight spacing between emitter and collector window edges, thus reducing C_{CB} to about 70% [89]. The emitter-base and the CMOS gate structures are fabricated in Level III. Besides the reduction of the parasitic capacitances and providing a parallel wafer surface after device fabrication, which is important to be able to apply multi-level interconnects, the structure provides another unique feature. The epi-seed layer under the bipolar transistor in Level I acts as a thermal path between the bipolar device and the substrate so that the device temperature in operation is significantly reduced [89]. The same structure could possibly be fabricated by a wafer-bonding technique [91]. In this way, any concerns about the crystalline quality of the SEG material could be circumvented, even though a high device yield for the SEG structure was demonstrated [87].

Another BiCMOS process using selective epitaxy, but with a somewhat different focus, is discussed in [92]. Partial SOI has also been utilized in a smart power BiCMOS process [93] to fabricate a VDMOS with wafer backside contact while all other devices were built on SOI. The Partial-SOI was formed here by high-dose implantation of oxygen (SIMOX) with use of a blocking mask.

(C) BiCMOS for RF&Microwave Single-Chip Solutions

The wireless communication market is believed to be one of the fastest growing businesses in electronics for the next years. Products are currently targeted for center frequencies of 900 MHz, 1.8 GHz, and 2.4 GHz. Conventional board designs with III-V, silicon-bipolar, and CMOS components are dominating the initial market, but they may be too expensive in the long term and may have difficulty to satisfy the large product volumes which are at the horizon. Single-chip solutions will therefore be very desirable. CMOS-only RF chips are expected to dominate the 900 MHz regime [94], but at the higher frequencies the RF functions will have to be designed with bipolar transistors. In that frequency range, BiCMOS will therefore be the ideal technology.

But the challenges in the development of integrated RF&Microwave systems are not only at the active device level. It is equally important to provide a set of passive components which can be integrated with the transistors to built matching sections, filters, oscillators, etc.. Several BiCMOS and bipolar technologies have been modified for that purpose, and most of them have tried to adopt these passive elements from the well-established III-V microwave technologies. A good example is the realization of an integrated inductance. In III-V processes spiral inductors are commonly used, but with a direct transfer of these inductor structures to silicon the quality-factor (Q) would be very limited because of the higher resistivity and smaller thickness of the AlCu interconnects and due to the lossy silicon substrate. Therefore, for example, AT&T developed a Au two-level interconnect technology for their existing BiCMOS process and replaced the standard 10-20 ohm-cm bulk material with high-resistivity silicon (HRS) substrates [95]. Similar modifications of interconnect technology have been published [96]-[98]. A different approach takes advantage of the fact that multi-level interconnects are a standard in todays advanced BiCMOS technologies [12],[17],[24],[23],[36]. It is possible to overcome the thickness limitation of small-pitch AlCu wires by shunting several metal levels together. The substrate losses in typical 10-20 ohm-cm silicon can be reduced by building the inductor spiral in the upper metal levels to increase the spacing between inductor spiral and the lossy substrates [99],[100]. The cross-section in Fig.11 illustrates a spiral inductor fabricated with five levels of interconnects. The metal layers M3, M4, and M5 had been shunted together to increase the thickness of the conductor, M2 was used as an underpass, and M1 was left out to increase the distance from the substrate. With this type of inductor implementation, Q-factors between 11.5 (5.1 nH) and 24 (1.45 nH) could be demonstrated without any deviation from standard silicon process technology [101],[102]. These values are equal or better than the results achieved by using the modified silicon technologies.

Besides the described inductor implementation, also other important RF&Microwave components

were already successfully integrated in BiCMOS technology, such as transformers, metal-insulator-metal (MIM) capacitors, and varactors, again without changing the conventional process flow [101],[102]. Some of these devices were used in circuit demonstrations. Multi-level inductors have been used in matching sections of a power amplifier [101], an inductor and a varactor were integrated in a CMOS-VCO [103], and transformers have been used in low-noise amplifiers [104].

These developments of new integrated high-performance devices in standard BiCMOS technology without any changes of the existing process underline once more our argument we made about the structural convergence of the design requirements as the technology is scaled towards smaller dimensions. The few new directions which were sketched here show that BiCMOS technology development is not strictly following the device scaling principles, but it is an art in itself to tailor a BiCMOS process also for a minimum complexity and a maximum versatility.

5. Summary and Conclusions

BiCMOS integration processes have developed in a similar way than CMOS or bipolar technologies: the process complexity, i.e. the number of mask levels and process steps, has increased steadily with device scaling. The average BiCMOS process has a 30-35% higher mask count than the core CMOS, but the differences of BiCMOS processes can be significant. Compromised, CMOS-based processes with utilization of special fabrication steps can have masks counts equal or smaller of than of conventional CMOS, while for optimum device performance and additional device functions a much higher investment is required. Though complex, high-performance submicron BiCMOS has the advantage that the structural requirements for the CMOS and bipolar transistor tend to converge with miniaturization, and modular integration concepts can be more easily implemented compared to earlier BiCMOS generations.

New fabrication concepts, such as BiCMOS on SOI, have the potential of providing even higher performance at a reduced process complexity and cost. High-performance BiCMOS seems to be particularly interesting for the fast evolving wireless and broadband communication markets. Consequently, the speed of the bipolar transistor in BiCMOS will have to be further increased by pursuing new concepts in device self-alignment and by exploiting Si and SiGe base formation. In portable communication circuits and systems BiCMOS on SOI substrates is a promising technology to achieve the required speed at low power. Special microwave functions will have to be added to the BiCMOS processes for wireless systems, but many of them can be derived

from the existing versatile fabrication processes. Smart power BiCMOS technologies for the automotive industry are on the rise, and also here the versatility of BiCMOS fabrication concepts will allow to obtain the desired power device function from existing fabrication processes.

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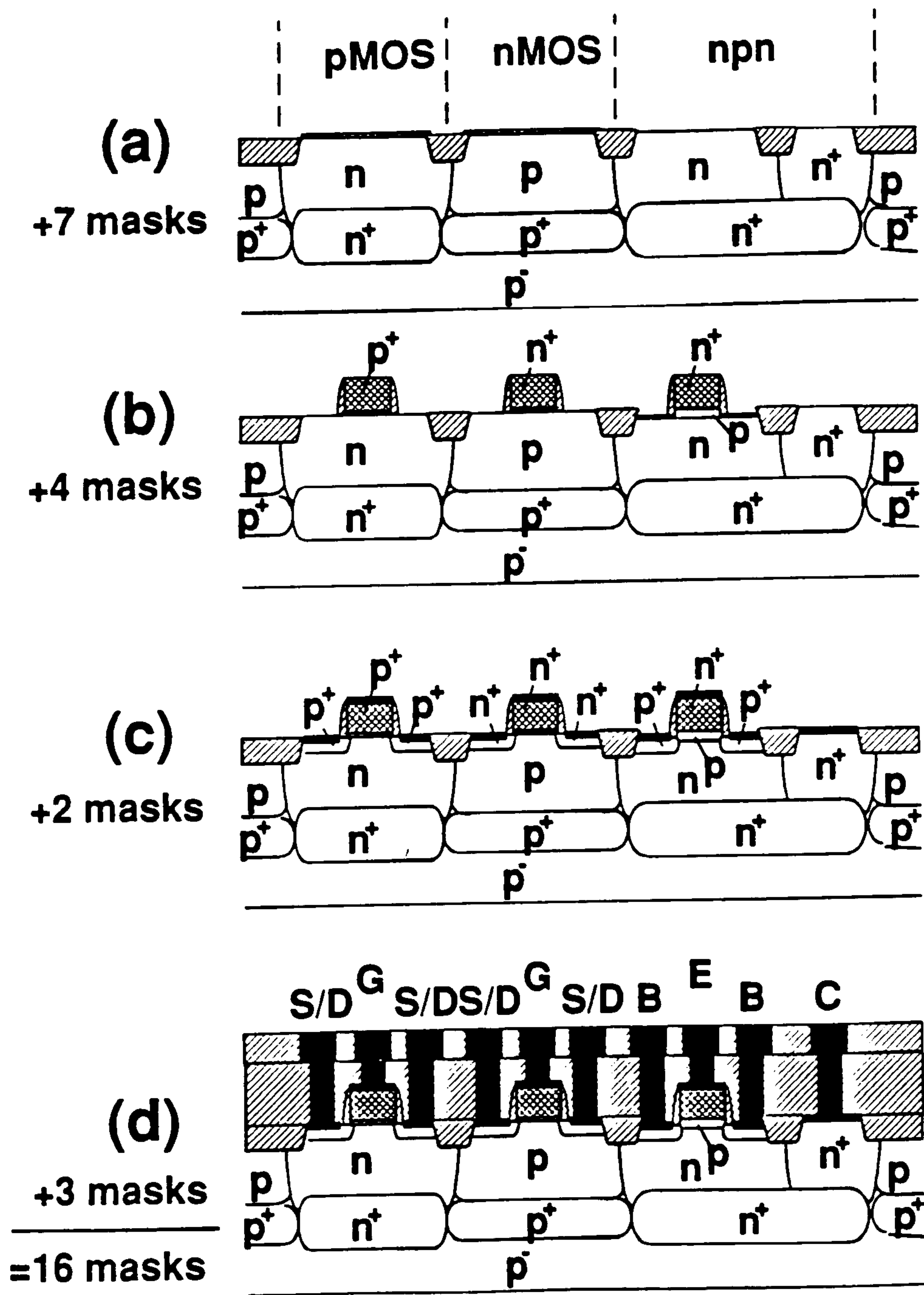

Fig. 1 Fabrication process flow of an exemplary BiCMOS technology with twin-well, dual work function CMOS and an outside spacer bipolar transistor.

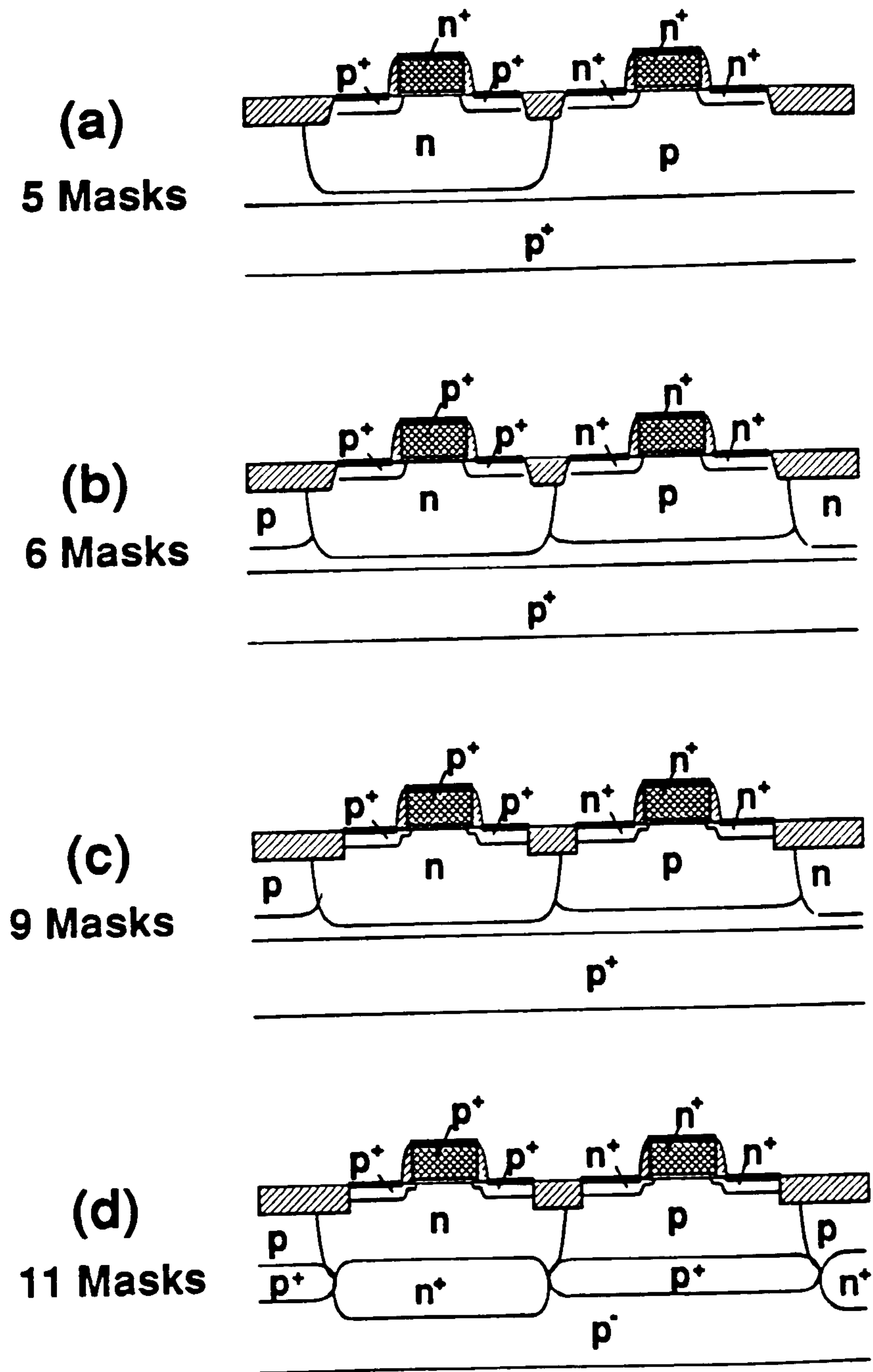

Fig. 2 CMOS process options for different channel lengths with the associated mask count for the illustrated parts of the processes. Processes (c) and (d) illustrate the transition from core CMOS to BiCMOS-integrated CMOS.

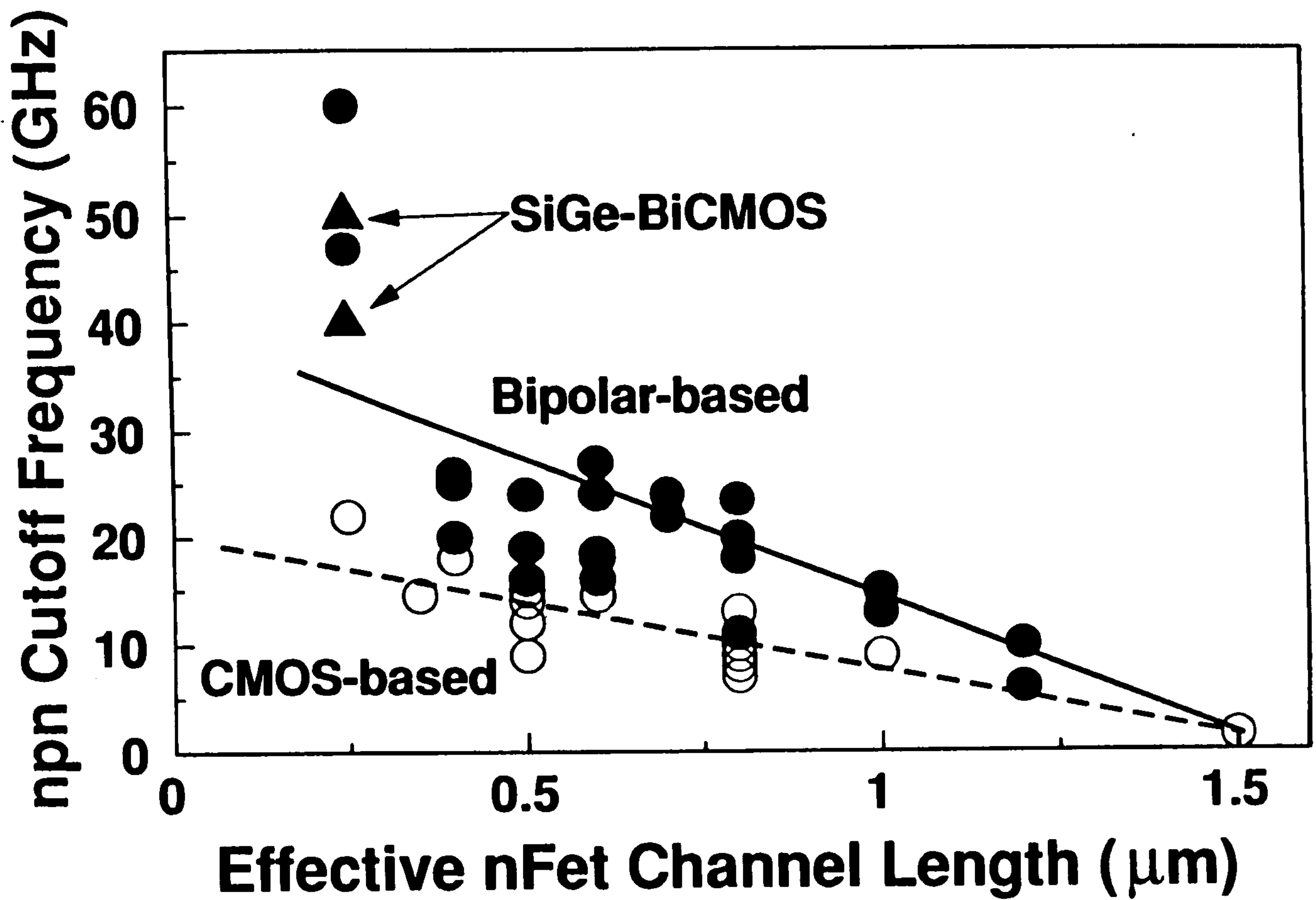

Fig. 3 Cutoff-frequencies of the npn transistor drawn versus the effective channel length of the nFet with data from references [4]-[44]. Part of the data is listed in Table 1. Solid circles represent BiCMOS processes which were designed with equal emphasis on CMOS and bipolar devices, while the open circles stand for bipolar transistors added to a core CMOS technology. The solid triangles are from IBM's SiGe-BiCMOS technology [15],[16].

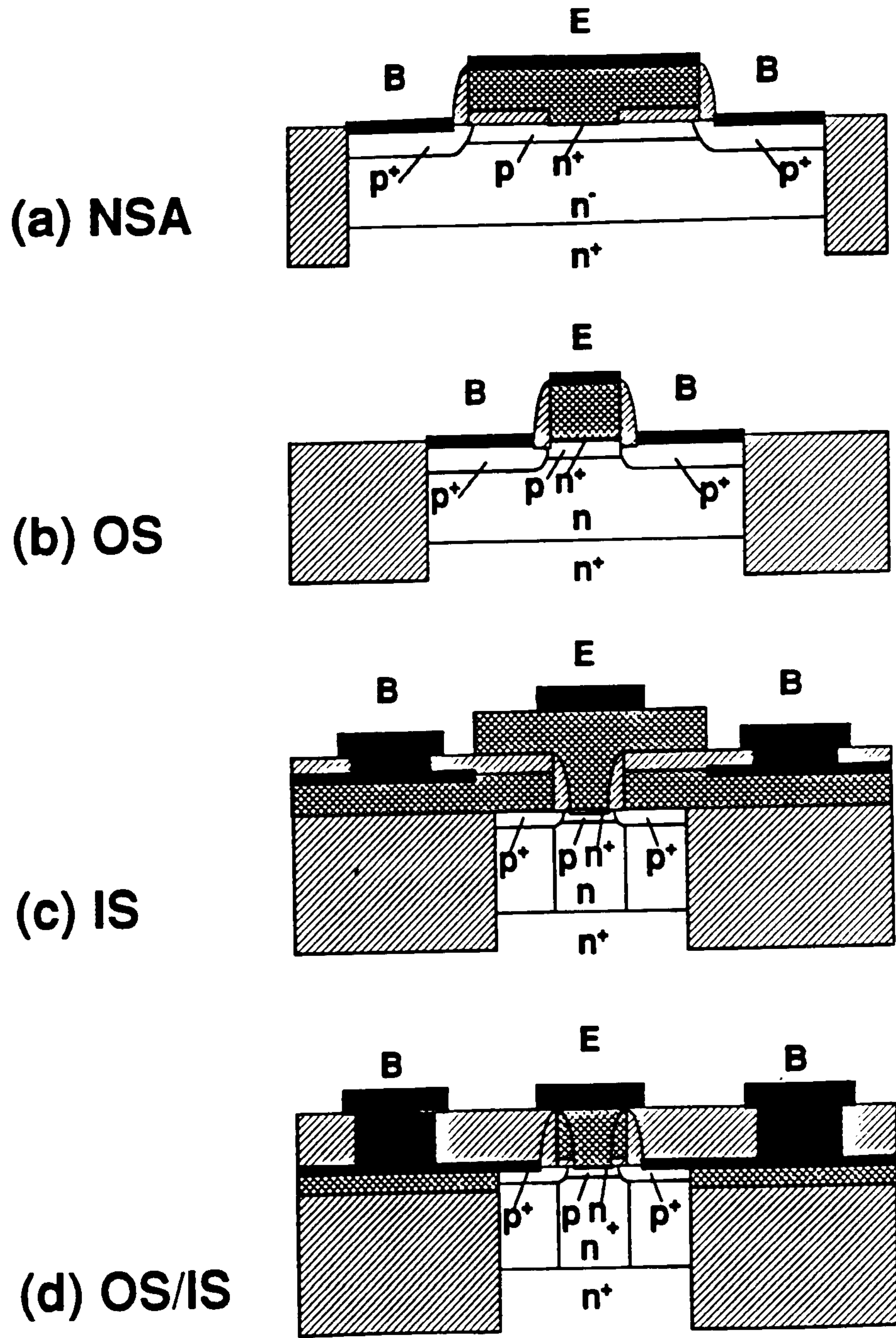

Fig. 4 Cross-sectional sketches of the emitter-base regions different structures for bipolar transistor integration (collector contact not shown). The non-self-aligned (NSA) structure in (a), the outside-spacer device (OS) in (b), the inside-spacer transistor (IS) in (c), and the novel structure in (d) are compared. The self-aligned integration scheme in (d) combines the benefits from both the OS and the IS devices.

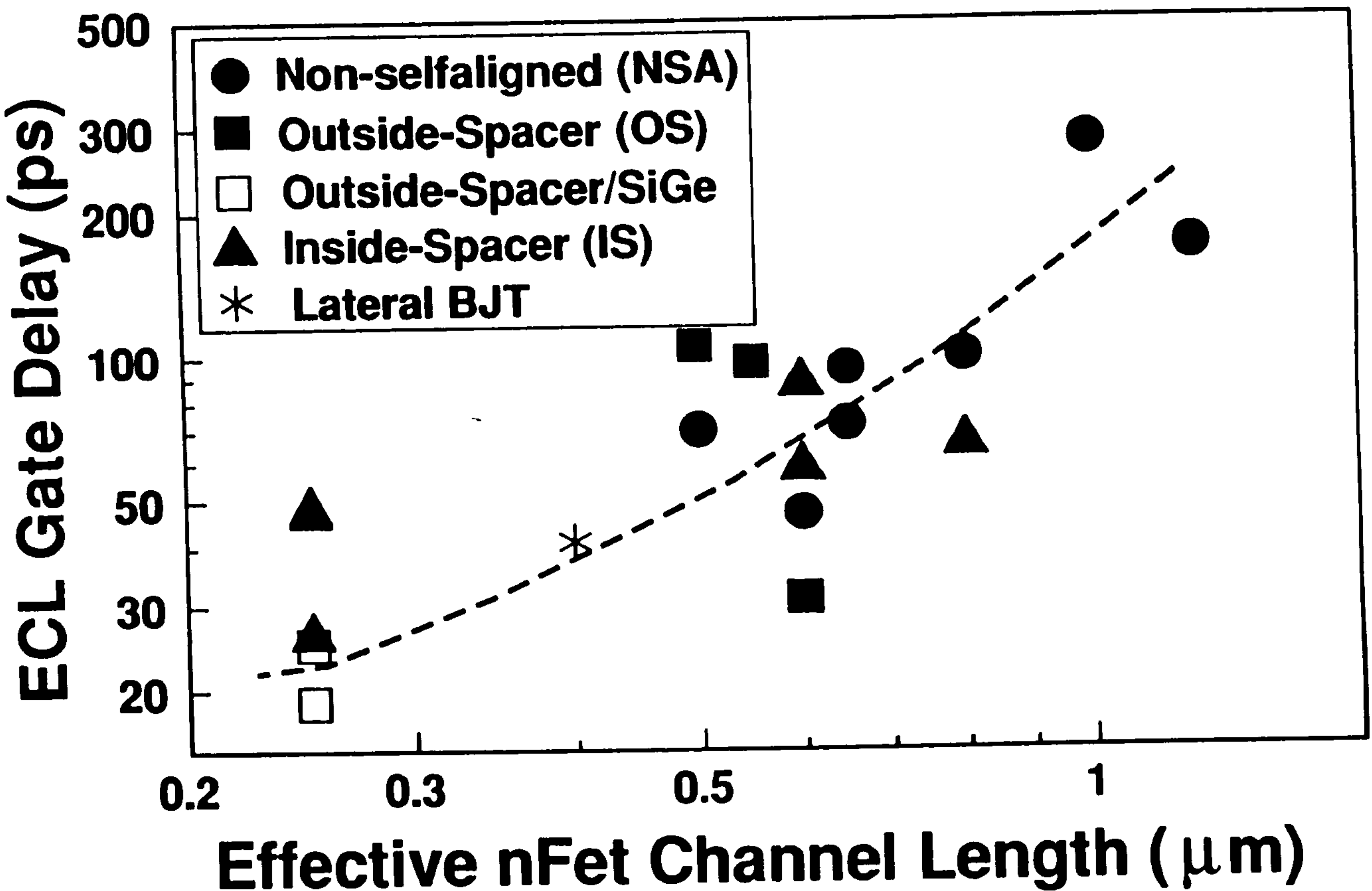

Fig. 5 ECL gate delay for ring oscillators fabricated in a BiCMOS process as a function of the nFet channel length. The symbols differentiate the self-aligned structures used for bipolar transistor integration.

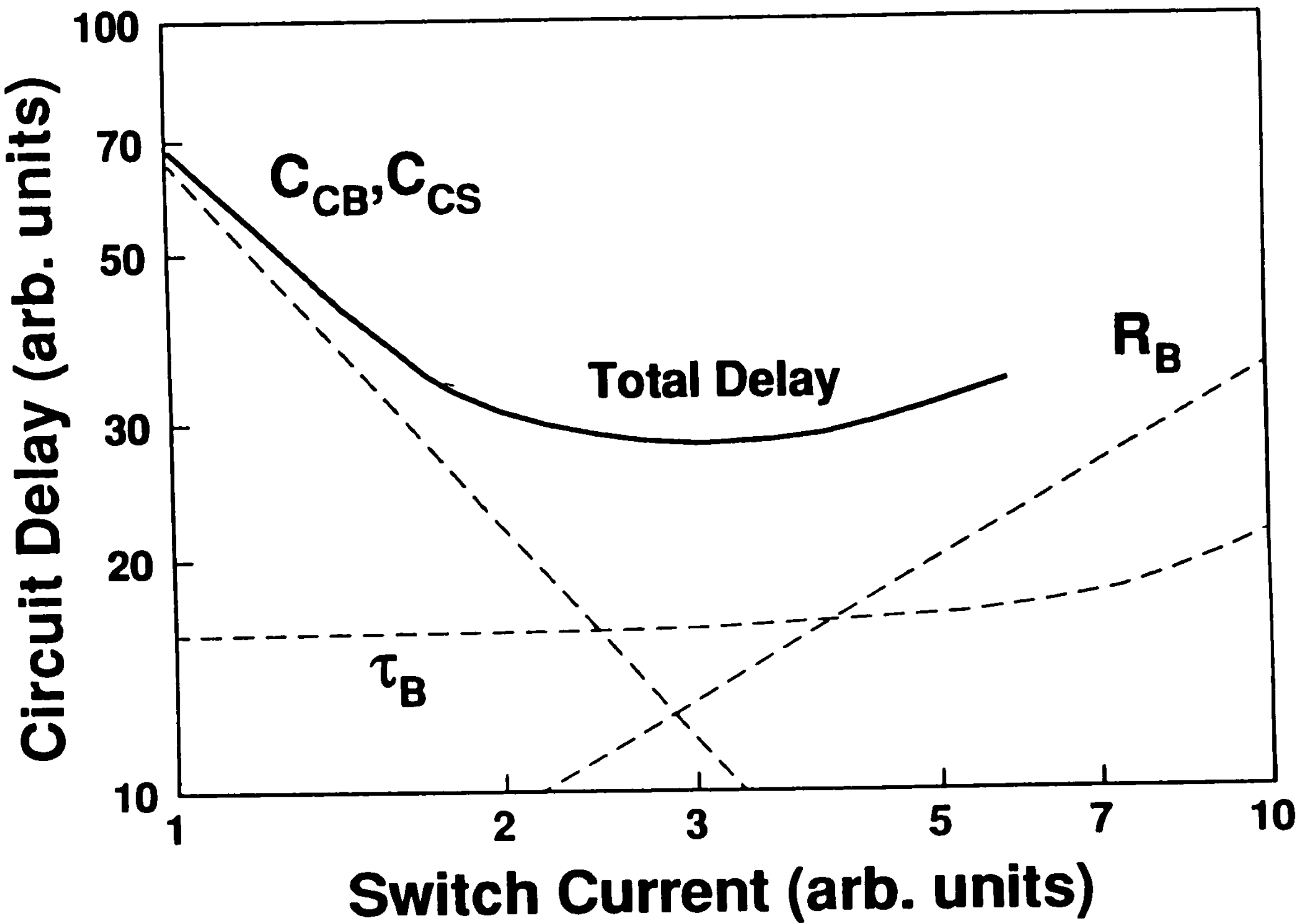

Fig. 6 Qualitative dependence of the ECL gate delay on the switch current. At small current the performance is mainly limited by the device capacitances, while at high power the base resistance dominates. In the vicinity of minimum gate delay the device performance is gated by the base transit time (τ_B) which is the dominant component of f_T [58].

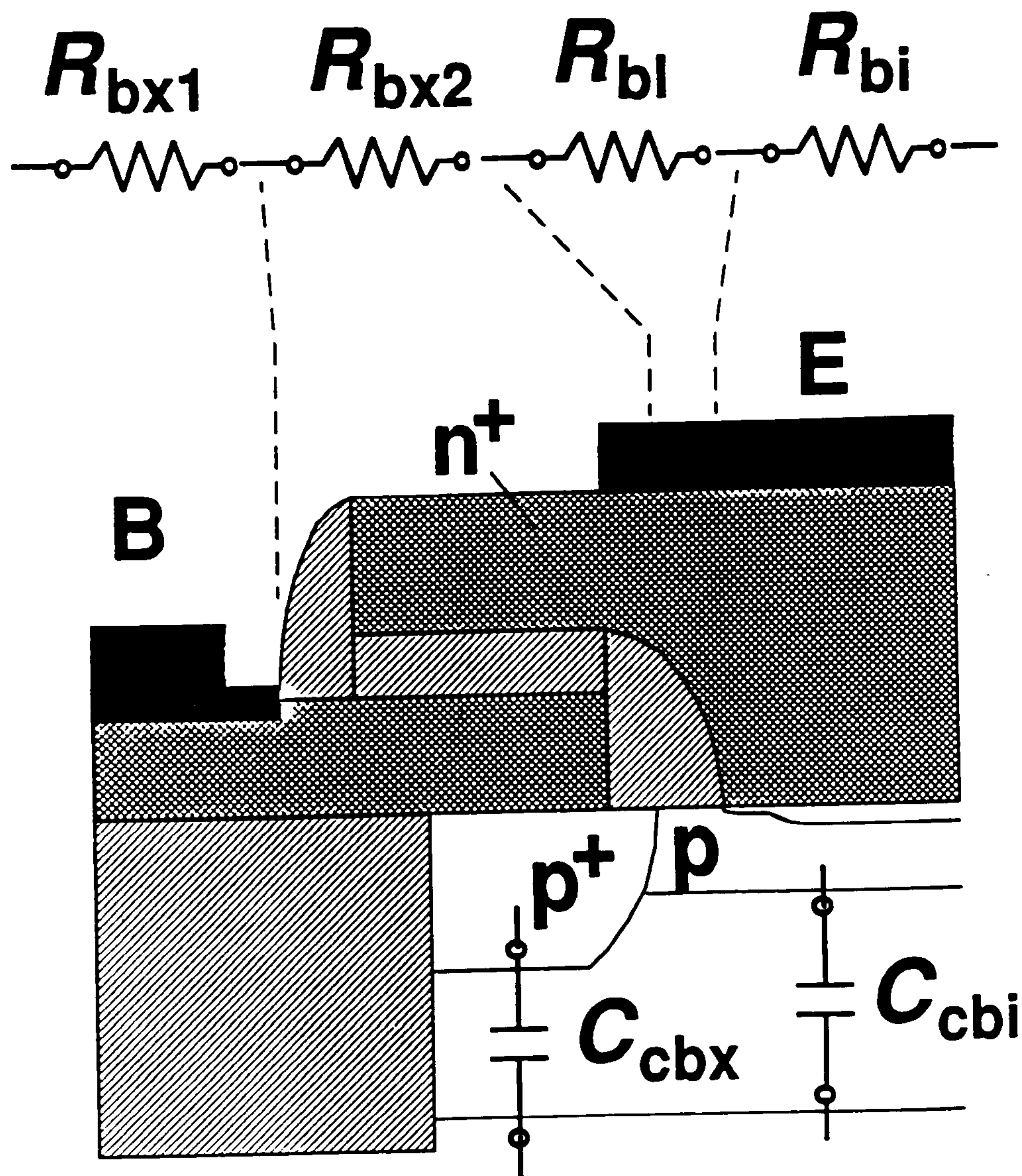

Fig. 7 Cross-sectional view of the left emitter edge of the IS device structure. The partial resistances and capacitances of the base resistance (R_B) and the collector-base capacitance (C_{CB}) are illustrated. R_B consists of the intrinsic base resistance (R_{bi}), the base link resistance (R_{bl}), the silicided part of the extrinsic base (R_{bx1}), and the polycrystalline part of the extrinsic base which is protected from silicidation by the emitter-polysilicon (R_{bx2}). C_{CB} separates into the intrinsic capacitance (C_{cbi}) and the extrinsic capacitance (C_{cbx}).

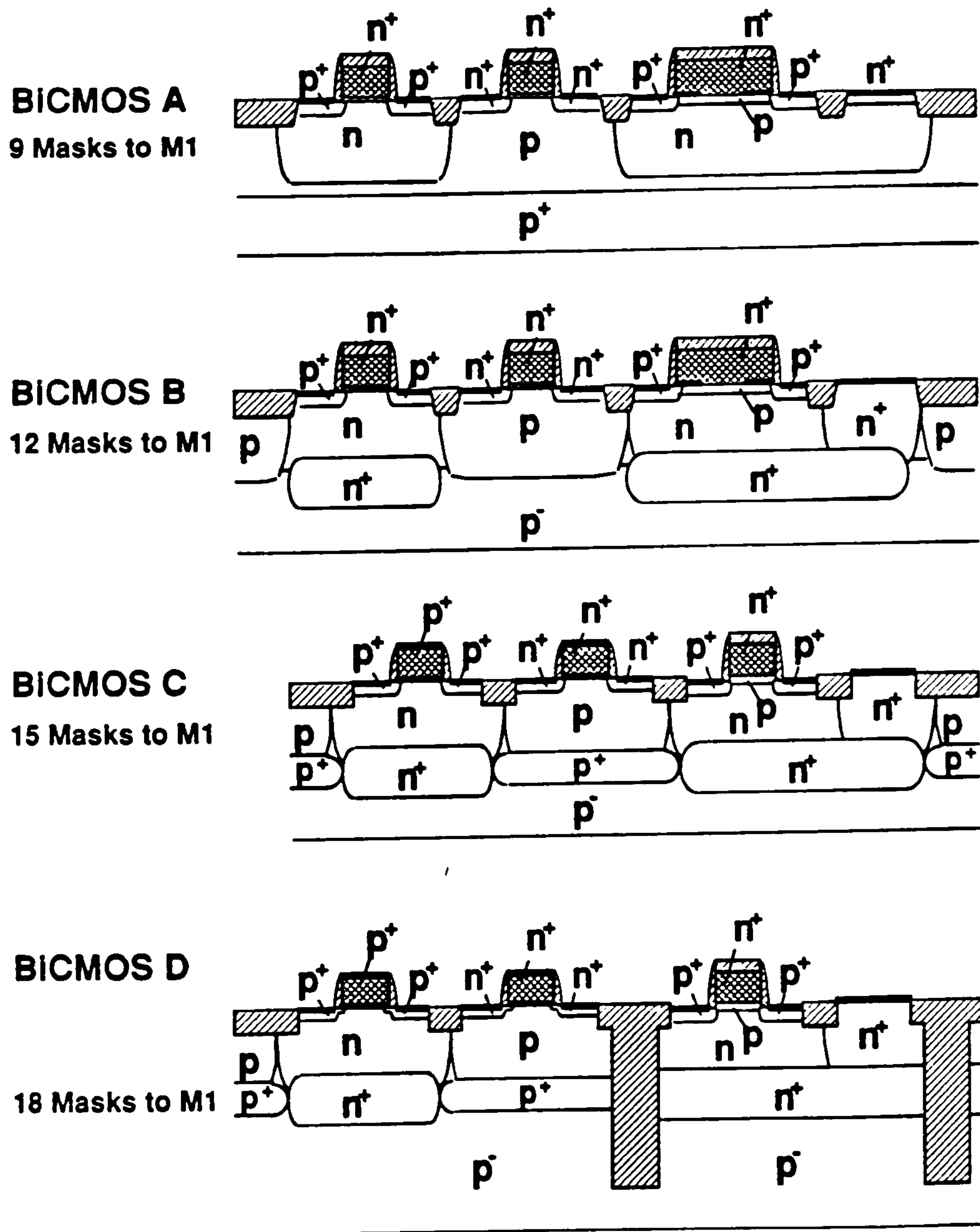

Fig.8 Cross-sections of four generic BiCMOS structures with different complexity levels (not drawn to scale). The mask count considers a single mask for all contacts.

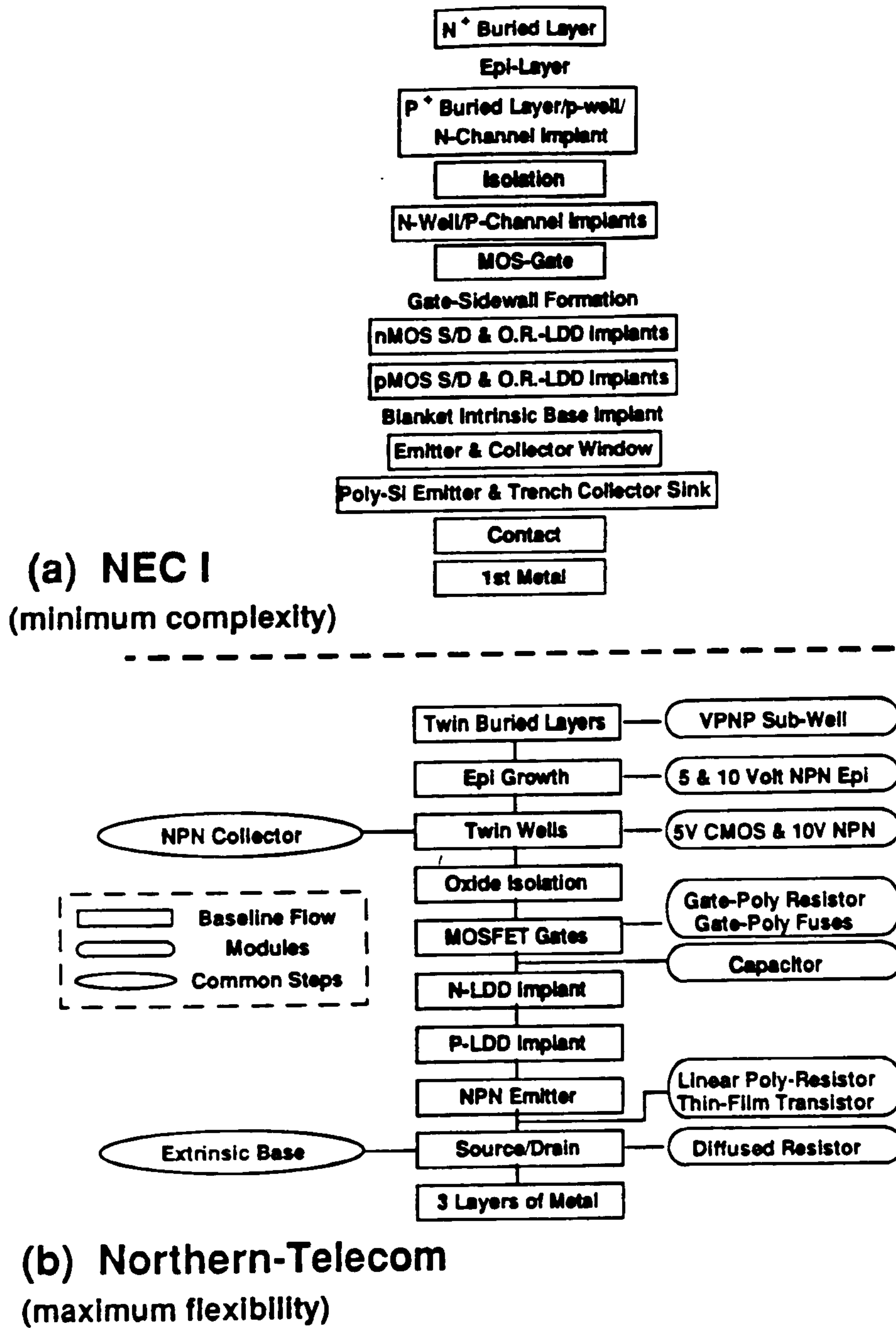

Fig. 9 Examples of a 0.35 μm BiCMOS process designed for minimum mask count (a) [26], and of a complex BiCMOS process which has a modular concept to add flexibility and obtain maximum efficiency for a certain application [30].

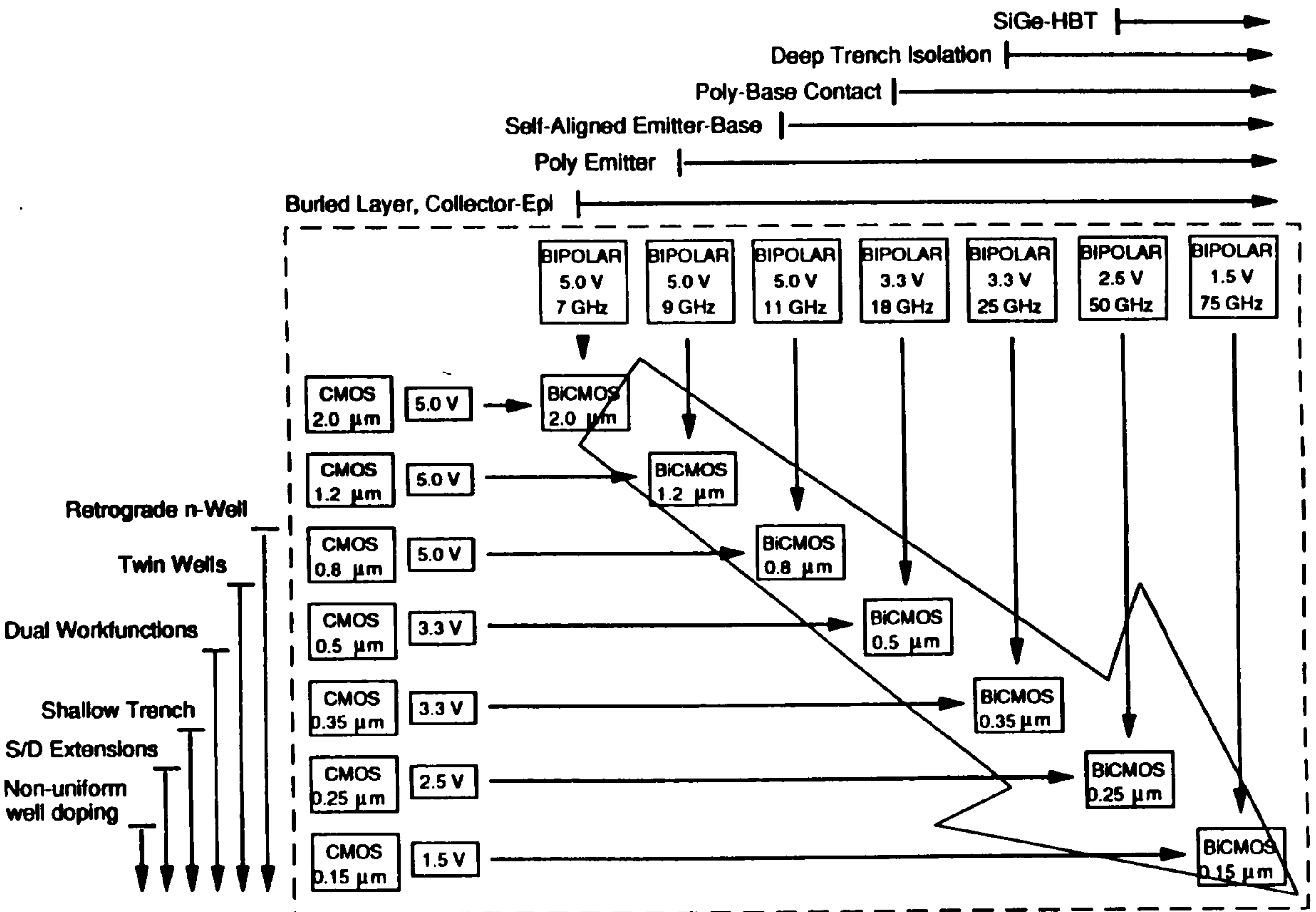

Fig.10 BiCMOS generations from 1.2 µm to 0.15 µm (projected) with required CMOS and bipolar device parameters. Significant changes for CMOS and bipolar integration technology are indicated at development stages where they are likely to become indispensable.

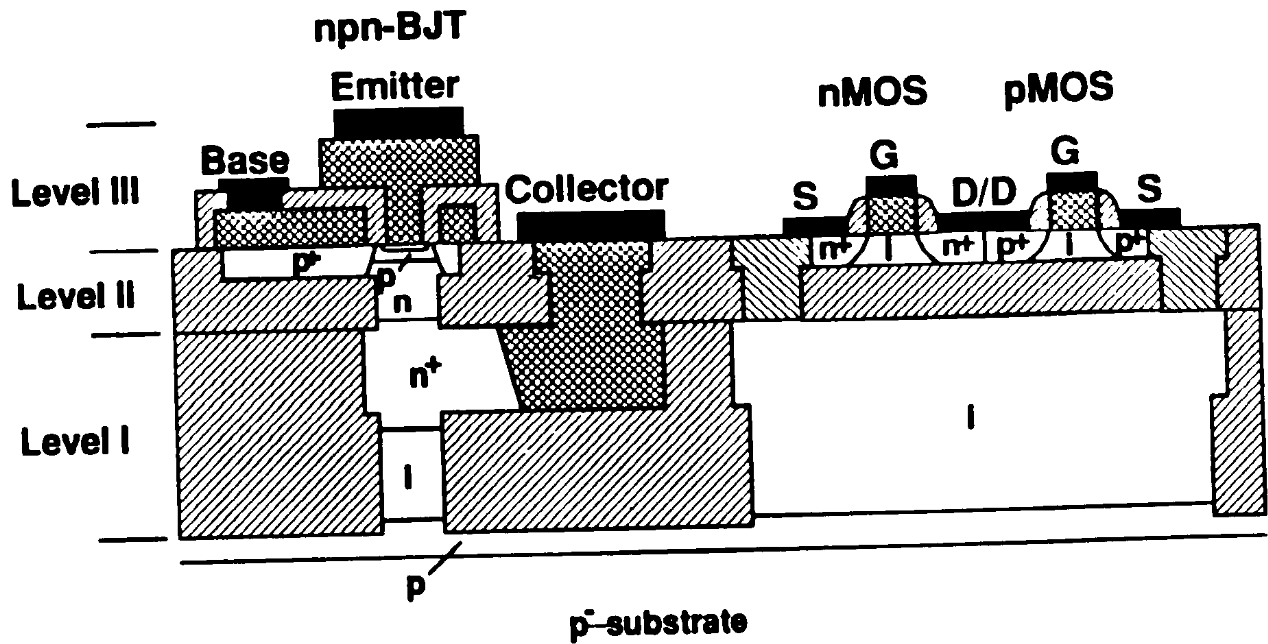

Fig.11 SOI-BiCMOS device isolation structure (pFet not shown), [86]. Selective Epitaxial Growth (SEG) and Chemical-Mechanical Polishing (CMP) were used in the fabrication process. Thin SOI for the CMOS devices and thick, partial SOI with a thermal path to the substrate for the bipolar transistors could be realized on the same wafer while preserving the wafer surface planarity.

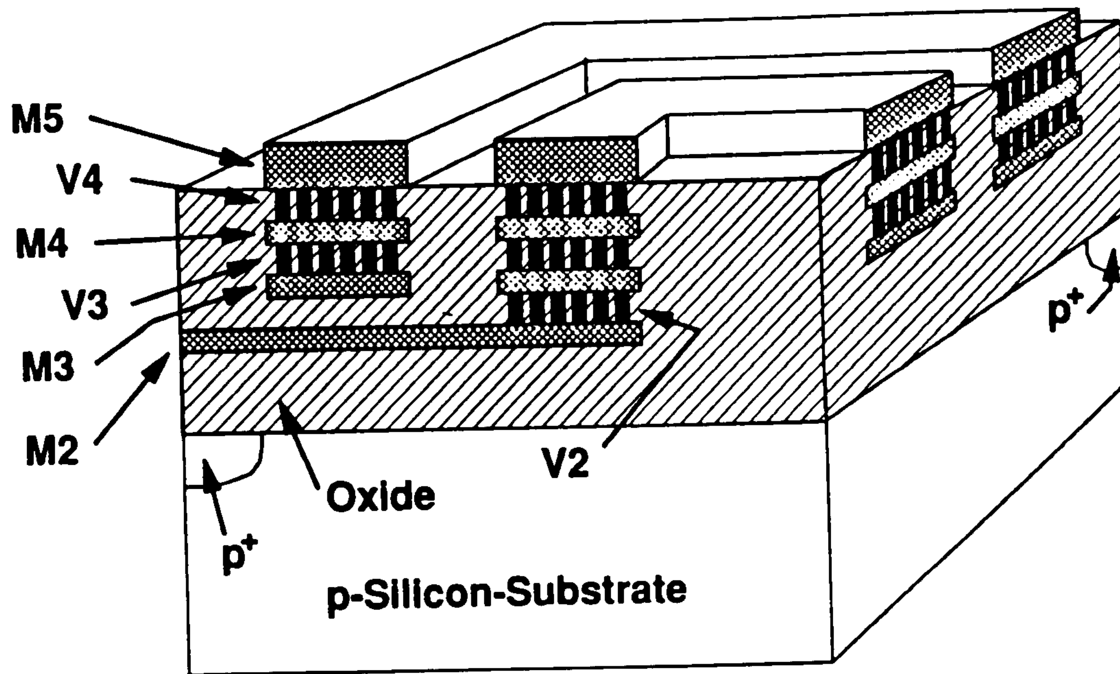

Fig.12 Cross-section of the center part of a spiral inductor fabricated in multi-level AlCu interconnects technology. The metal layers M3, M4, and M5 are shunted together by dense via arrays to achieve an effectively thicker conductor M2 served as an underpass, and the M1 was left out to increase the spacing between inductor spiral and substrate and thus reduce substrate losses.

Company	Year	Application(s)	CMOS-L_{eff}	BJT-f_T	BJT-Type	Specialties	Met.-Lev.	Masks
AT&T	1995	Mixed Signal	0.6 μm	24 GHz	OS	SEG,Planariz.	3	21
Cypress	1991	Logic/SRAM	0.8 μm	10 GHz	OS		2	
Fujitsu	1988	SRAM	1.2 μm	6 GHz	IS		2	
Hitachi I	1989	SRAM	0.8 μm	11 GHz	IS		3	
Hitachi II	1992	Logic/μP	0.6 μm	27 GHz	IS	SOI	2	
HP	1992	Logic/SRAM	0.5 μm	16 GHz	NSA		2-4	17-21
IBM Ia	1990	Logic/SRAM	0.45 μm	15 GHz	NSA		2	8 to M1
IBM Ib	1993	Mixed Signal	0.45 μm	12 GHz	NSA	Analog Passives	3-5	
IBM II	1992	Logic	0.25 μm	47/60 GHz	IS		2	
IBM IIIa	1992	Logic	0.25 μm	50 GHz	OS	SiGe-HBT	3	
IBM IIIb	1995	Mixed Signal	0.25 μm	40 GHz	OS	SiGe-HBT	3	
Intel	1995	μP (Pentium)	0.6 μm	18 GHz		Shallow Trench	4	
Mitsubishi I	1992	SRAM	0.6 μm	18.5 GHz	IS		2	
Mitsubishi II	1994	Mixed Signal	0.8 μm	20 GHz	IS	4 GHz pnp		
Motorola I	1995	SRAM	0.4 μm	15 GHz	IS	TFT, pnp	2	27
Motorola IIa	1991	Logic/μP	0.5 μm	26 GHz	NSA	4 GHz pnp	4	
Motorola IIb	1993	Smart Power	0.5 μm	26 GHz	NSA	LCMOS,LIGBT	2	
Motorola III	1994	SRAM	0.5 μm	14 GHz	Lat.-BJT	SOI, pnp	2	
National I	1989	SRAM	0.6 μm	15 GHz	NSA		4	
National II	1989	Logic/Analog	0.5 μm	9 GHz	OS		1	
NEC I	1994	Mixed Signal	0.35 μm	14.5 GHz	NSA	W-plug	1	11
NEC II	1992	SRAM	0.5 μm	15 GHz	IS	FT, 4-poly		
Northern Tel.	1991	Mixed Signal	0.65 μm	11 GHz	NSA	Analog Passives	3	19-27
NTT	1992	Logic/μP	0.25 μm	22 GHz	IS	SIC	2	
Philips I	1989	Logic	0.8 μm	13 GHz	OS			
Philips II	1990	Logic	0.55 μm	18 GHz	OS		3	
Siemens I	1989	Logic	1.2 μm	10 GHz	IS		2	
Siemens II	1991	Logic	0.8 μm	23.5 GHz	IS		3	
Tektronix	1988	Logic/Mixed	0.8 μm	16 GHz	IS	Au-Interconnects	2	18
Temic	1992	Mixed Signal	0.8 μm	8 GHz	OS	pnp	2	
TI	1987	SRAM	0.8 μm	7 GHz	OS	Deep Trench	2	
Toshiba I	1983	Logic/SRAM	1.0 μm		NSA		1	
Toshiba II	1990	Mixed Signal	0.5 μm	12 GHz	IS	TFT, 5 GHz pnp	2	

Table 1 BiCMOS integration processes selected by company names, publication dates, and target applications. The processes are characterized by the effective channel length (L_{eff}) of the CMOS, the cutoff-frequency (f_T) of the bipolar transistor, the type of lateral emitter-base structure (OS = outside spacer, IS = inside spacer, NSA = non-self-aligned), the distinct specialties of the processes, the number of interconnect levels, and in some cases the total mask count.