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Research Report

Copper Interconnect: Fabrication and Reliability

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Abstract

The materials, processes, and reliability issues in the development of multi-level Cu chip interconnections are described. Prototype four-level Cu/polyimide structures have been fabricated by using a damascene process which maintains planarity at each level. Electromigration lifetime for two-level Cu interconnections is found to be longer than that of Al(Cu) while having approximately twice the conductivity.

Introduction

It is generally recognized that, as the features of integrated circuitry (IC) chips are scaled to submicron dimensions, on-chip interconnections face increasing technical demands. Scaling of active devices leads to increasing speed, while the delay due to interconnections either remains constant or increases. Consequently, both high conductivity wiring and low dielectric constant insulators, such as Cu, polyimide (PI), offer major performance gains [1]. In addition, higher operation frequencies for IC chips lead to higher current densities in increasingly smaller features of interconnections. As a result, a highly reliable wiring for allowing high current density is required. Cu is the obvious choice for a new advanced interconnection metallization based both on its desirable high conductivity and the fact that it is relatively easy to obtain a clean interface with Cu, which greatly reduces contact resistance between metal levels. Significant progress has been made in the past few years in developing processing techniques for multilevel copper interconnection systems in advanced microelectronics [2-4]. Successful demonstrations of fully integrated 4-level copper interconnection systems have recently been reported [2]. In this paper, we describe the materials, processes, and electromigration reliability issues related to the development of multi-level Cu wiring structures incorporating full passivation and containment of both the Cu and polyimide. Finally, a comparison of the experimental results between two interconnection metallizations Al(Cu) and Cu is also presented.

Properties of copper

A. Copper Resistivity

The low resistivity of copper (1.7 μΩ-cm at 22 °C) is its prime advantage in replacing aluminum alloys for on-chip interconnections. The resistivity of Cu is increased from its residual low temperature value by electron scattering from phonons, impurities, vacancies, dislocations, grain boundaries, precipitated second phase particles and compound phases. For pure bulk Cu, the temperature coefficient of resistivity (TCR) near 20°C is 0.43%/°C [5], and a typical resistivity of an as-deposited Cu thin film line is 1.9 μΩ-cm with a TCR of about 0.36%/°C, so that a temperature increase of 10-20 °C raises the resistivity by about 0.1 μΩcm, a 5% increase. This factor should be considered in the thermal design of a chip, but is not one which we can modify directly. In copper, the electron mean free path is about 0.03 μm at 20 °C [6], which is less than the grain size and linewidth in thin film lines, and therefore will not limit resistivity until the dimensions are significantly below 0.1 μm. Similarly, surface scattering is usually ignored, but dimensions are entering the regime where this term will eventually contribute to the line resistance. If copper contains impurities, the dominant contribution to increased resistivity is solute scattering. The resistivity of copper rises rapidly with increasing concentration of most solutes and is summarized [7]. For dilute impurity concentrations, most solutes raise the resistivity of Cu by more than 1.0 μΩ-cm per atomic percent, but only if these elements are in solution. Many metals have low solubility in Cu [8], and therefore may be caused to segregate to surfaces, grain boundaries, or internal interfaces. This segregation can decrease the resistivity to values close to that of pure Cu.

The resistivities of pure Al (2.7 μΩ-cm) and Cu (1.7 μΩ-cm) are actually not obtained in interconnections, since Al is alloyed with copper to increase its resistance to electromigration and stress-induced migration. A typical resistivity, for Al-0.5 wt.% Cu, is 3.0-3.2 μΩ-cm. Also, state-of-the-art aluminum interconnections are sandwiched between layers of Ti or TiN to further increase their reliability, reduce contact resistance, and for photo-resist lithographic process, but these layers sacrifice a significant fraction of the cross-sectional area. The effective resistivity, based on the full cross-sectional area of the wiring structure, can easily be estimated and compared for these two systems. For the Al(Cu)-based system, a structure of Ti(10nm)/TiN(10nm)/Al(Cu)(300nm)/Ti(10nm)/TiN(40nm) would increase the effective resistivity to 4.1 μΩ-cm, because of the high resistivity of Ti and TiN, and the formation

of $TiAl_3$ at the Al(Cu)/Ti interface. For the Cu-based system, the thickness of liners (e.g. Ta) has to be low to achieve the enhanced conductivity intrinsic to Cu metallization. Unlike the Ti/Al system, no reaction between Ta/Cu was found even when a Ta/Cu/Ta trilayer film was annealed at 600 °C for 1 hour, because there are no Cu-Ta compounds and the solubility of Ta in Cu is extremely low. To assess the effect of different thicknesses of the Ta liner, one can use a calculation which employs two parallel resistors (Cu and Ta liner), with the assumption that the thicknesses of liner on the bottom and the sidewall are equivalent. The effective resistivity of the Cu damascene line of ≤ 2.4 $\mu\Omega$-cm is estimated, if the ratio of liner thickness to Cu thickness is ≤ 0.1 [9].

B. Copper Microstructure

The grain size distribution of as-deposited Cu films is usually not log-normal [10], and often contains a bimodal distribution indicating that some abnormal grain growth occurs during the deposition process [11]. Heating to 400 °C causes the small grains to grow first, followed by the larger grains at a higher temperature. Fig. 1 shows a focused ion beam micrograph of 1.8 μm wide and 1.0 μm thick CVD Cu lines after annealing at 400 °C for 1 hour. The metal lines were formed by a damascene technique [12] which will be discussed in a later section. A mixture of large and small grain sizes (bimodal distribution), and twins were seen in the Cu lines.

Fig. 1. Focused ion beam micrograph showing the grain structure of the CVD Cu lines.

Contaminants or second-phase materials may strongly influence this grain growth process. For example, the impurities of Mg and Sn retard Cu grain growth, while in dilute Cu-Co alloys (several atomic % Co) a dramatic abnormal grain growth process has been found to occur at a low temperature (200 °C), in which many grains increase in size to more than 10 times the film thickness [13]. Fig. 2 shows a TEM micrograph of a 1 μm thick electro-plated Cu (0.7 at.% Co) film after annealing to 450 °C for 30 min, in which a single (200)-oriented grain larger than 20 μm diameter is shown, containing numerous orthogonal twins. This is in contrast to normal grain growth, for which the grain size typically saturates at grain sizes of 2-3 times the film thickness. Interestingly, the large grains in Cu-Co have a strong (200) texture, again in contrast to other reported Cu textures, which are typically a mixture of (111) and (200) [10]. In aluminum alloy films, the typical texture evolution on heating is towards a very strong (111) texture [14], with some exceptions reported [15]. Abnormal grain growth has also been observed in Al alloy films with layered structures [16].

Properties of Interlevel Insulators

A. Dielectric Properties of Interlevel Insulators

The need to reduce the capacitance of interconnection structures in addition to their resistance has stimulated activity to identify low dielectric constant insulators with suitable properties for integration with Cu [1]. The dielectric constant must be substantially lower than that of amorphous SiO_2 (ε = 3.9-4.1), which is the current industry standard. During the development of Cu/polyimide (PI) structures, it was shown that the dielectric constant of BPDA-PDA is highly anisotropic, with $\varepsilon = 2.9$ out-of-plane and $\varepsilon = 3.7$ in-plane [17] Other low-ε polymers being considered include: fluorinated polyimides (ε = 2.5-3.3) [18]; poly(tetrafluoro-p-xylylene) (parylene) ($\varepsilon \approx 2.3$ isotropic) [19]: PTFE ($\varepsilon \approx 2.0$) [20]; benzocyclobutenes ($\varepsilon \approx 2.7$) [21]; Si-containing polymers (ε = 2.8-3.7) [17]; and polyimide foams ($\varepsilon \approx$ 2.0-2.3) [22]. Inorganic insulators being considered for integration with copper include: BN ($\varepsilon \approx 4.0$) [23]; silsesquioxanes ($\varepsilon \approx 2.9$) [24]; and fluorinated silicon oxide ($\varepsilon \approx 3.5$) [25]. For some of these materials, their thermal stability is questionable, and their mechanical integrity needs to be examined when thermally cycled together with copper. Thermomechanical simulations would be helpful if the detailed elastic and inelastic constitutive relationships for most of these materials, especially in thin film form, were available.

B. Mechanical Properties of Interlevel Insulators

In the search for low dielectric constant insulators, one must often make a tradeoff between dielectric constant and thermal stability. Low values of dielectric constant ($\varepsilon < 2.5$) are primarily found among organic insulators, with few materials demonstrating stability against thermal decomposition above 400 °C. The highest temperature reached during interconnection fabrication is determined by steps including curing the interlevel insulator and final passivation, wirebonding and attaching the chip to a package. At present

Fig. 2 Plain-View TEM micrograph of 1 Cu (0.7 at.% Co) thin film after annealing to 450 °C for 30 min.

it is necessary to require 350-400 °C thermal stability for the interlevel insulator.

A suitable material should not possess any phase transitions which result in significant lowering of the elastic modulus. The insulator must not evolve volatile components or degrade in mechanical properties after multiple temperature excursions. If the fracture toughness is reduced, stress-induced cracking may result. In fabricating multilevel structures, the first level insulator may experience as many as 10-15 cycles to the temperature of metal deposition or insulator curing. The consequences of exceeding the glass transition temperature or melting point are decreased modulus and yield stress. When the metal interconnection lines have high residual stress levels, the resulting deformations of the insulator can be catastrophic, especially when adhesion is poor. Outgassing, from thermally induced decomposition, can have several adverse effects such as blistering, void formation and increased resistivity of the metal [26]. High resistance Al-Cu studs have been observed in metal filling of vias in organic insulators [27], as a result of gases exiting the via during metal deposition. A serious disadvantage of Al-based metallization with CVD W or reflowed Al studs is the high processing temperatures. Using a low temperature Cu deposition process with high aspect ratio filling capability allows the consideration of insulators with lower thermal stability, which greatly increases the range of insulator choices.

Barrier/adhesion layers

To incorporate Cu wiring into VLSI structures, it is necessary to include diffusion barrier layers to prevent Cu penetration into the underlying devices [28]. It is essential to prevent copper from entering the device silicon and forming deep level traps, or from diffusing into the insulator between Cu lines under the electric fields encountered during operation [29]. In addition, Cu reacts readily with Si at temperatures as low as 200 °C to form Cu_3Si [30,31]. Surprisingly, this compound catalyzes the oxidation of Si at room temperature, resulting in rapid growth of a layer of SiO_2 up to micrometers in thickness [30,31]. The need for a robust diffusion barrier between Cu and Si was recognized early [32], and several promising materials have been developed, including W, WN, Ta, Nb, TaN, TiN and TaSiN. A review of barrier materials has recently been published [28]. Although several excellent diffusion barrier layers have been demonstrated, in reality a thin, perfect, barrier layer in high density contact hole areas is seldom achievable. For this reason, the contact level stud to Si devices for this suggested Cu interconnection technology is the same as that in the Al(Cu)/SiO_2 technology [33]. The contact consists of a planarized SiO_2/Si_3N_4 dielectric with a Ti/TiN adhesion/diffusion barrier and chemical vapor deposition (CVD) tungsten contact plug. The diffusion barrier layers were evaluated by measuring the device's electrical properties of a p^+/n junction diode and the functionality of 64 Kb SRAM chips. A 0.25 μm junction depth and a self-aligned $TiSi_2$ salicide process were used. Ti(25nm)/TiN(25nm)/CVD W(1000nm) contact studs in SiO_2 were formed by chemical-mechanical-polishing (CMP). The diameter of the contact stud was 1μm. The studs were connected by Ta(20nm)/Cu(1μm)/polyimide(1μm), 2 μm x 2 μm metal lines overlapped with W studs by 0.5μm on each side. No significant difference in I-V curves, measured at 80 K, and after the samples were annealed at 400 °C for 16 hours, was observed [9]. Fig. 3 shows an optical micrograph of a 64 Kb SRAM. Functional check showed no bit yield lost after thermally cycling 12 times from room temperature to 400 °C. These data show that the Cu/polyimide-W contact stud structure did not degrade the devices under typical VLSI processing conditions.

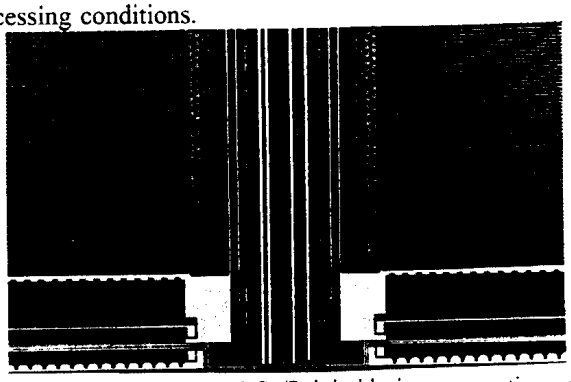

Fig. 3 Optical micrograph of Cu/Polyimide interconnections of 64 kb SRAM.

A specific materials challenge is to develop true interfacial layers which promote copper adhesion, prevent interdiffusion, serve as a deposition seed layer, and provide passivation on exposed surfaces during processing. One approach to generating interfacial layers is by appropriate processing of a copper alloy. Gibbsian segregation of solutes to the Cu surface and interfaces is too weak a driving force to form a robust interfacial layer. Preferably, a chemical reaction driving force is used, such as reaction with adjacent materials (containing oxygen, for example), which provides a mechanism for self-forming passivation and barrier layers. This approach has been demonstrated for Cu-Cr alloys. It has also been shown that during sputter-deposition of a Cu-1.0 at.% Cr alloy at 200-250 °C, precipitation and segregation of the Cr take place during growth [34]. Further optimization of this type of alloy process, or *in situ* formation of a surface layer of Nb [35] or TiN on Cu [36], for example, may provide a successful path to self-forming barrier layers.

Interconnection Integration

A. Damascene

Several different schemes for fabrication of multi-level Cu interconnections have been reported [4]. The most popular method is either a single or dual damascene process which is to pattern the dielectric level first, fill metal into trenches followed by chemical mechanical polishing (CMP) to remove the surface layer and leave material in the holes

and trenches [2,12]. A typical damascene level is fabricated by the deposition of a planar dielectric stack which is then patterned and etched using standard lithographic and dry-etch techniques to produce the desired wiring or via pattern. This is then followed by metal deposition of the Ta/Cu metallurgy. Subsequent levels are fabricated by repeated application of this process. In the damascene process all wiring levels are planar at every level, which typically results in enhanced wafer yield over a nonplanar structure. The Cu four-level interconnection structure shown in Fig. 4 was fabricated by the damascene process. This system demonstrates excellent planarity and low contact resistance [9] between the levels. Each level of Cu/PI structure is a trilayer structure of plasma enhanced chemical vapor deposition (PECVD) Si_3N_4/Polyimide (BPDA-PDA)/PECVD Si_3N_4.

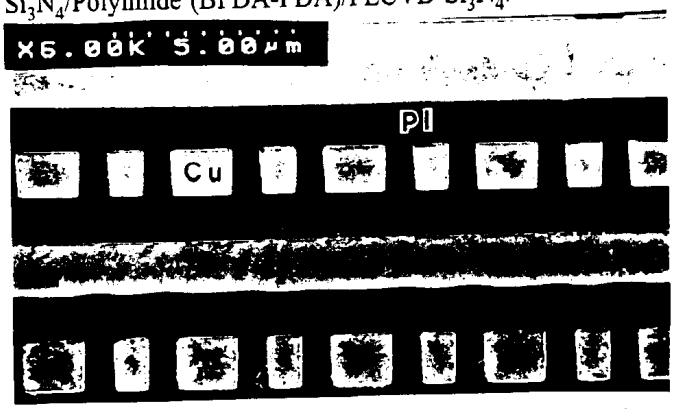

Fig. 4. SEM cross-section photographs of copper/polyimide interconnection system [2,9].

In this structure, a high dielectric constant PECVD Si_3N_4 was used, which is an excellent material from a processing standpoint, but its dielectric constant compromises electrical performance. A better materials choice, with a dielectric constant less than 4, should be used for taking full advantage of the Cu/polyimide interconnection architecture. In regions where the Si_3N_4 remains between polyimide layers, it increases the inter-line capacitance, and must therefore be as thin as possible. Other materials with lower dielectric constant serving the same function as the silicon nitride would be desirable.

B. Passivation/Adhesion

The use of Cu metallurgy raises several process concerns for the control of Cu oxidation and diffusion, since it is necessary to passivate Cu during processing steps. These steps might include O_2-plasma etching, polyimide curing, resist removal, and surface cleaning treatment. In addition, the adhesion of Cu to polyimide and SiO_2 is poor. A good metallic adhesion/diffusion barrier of Ta is deposited by sputtering. Using a thermal stress cycle of 500°C for 4 hrs (N_2 ambient), Ta was found to be suitable as a conducting diffusion barrier and PECVD Si_3N_4 as an effective insulating barrier. It is important to note here that the Cu lines are normally encased in a combination of Ta and silicon nitride regardless of process variations such as level-to-level overlay or RIE over-etch. Also important is the fact that the polyimide is completely passivated at all times. Certainly, no system of barrier layers will be defect-free; however, this combination of barriers and process steps is designed to minimize the exposure of Cu and polyimide to the outside environment.

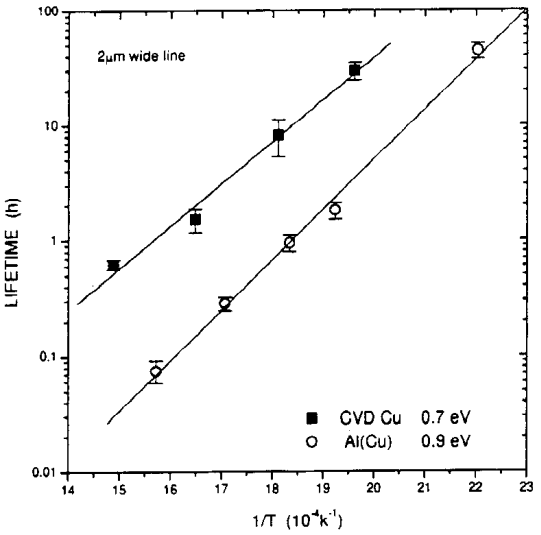

Fig. 5. Plot of log (lifetime) vs 1/T for CVD Cu and Al(0.5%Cu) lines. The lines are least-squares fits.

Electromigration

Atom motions of Cu and Cu alloys have been studied for several decades. The electromigration in two-level Cu/PI and Cu/SiO_2 structures has been reported by us [2, 37-39]. They showed that Cu is far superior to Al(Cu)/SiO_2 system for electromigration lifetime. However, a wide range of electromigration activation energy of 0.4 to 2.1 eV has reported in literature. [40, 41] The activation energy for the Cu grain boundary diffusion of 0.88 eV [42] to 0.95 eV [43] has been measured by the radioactive tracer diffusion techniques. It suggests that the electromigration activation energy in the pure Cu thin film lines should be close to 0.9 eV. A low value of activation energy for electromigration of 0.7-0.8 eV obtained in physical vapor deposited bamboo-like pure Cu [44] and CVD Cu [42] lines suggested that the dominant diffusion path in these fine Cu thin film lines was the interface diffusion. Fig. 5 shows the plot of lifetime (the time to grow a 0.7 µm long void) versus 1/T for CVD Cu and Al(Cu). A value of 0.7 eV and 0.9 eV is obtained for the CVD Cu and Al(Cu) respectively. The advantage of using Cu for electromigration resistance is lost, when one extrapolated interconnection lifetime at chip operating temperature. However, addition of a small amount of impurities (e.g. Sn,[45] Zr,[45,46] Pd [47]) in Cu can drastically affect the kinetics of electromigration and diffusion in Cu.

Conclusion

The processing sequences for fabricating Cu interconnections were described. A fully planarized four-level

Cu/polyimide structure was successfully fabricated by a damascene process. Use of a thin Ta liner around the Cu line reduces the effective resistivity to about 50% less than that of Al(Cu). The Cu microstructure shows a mixture of large and small grains, and twins. The silicon nitride layer in the Cu/polyimide structure serves as an adhesion layer between polyimide, passivation layer, barrier for preventing corrosion and chemical-mechanical polishing stop. The physical properties of various polymers were summarized. The combination of Ta liner and silicon nitride with W studs can effectively prevent Cu from penetrating into the Si to degrade the devices.

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