RC21618 (12/03/99)

Engineering and Technology

# IBM Research Report

## Quality of EDA CAD Tools: Definitions, Metrics and Directions

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**Abstract**

In this paper we survey major problems faced by EDA tools in tackling deep submicron (DSM) design challenges like: crosstalk, reliability, power, and interconnect dominated delay. We discuss the need for rethinking quality models used in EDA tools to allow early and reliable planning, estimation, analysis, and optimization. Key design quality metrics from a CAD tool perspective are surveyed, and methodologies and directions are proposed for the next generation design automation tools, intended to meet the challenges ahead. Ideas such as forward synthesis, incremental synthesis, system-level interconnect prediction and planning, and their implications on design quality, design tool architecture, and design methodology are explored.

# 1 Introduction

As the complexities of VLSI circuits increase, the crucial role of electronic design automation tools in virtually every aspect of VLSI circuit design is undeniable. Larger designs require much greater designer productivity to achieve reasonable design schedules and costs, and this dictates a greater role for EDA tools. In addition, as the chips become larger, geometries get smaller, and clock frequencies increase, on-chip interconnect gains increased importance [45]. Issues like wire-congestion and routability [144, 176], crosstalk and coupling noise [55, 162, 174], transmission-line behavior [45, 131], power consumption [20, 99], reliability and yield [82, 85], and their interrelation are crucial factors in designing next generation EDA tools. Furthermore, the intense competition, and the unending desire to get new products from inception of the ideas to the market in the shortest amount of time, is driving the electronic design automation strategists to reconsider their models and reform their methodologies [17, 18, 38, 77, 114, 115]. Semiconductor scaling limits are forcing designers to look to novel circuit and design techniques and to reduce design guardbands to maintain performance growth, all of which drive a need for greater modeling complexity and accuracy in EDA tools.

Traditionally, EDA tools have been divided into more or less independent realms, namely, system-level, high-level, logic-level, and layout-level [102], each with its own set of synthesis, verification, and analysis tool-set, which were more or less unaware of the underlying overall picture linking them to one-another and to the final design. A typical design process would consist of design specification, followed by manual or automated system-level synthesis/analysis/verification, the result of which would be handed over (the wall) to go through high-level synthesis/analysis/verifications and so on, until the layout of the design is available. If the design did not meet its timing/power/ area/noise constraints there would be a back annotation step and the whole process or part of it would have to be redone, resulting in a major waste of design effort and increased time-to-market.

With the exponential growth of circuit complexities, the importance of early planning and understanding the different trade-offs earlier in the design cycle is an absolute must. The interaction of various quality metrics such as delay, power consumption, crosstalk and coupling noise, reliability, wireability and wire-congestion, and understanding and modeling of these interactions gains more and more importance as the race for smaller feature sizes continues. In today's competitive marketplace a design which is incorrect or significantly sub-optimal design according any of these design quality metrics is not economically viable, hence all must be considered as design transformations and optimizations are being made.

A typical design methodology, targets one or two quality metrics, like area and delay, and considers other performance criteria only as after-thoughts. The synthesis process is done with only the primary objectives in mind. Other performance metrics are considered only late in the design process and are optimized mainly by local modifications to improve secondary quality criteria. However, since these local optimizations often result in unacceptable quality degradation from the standpoint of one of more important performance constraints, a time and resource-hungry iteration becomes inevitable, generally with no guarantee of convergence.

For all these reasons it is crucial to have a seamless synthesis/analysis/verification environment where the important quality aspects of the design can be monitored and optimized across the various levels of the design abstraction. More importantly, it is absolutely vital to have reasonably accurate prediction and estimation tools to allow the early exploration and pruning of the design space and to minimize and ultimately eliminate back annotation and time consuming iterations.

In this paper, we survey the key design quality metrics from a CAD tool perspective, and propose methodologies and directions for next generation design automation tools to meet the challenges ahead. Ideas such as forward synthesis, incremental synthesis, system-level interconnect prediction and planning, tool interoperability, and their implications on the design quality and design automation methodology will be explored.

# 2 Important Design Quality Measures and Their Interaction

In this section, we discuss various established and emerging design quality metrics, and the main challenges of EDA tools to effectively predict, analyze their interactions, and optimize them in the DSM era.

## 2.1 Area

Area of digital circuits is one of the first quality measures for VLSI design which has been studied. Estimation and minimization of the circuit area translates to reduction of the cost of silicon needed to implement the circuit. Moreover, there are secondary effects, like packaging cost [8], average interconnect length [43, 47], which have been studied in the context of area estimation.

Early studies on area estimation date back half a century to work by Shannon [147] and Muller [107] which relate the asymptotic complexity of Boolean functions to their number of inputs. Other researchers have studied the relationship between the area

complexity and entropy of the Boolean networks [29, 39, 75, 124]. Recently, research on area complexity of digital circuits has been revitalized in the context on system-level interconnect prediction [43, 44] and high-level power estimation [111, 112].
There are several important factors, however, which have been largely neglected in the area estimation literature. Many of these factors have to do with various design performance trade-offs and constraints, for example, the drive strength constraints at the chip/block output and the timing/delay constraints. Clearly, tightening these constraints, would require a more aggressive set of optimization steps such as gate resizing, cloning, or buffer insertion, which have direct consequences on the chip area requirements [36, 40, 79, 97, 158]. Such scenarios show the dependence of the final chip area on such performance constraints. Proper understanding and modeling of such dependence is important in designing realistic and practical area estimation and optimization techniques needed for next generation EDA tools.

## 2.2 Congestion and Wireability

Generally, the most time consuming step in the layout phase is the routing step. Hard routing instances would take much longer time to complete, and can result in routing solutions which are highly suboptimal, with ineffective usage of the routing area. Hence, it is imperative that the routing complexity, or the wireability of the design is considered earlier in the design cycle.
Previous research on the congestion and wireability have focused on package and image capacities [66], FPGA technology mapping [3, 145], FPGA routing and routing architectures [122, 179, 184], printed-circuit board designs [33], post-placement routability analysis [62], placement for wireability [73], rewiring [23], and planar layout routability [71, 91, 92].
With the growing role of the interconnect in the overall system performance the wireability and congestion gains increased importance. A highly congested region causes longer routing due to various wiring conflicts and constraints, in turn lowering circuit performance. Furthermore, wire congestion has implications on the reliability and yield of the circuit. Highly congested areas have higher potential for crosstalk and coupling noise as well, which can boost potential of failure and lower circuit reliability [87, 95]. Moreover, bridging defects are more likely in regions of high wire density [28, 65, 85]. Therefore, it is increasingly important to model and predict wireability and wire congestion during the early stages in the design process.

## 2.3 Crosstalk and Coupling Noise

Crosstalk and coupling noise[148] caused by the switching on adjacent interconnects boost failure mechanisms in high performance ICs [87, 95]. For example, coupling noise can cause functional errors by inducing incorrect signal values on logic lines. Moreover, induced noise may cause extra power consumption on signal lines due to momentary glitches within the logic. This indicates that crosstalk and coupling noise can and have deleterious effects on the long-term reliability of VLSI circuits [150, 162]. In the DSM technologies coupling effects play an even more significant role because

of the decrease in wire-spacing and the increase in wire thickness employed to reduce the parasitic interconnect resistance [162]. This is compounded by the increasing role of the interconnect parasitics on performance criteria such as delay and power consumption [8].
Hence, to optimize circuit performance in the DSM regimes we need early estimation and optimization mechanisms for crosstalk. Although low-level models and estimation mechanisms for coupling noise are relatively well understood [132, 182] there is a lot of room for higher level estimation of crosstalk mechanisms. One road block to attaining higher level estimates is the extreme dependence of coupling noise on temporal and spatial signal correlations [30]. Hence, most of the crosstalk estimation, analysis and optimization algorithms have focused on static noise.
Investigations have been reported on estimation and optimization of crosstalk at the global routing [105, 118, 181, 185], detailed routing [155, 165, 174], and post-routing [24, 155, 143] stages. Recently, Chen and Keutzer [30] have proposed a mechanism for considering temporal and functional information to eliminate false transition combinations and thereby overcome inaccuracies in static noise analysis.

## 2.4 Delay

Delay is a key performance factor in the modern VLSI design practices. The main driving forces for delay optimization are micro-processor and real-time Application-Specific Integrated Circuit (ASIC) designs. Delay optimization is inherently more difficult than area optimization because area is an aggregate metric, which causes various over and under estimates to cancel one another and results in an aggregate result that is potentially more accurate than the area estimation of individual components, while delay is a path-based metric which is much more sensitive to its individual components.
Early delay optimization study focused on minimizing the delay in a *unit delay model* [14, 56], which assumes unit delay for logic gates and zero delay for interconnects. These techniques aim to minimize the maximum number of logic gates along any path from the inputs to the outputs, or between registers. Such a delay model is mostly used for technology independent delay delay optimization.
The main problem with technology independent logic optimization is that it ignores interconnect delays, which tend to dominate the total path delay in DSM designs [77]. And although a few of these systems consider gate fanout [156], which has significant impact on the path and stage delay, many do not [158]. The problem is compounded when using static timing analyzers which over-estimate the delay through ignorance of false paths [16, 5, 84, 133].
Although, there has been considerable research on delay optimization [40, 46, 177], this problem has not been understood very well yet. While there are a few path-based optimization techniques [26, 46, 79], most of the research in the literature has focused on net-based techniques to simplify the problem formulation. Slack and budgeting algorithms have been proposed to translate the path-based timing objectives to a net-based optimization problem, with much simplified objective function [64, 110]. There have also been iterative techniques which use post-layout de-

lay and time-criticality information to perform re-budgeting and re-synthesis [157], placement modifications [101] or rewiring [72]. There are two problems with such an approach. First, because of the locality of the optimization techniques applied there is no guarantee that the circuit delay will converge to global or even local minima. Second, the efficient implementation of such iterative techniques requires truly incremental capabilities for the logic and layout synthesis algorithms, which is rarely the case in typical synthesis environments.
The increasing role of interconnect in total delay is rendering many of the simplifying assumptions invalid, resulting in a shift in the main stream performance driven synthesis toward increased interactions between high-level, logic, and layout synthesis realms.

## 2.5 Power Consumption

The advent of personal and portable computing and communication devices and the desire for longer battery life, the heat dissipation bottleneck in highly integrated circuits, increasing clock frequencies, and environmental considerations are among the main driving forces to push power consumption as a major performance criteria in modern VLSI design [20, 99, 119].
Approaches to power consumption minimization proposed in the literature include system and architectural level techniques such as bus-encoding [12, 117, 153], hardware/software partitioning [67, 90], multiple supply voltage designs [22, 126, 168], and power management and sleep mode exploitation techniques [152, 52, 53, 125], register transfer level techniques such as clock gating [13, 113, 163] and power conscious allocation and binding [21, 86], logic-level transformations such as activity-driven gate and logic decomposition and technology mapping [164, 166, 167], precomputation-based techniques [4, 34, 78, 104], layout-level techniques such as gate and wire sizing [40, 57, 138, 173], and power conscious placement and partitioning [169, 172] and circuit-level techniques such as dual threshold and low power logic families [178, 187], adiabatic and charge recovery circuit families [6, 183], dual-edge-triggered flip-flips [123], and circuit techniques for low-power data path elements [1, 81].
Arguably, the most effective way to reduce power consumption in CMOS technology is to lower the supply voltage, which exploits the quadratic dependency of dynamic power on voltage. Reducing the supply voltage, however, leads to increased delay and decreased clock speed. To satisfy the contradicting requirements of high performance and low power, variable-voltage design methodologies have recently been developed. At higher levels of design abstraction, the system can be made to operate at different points along power vs. delay curve by varying supply voltage [126]. At lower levels, instead, dual-voltage approach can be used for low power without degrading performance [25]

## 2.6 Yield and Manufacturability

Imperfections in the IC fabrication process, result in yield reduction and manufacturing defects, whose severity grows with a variety of issues such as the circuit size and density. Furthermore, severe operational conditions, e.g., excessive temperature and noise can boost the failure mechanisms, and hence reduce device life time. Therefore, the development and use of yield prediction, analysis and enhancement techniques and mechanisms at the design stage is economically justifiable. These techniques are aimed at boosting the tolerance of the design to manufacturing defects by incorporating a variety of logic (e.g. redundancy addition) and layout (e.g., floorplan modification and wire spreading) modifications. These techniques are surveyed in [82].

## 2.7 Interactions Among Objectives and Cost Functions

EDA tools use different cost functions to improve the design quality. The cost function used in optimization may not be exactly the same measurement in quality (area, delay, power consumption, etc.). For instance, wirelength is usually used to optimize the layout area and congestion is used to optimize the routability. Different cost functions used by EDA tools interact with each other to some extent. Most of them are globally consistent. Intuitively, partitioning circuits (i.e. using a net-cut objective) helps to reduce wirelength and minimizing wirelength is equivalent to minimizing congestion globally [176]. There have been different heuristics to optimize different cost functions. KL-FM [54, 76], CLIP [48], and hMetis [74] are among those to optimize the net-cut objective; GORDIAN [80], TimberWolf [146], and NRG [140] are examples of tools that optimize wirelength. Due to the nature of different cost functions, some are much easier to optimize than others. For instance, partitioning tools can handle very large designs faster than placement tools by an order of magnitude. It is reported that partitioning heuristics can be used in placement to speed up the optimization procedure [141]. Similarly, a wirelength objective is found to be very useful in minimizing congestion in placement [176].

Many useful optimization algorithms target a cost function which does not exactly match the design quality objectives. Often these quality objectives can be translated into weightings on the cost function used by the optimization algorithm, in many cases with multiple design objectives being mapped to a single optimization cost function. For example, a placement algorithm which minimizes wire length can use a net weighting based on net criticality and net switching frequency to simultaneously optimize delay and power consumption. There may be many alternative mappings between a design objective and a cost function, e.g., different ways to apportion delays along a path [110], and thus the translation process can result in an overly constrained and sub-optimal design.

Better understanding of interactions among different cost functions helps us steer EDA algorithms in the right direction. However, the interactions between other optimization objectives such as delay, power, clock skew, and noise are not well understood. Fundamental understanding of these concepts and their interactions are necessary to improve the quality of EDA tools.

With the current limited understanding of these issues, designers and CAD tools developers often must settle for rule-based and ad hoc techniques. For example, a rule might indicate typical interactions between clock-skew, power, delay, area, congestion metrics: minimizing clock-skew can potentially reduce glitch power and delay, while increasing area and congestion, or use of multiple supply voltages would potentially increase area and delay, while minimizing the power. Thus, a local change which might adversely impact critical metrics in the changed region would be disallowed. Another issue of growing importance which magnifies the significance of understanding interactions among these quality metrics is the inevitable presence of process variations [82]. This is particularly important for metrics like clock skew which are not single-ended constraints, and can be tolerated only within certain range.

# 3 Promising Directions in EDA Tool Development

In this section, we will propose some of the research directions that we find appropriate and most promising to address the main challenges and short-comings of current EDA tools and methodologies,.

## 3.1 Increasing Interaction Between Physical, Logical and Functional Design Abstractions

In the last few years, the research community has witnessed increasing levels of interactions between physical, logical, and functional realms in the synthesis of VLSI circuit and systems. The motivations, as mentioned earlier, include: increased and increasing importance of interconnects on the key performance criteria, minimized time to market, more efficient exploration of design solution space, and more accurate information on which to base synthesis decisions. Various approaches with varying levels of interactions between the synthesis and layout phases have been proposed. We can classify these techniques into several classes:
**Gain-Based Synthesis:** One of the recent directions in the synthesis area, is the constant-delay synthesis or gain-based synthesis [116] based on the theory of logical effort [159], which performs the gate sizing based on logical effort, electrical effort, and timing constraints. The succeeding layout phase, is then performed with additional timing and capacitance constraints to meet the initial gate sizing decision. The interaction between synthesis and layout is kept at a minimum and is achieved through generation of additional timing and capacitance constraints during the synthesis phase, for the succeeding layout stage. Successful application of this approach requires appropriate circuit libraries [11, 42].
**Layout-Friendly Synthesis:** Here, synthesis is more concerned about the layout implications. However, little or no companion layout information is used during synthesis, or if there is usage of some layout companion, no such information is passed onto the succeeding layout phase (e.g. through the generation of layout geometric constraints). The wireplanning of [59] is an example which can be classified into this category. The authors, use the placement of I/O pins to achieve a layout-friendly logic factorization. Other approaches belonging to this class include layout friendly logic extraction of [171, 170], and logic replication algorithms [50, 70, 100], which are typically combined with the min-cut partitioning [19, 61, 76, 83, 137].

**Layout-Driven Synthesis:** This class, includes those approaches in which synthesis is performed with a companion, possibly rough, layout/placement of various pieces of the logic. As the synthesis decisions are made, nodes may get created and/or deleted, and the companion layout may need to be updated to reflect these changes. The benefit of having a companion layout view is access to a more realistic estimates about the interconnect parasitics. This would allow the synthesis phase to make better decisions, while optimizing the logic. Examples of research which can be classified in this category are the technology mapping algorithms of [98, 121], the logic extraction techniques of [31, 69, 120], the reproducing placement problem of [139], and the layout-aware RTL binding algorithm of [180]. Other techniques in this category are those approaches in which logic optimization and resynthesis transformations are applied during the layout phase. As the name suggests, the synthesis decisions are driven by the current layout configuration, and the design quality or performance constraints. Rewiring algorithms of [23], the congestion alleviation resynthesis algorithm of [94], and other techniques reported in [72, 103, 109, 108, 154] are additional techniques we can classify here.
**Integrated Synthesis and Layout:** This class represents the ultimate integration of the synthesis and layout phases. Due to the prohibitive complexity of the problem, only partial integration results have been addressed in the past, which have barely scratched the surface of the possibilities in this direction. The integration of floorplanning, linear placement and technology mapping phases for area or delay minimization have been reported in [96, 134, 135, 136]. The integration of logic and layout phases for pass-transistor logic designs has been reported in [106].
**Synthesis-Driven Layout:** This category consists of those techniques which perform layout optimization moves either within the synthesis phase, or in a post-layout phase where synthesis and layout optimizations are applied to improve the design or meet the performance constraints. The floating steiner point problem of [139], linear placement modification of [94], and logic resynthesis approach of [93] are examples of techniques in this category.
**Synthesis-Friendly Layout:** This class consists of layout synthesis algorithms and environments which is capable of withstanding functional and/or logic changes, with minimal disruption to the layout. That is, layout synthesis should be performed in the presence of inaccurate or incomplete data in a way that the result is resistant to change. The previous approaches in this class [10, 175] have barely scratched the surface, and there is much room for further investigation in this area.

## 3.2 System Level Interconnect Prediction and Planning

The growing significance of interconnect and its implications on various optimization and verification EDA tasks has caused reconsideration of many assumptions and methodologies. Parallel to the efforts to integrate various synthesis and layout optimization techniques, researchers have identified a need for early estimation of and planning for the interconnect to allow more predictable design behavior in the DSM design methodologies.
The advent of deep submicron era has placed additional pressure on floorplanning to

account for interconnect [27, 37, 129]. Floorplanning needs to be used in the heart of many synthesis applications. Designers want to evaluate the effects of early design decisions on the final layout. The reduction in device sizes has led to the integration of microprocessor and chip-set. Quick floorplanning tools are needed in this domain as many different combinations exist for the chip-set. With large systems (hundreds of modules) Simulated Annealing based floorplanners fail. Ranjan et. al. [129] have discussed the fast prediction of floorplan metrics. They have proposed a *constructive* technique for predicting quality of the floorplan. In this work they exploit flexibility in the representation of modules to construct fast floorplans. Their results show that by their *constructive prediction* (as opposed to statistical prediction) approach they can estimate the quality of the final floorplan (e.g., routability and delays) within 5-10% accuracy. Chen et. al. [27] use a multi-stage simulated annealing approach to combine floorplanning and interconnect planning. They use a temperature adjustment scheme to obtain smooth transitions between different stages of the simulated annealing algorithm. Cong et. al. [37] combines buffer block insertion during interconnect-driven floorplanning.

## 3.3 Integrated and Incremental Synthesis

Most real-life VLSI system design projects have to meet a variety of often conflicting design performance constraints. Therefore, as the complexities of VLSI systems grow, it becomes increasingly important to explore design alternatives and compare various trade-offs at various stages in the design process. There is a wealth of literature in the area of incremental and dynamic data structures and algorithms. In the following subsection, we intend to briefly survey them briefly and note on their potential use for the implementation of an incremental EDA tool.

**Dynamic and Incremental Data Structures and Algorithms:** Frequently, small changes in the input of a problem are likely to cause correspondingly small changes in the output. It is, therefore, natural to attempt to identify the part of the output which needs to be updated and update it to produce new output. Incremental computation is especially useful in any context in which an object is being designed or defined gradually, and needs to be processed repeatedly throughout its design process. VLSI circuit design is a perfect example for such a scenario.

Many of the VLSI CAD problems can be modeled as (hyper)graph or tree problems (see for example [102, 68, 89, 130, 142, 149, 151, 186].) Various incremental and dynamic algorithms have been proposed for (hyper)graphs and trees [68, 130, 151, 186] It is therefore, worthwhile to study the incremental graph and tree algorithms and data structures [2, 9, 32, 51, 58, 127] in the context of EDA cad tools.

**Incremental Design Exploration:** To eliminate the potentially divergent design iterations EDA tools need to perform incremental design modification as well as incremental analysis and estimation of the results. Issues like back-tracking without having to recalculate (from scratch) where we have come from and some check-point management gain increased importance in such a scenario [156].

Incremental algorithms for synthesis and layout are needed when design undergoes local or incremental change. Often these local changes are made to correct local

errors or to make local improvements in one or more of the design quality metrics. Such local incremental design modification algorithms can be used to explore several alternative corrections or optimizations, and can be joined with incremental quality metric analysis algorithms to ensure that the complete design cost function is considered and all design constraint are met. Constructive algorithms usually are not suitable for incremental design changes due to their global nature, and because it is often difficult to map all necessary design quality constraints and cost functions into such algorithms. On the other hand, in many situations, mechanisms are needed to control the portions of the design that are exposed for optimization [15].
Many iterative algorithms such as simulated annealing and force directed algorithms can be easily modified to handle incremental placement and floorplanning. Most state-of-the-art placement algorithms are based on the top-down hierarchical approach. In the hierarchical approach, incremental placement is done by traversing several hierarchical levels. A small number of research results in the area of incremental layout have been reported in the recent past, focusing on floorplanning [41], placement [35], and FPGA routing [49, 128]. Incremental logic optimization has been studied in [15, 160], while [7] addresses BDD optimization using an incremental sifting algorithm. [161] presents an incremental approach for FSM traversal in the sense that the reachable states can be incrementally updated as local changes are made to the design. An incremental timing analysis algorithm is presented in [88]. Finally, a retiming-based incremental scheduling modification algorithm has been presented in [63].
Previous research and development effort on EDA tools that would allow incremental design modification and would provide incremental analysis and optimization mechanisms efficiently is very scattered and incomplete. Comprehensive study of incremental algorithms and solutions in the context of EDA CAD tool development is an open area of research with a great deal of potential. As our understanding of the off-line and constructive algorithms gain acceptable maturity, we have to face the challenge of devising efficient techniques to handle incremental design modifications in a comprehensive manner. Proper understanding and active participation in the incremental and dynamic data structure research and development would gain increased importance in such a scenario.

## 3.4 Interoperability and Standardization

The presence of multiple design constraints, the interaction of various quality measures, and the increasing pressures to achieve performance closures in the shortest time are key driving forces for development of multi-faceted, incremental design analysis and optimization engines which would allow the observation and optimization of various performance metrics across different levels of the design abstraction. Moreover, the unification of carefully designed query mechanisms and programming interfaces between these engines and the outside world is a key enabler for tool interoperability, which is of increasing importance in the EDA CAD industry.
Both the semiconductor and the EDA industries have started to recognize the increasing importance and the crucial role of tool interoperability for continuous growth of electronics industry in the DSM era. The majority of current EDA practices attempt

to facilitate a plug-and-play, tool-to-tool interface between an ever increasing suite of different tools.
Standard ASCII file exchange formats have enabled a degree of tool interoperability in the past, but are inadequate to support the degree of tool interaction needed to support DSM designs, where incremental design exploration and optimization play a central role. To address these shortcomings, and to provide an industry-wide standard to facilitate tool interoperability, industry trends are pointing to in-memory procedural interfaces between tools and databases. If such standards are not adopted the alternative will be proprietary procedural interfaces from EDA vendors, allowing tight integration between tools from one vendor, but inhibiting development of design solutions drawing tools from multiple sources.
Perhaps, the greatest imperative of all for EDA standards is to allow integrated logical and physical design through an open tool flow architecture, exemplified by the Chip Hierarchical Design System (CHDS) [17], and its Technical Data standard (CHD-Std) [60]. CHDS, which is funded by the semiconductor companies, is the only open architecture methodology supporting DSM design needs. The open architecture of CHDS creates an environment allowing users to integrate various tools as required by their large and diverse design flow requirements. The communication between the tools is facilitated through programming interface layers which create a bridge between tools that might not be able to communicate directly otherwise, hence the burden of communicating through ASCII files, and the bottleneck thereof, is essentially removed.

# 4 Conclusion

In this paper, we surveyed design quality metrics from a CAD tool perspective, and studied their interactions. Various shortcomings of the current EDA tools and methodologies to tackle the DSM design challenges were discussed and several promising remedies such as unified functional/logical/physical synthesis, incremental and integrated synthesis and optimization, and system-level interconnect planning and prediction are surveyed, and their implications on design automation practices and methodologies are explored.

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