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High Performance Bottom Electrode Organic Thin Film Transistors

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Abstract:
Pentacene-based organic field effect transistors exhibit enormous potential as active elements in a number of applications. One significant obstacle to commercial application remains: no completely lithographic process exists for forming high performance devices. Processing constraints prevent electrodes from being lithographically patterned once the semiconductor is deposited, but depositing the electrodes before the semiconductor leads to low performance transistors. By using self assembled monolayers to change the surface energy of the metal electrodes and morphology of the pentacene subsequently grown on the electrodes, high performance transistors may be formed using a process compatible with lithographic definition of the source and drain electrodes.

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I. Introduction

Organic semiconductors, and the organic semiconductor pentacene in particular (Fig. 1), have attracted considerable interest for use in a number of applications including large area flat panel displays, radiofrequency identification tags, and smart cards. Significant improvements have been made in the performance of these materials through the optimization of deposition parameters, material purification, and optimized design of device and gate geometry. Mobility values from test devices with pentacene active layers are adequate for use in these applications and are comparable to amorphous silicon [1]. Furthermore, the use of relatively high dielectric constant gate insulators results in low operating voltages without compromising mobility [2]. Processing these devices is, however, difficult. Pentacene is intolerant to exposure to solvents and other liquids [3] and this has limited its commercialization potential to date by eliminating photolithographic techniques from defining the semiconductor layer and contacts deposited after the semiconductor. Pentacene transistor drain-source contacts can be made in one of two configurations (Fig. 2)--top contact and bottom contact. It has been demonstrated that the bottom contact configuration gives inferior performance to the top contact configuration for a range of deposition conditions and material thickness [4], [5]. As a consequence of this behavior, the top contact configuration is almost exclusively studied and reported in the literature. Shadow masking is generally used in the laboratory to define the top contacts made to pentacene, a procedure which does not lend itself well to manufacturing.

To create a manufacturable process photolithographically defined drain and source contacts are needed. The performance levels needed for commercial technologies have only been demonstrated in top contact devices, however, and since no photolithography may be performed after pentacene has been deposited, bottom contact devices are the only option for a fully lithographic pentacene process. This paper will present a technique for achieving performance comparable to top contact FET devices using a bottom contact process, enabling a high-performance pentacene process with lithographically defined source and drain electrodes. This removes one of the two remaining obstacles to a high performance, fully lithographic pentacene process which is extensible to other organic materials.

II. Film Growth and Ordering

Pentacene's excellent semiconducting performance is the result of the high degree of molecular ordering seen during its film growth. Once the gate and gate insulator have been deposited in typical laboratory top contact devices, pentacene is evaporated under ultra high vacuum conditions in a molecular beam deposition arrangement. Details on the deposition system and process can be found in ref. [6]. Pentacene is a non-polar rigid short molecule and is repelled by substrates typically used, which are polar (e.g. SiO_2). Pentacene stands almost normal to the substrate and at room temperature packs in a crystalline structure similar to the triclinic structure observed in bulk single crystals.[7],[8] The pentacene layers deposited after the completion of the first polycrystalline layer encounter a different surface energy compared to the first layer deposited on SiO_2. As a result, these layers are less ordered and have smaller grains in a manner similar to

Stranski-Krastanov growth. Under specific deposition conditions, they form the "single-crystal phase" of pentacene, as opposed to the "thin film phase" formed directly on SiO_2. These growth forms and processes have been well documented by X-ray diffraction analysis [7],[9]. A typical surface micrograph of pentacene grown on an oxide is shown in Fig. 3.

Metals do not repel pentacene due to their almost infinite ability to rearrange their surface charge to accommodate nearby molecules. The effective surface energy is therefore considerably lower than that of materials typically used for the gate dielectric layers which serve as the substrate for pentacene growth (this effect is reported for poly(a-methylstyrene) in ref. [10]). Normally, higher attraction is expected to lead to smoother and more highly ordered growth patterns (see ref. [11] for an example involving amorphous silicon and ref. [12] for an example in a crystalline system). This is not the case with pentacene since repulsion from the substrate is essential for favorably ordered growth. Growth of the large-grained first layer of pentacene is consequently not observed on metals. This type of behavior has been observed in other rigid, short molecule systems, where an attractive surface disrupts the ordered packing of an otherwise crystalline rigid rod structure [13]. Absence of repulsion between the pentacene backbone and the substrate causes a fraction of the admolecules to lie flat on the surface during condensation which prevents lateral ordering, and a different non-planar form of the material occurs on the metal contact [5]. A micrograph of a typical pentacene layer formed on top of a metal layer is shown in Fig. 4a. The contrast between the two deposited phases is schematically drawn in Fig. 9.

In an organic FET the structure and contact behavior of the film formed on top of most of the electrode is not important for the performance of the device. Device behavior is only affected by the structure of the material in and immediately bordering the channel. The mobility in the metallic electrode is many orders of magnitude higher than that in the semiconductor, consequently charge injection only occurs at the channel edge. It is the crystalline structure of pentacene at this edge which causes the performance limitation of the bottom contact arrangement. The large grain, well ordered structure in the center of the channel changes into a microcrystalline structure as we move closer to the edge of the channel. Right at the edge of the channel between the interface with the bottom contact electrode is seen an area with a large number of grain boundaries and crystal frustration (fig 4b.).

III. Device Performance

Typical performance curves for top and bottom contact devices are shown in Fig. 5. Excepting the electrode placement, the pairs of devices shown are otherwise identical and were produced simultaneously. The absolute level of mobility varies substantially amongst sample pairs because of variations in the source material. One observed phenomenon is that the first several device runs after loading new source material exhibit poorer performance. High vapor pressure impurities which sublime with the semiconductor material are suspected to cause this problem. Many impurities act as dopants, increasing the parasitic channel conductance (decreasing the on/off ratio), and others act as trap centers which reduce the effective channel mobility. After several runs these impurities are depleted from the source material and performance improves. A number of control sets

have confirmed that identical samples produced in the same run have reproducible characteristics.

The behavior observed in the I-V characteristic is what would be typically expected from a field effect transistor. The bottom electrode device exhibits a strong nonlinearity near the origin and conducts significantly less current than expected at low drain-source voltages. It is clear that there is a nonlinear charge injection into the channel occurring. It might initially appear that a Schottky barrier is responsible for this nonlinearity. Gold, however, was used as the electrode for these devices. Au has a high workfunction which has been proven to give good ohmic contact to pentacene.

Several studies have demonstrated that the trap density is significantly higher and performance correspondingly decreased when organic semiconductors have a large number of small grains and many grain boundaries which form trapping sites [14]. The movement of charge carriers through a trap-dense system is impeded by scattering at these traps and momentum transfer of the carriers to phonons in the crystal. This decreases the mobility of the carriers (holes in the case of pentacene) in the material, and macroscopically the increased scattering manifests itself as a decreased field effect mobility in transistors with these increased grain boundary areas. It is believed that this scattering, and its nonlinear relation to electric field, accounts both for the nonlinearity observed at the origin and the lower effective mobility seen in bottom contact devices.

IV. Experimental Procedure

The solution to this problem, therefore, is to increase the ordering of the pentacene on the electrode and at the channel edge. To accomplish this the effective surface energy of the metal must be reduced. Self-assembled monolayers are able to change the polarity (and as a consequence surface energy) of a material by attaching on one end and presenting a backbone chain with selectable characteristics on the other end. Thiol-based self-assembled monolayers (SAMs) have been extensively studied on metals such as gold and platinum and are well characterized [15]. Indeed, one of the most widely used characterization techniques for self assembled monolayers is the measurement of the surface energy by observing the contact angles of solvents on treated surfaces. Another appealing characteristic of using a SAM is the self-limiting characteristic of such films. Once a monolayer has adhered to the surface no more material will attach. This prevents a thick layer from forming which might interfere with charge injection into the FET channel.

The transistors were fabricated on a degenerately doped silicon wafer, which also served as a gate electrode. A thermally grown silicon dioxide layer was used as the gate dielectric for the transistors. Gold-chrome electrodes were then deposited and patterned on SiO_2 substrates by electron beam deposition The electrodes were patterned using shadow masks for convenience, but nothing prevents the use of lithographically patterned electrodes for this process. 1-hexadecanethiol was applied from solution to the Au-Cr electrodes to modify the surface energy. In this step it is key that chrome or another appropriate material must be used as an adhesion layer for the electrode because the thiol treatment lifts pure gold films from SiO_2.

The thiol was applied by forming a dilute solution of 1-hexadecanethiol in ethanol and immersing the substrates overnight, using part of the procedure from ref. [16]. Pentacene was then evaporated under ultra high vacuum conditions onto the electrodes. Device characteristic curves and mobility measurement results for a treated sample and a

control which was soaked in pure ethanol prior to deposition are shown in Fig. 6. It can be seen that the treatment increases the mobility considerably--by a factor of 7 in the linear region and more than a factor of 5 in the saturation region--and also increases the current carrying capability of the device considerably. The treated device has performance comparable to top-contact devices using the bottom contact geometry. Great care was taken to eliminate all possible variables in metal deposition, cleaning of the substrate wafers, etc. Both sample substrates were processed simultaneously and in the same deposition runs, with thiol added to the ethanol solution used to treat one of the wafers as the only variable. This result has been repeated with similar success in other sample pairs. Such a pair is shown in Figure 7. The mobility is enhanced by a factor of three in the 1-hexadecanethiol treated sample to 0.48 $cm^2V^{-1}s^{-1}$ (Fig. 7b), even in a situation where the material deposition parameters are very favorable to high performance and the untreated device is performing relatively well (μ=0.16 $cm^2V^{-1}s^{-1}$)(Fig. 7a).

It is clear from these measurements that the treated sample has a significantly higher mobility. Scanning electron microscopy also confirms that the samples have significantly different morphologies. Fig. 8 shows a micrograph of the channel edge of a device formed by depositing pentacene on top of a treated electrode. The structure in this micrograph shows large grains on both sides of the electrode edge, demonstrating that the SAM has led to an increase in the grain size on the electrode. While further tests are needed to directly confirm the hypothesis that the increase in grain size leads to a decrease in trap density and consequently higher performance, this result is fully consistent with the conclusion reached by other studies in which the pentacene grain size has been modulated using other means, such as by using temperature and deposition rate as in [17].

One open question is the effect on contact resistance of placing a potentially insulating film on top of the electrode. While this is normally expected to increase the contact resistance, the overall effect observed shows significant net benefit to the process. Self-assembled monolayers properly deposited are extremely thin and do not present a significant conduction barrier. Additionally, the effective contact resistance in normal bottom-contact devices is both high and non-linear. This process eliminates the barrier small grain size semiconducting material presents to charge injection into the channel.

V. Conclusions

This technique has the potential to greatly expand the applicability of organic semiconductors as active elements in dense lithographically patterned circuits. It allows the large grain growth of pentacene seen in the channel center on the SiO_2 gate dielectric to also occur on the electrodes deposited before the semiconductor. The highly ordered structure this forms allows high performing semiconductor material to be grown through the entire channel regardless of the surface energy of the material serving as the deposition substrate. The high performance once limited to devices in which pentacene was deposited on dielectrics only can now be observed in devices where the electrodes are deposited first on the dielectric followed by the pentacene film. This permits photolithography of the electrodes in a high-performance organic FET device and is a key step to producing a manufacturable deposition process for such devices.

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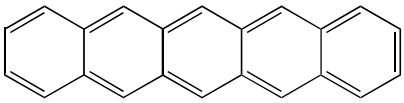


Formula: $C_{22}H_{14}$	[18]
Molecular Weight: 278.35	[18]
Melting Point: 573K	[18]
Vapor Pressure at 444K: 0.00161 Pa	[18]
Optical Bandgap: 2.8 eV	[19]

Figure 1: Structure and basic properties of pentacene

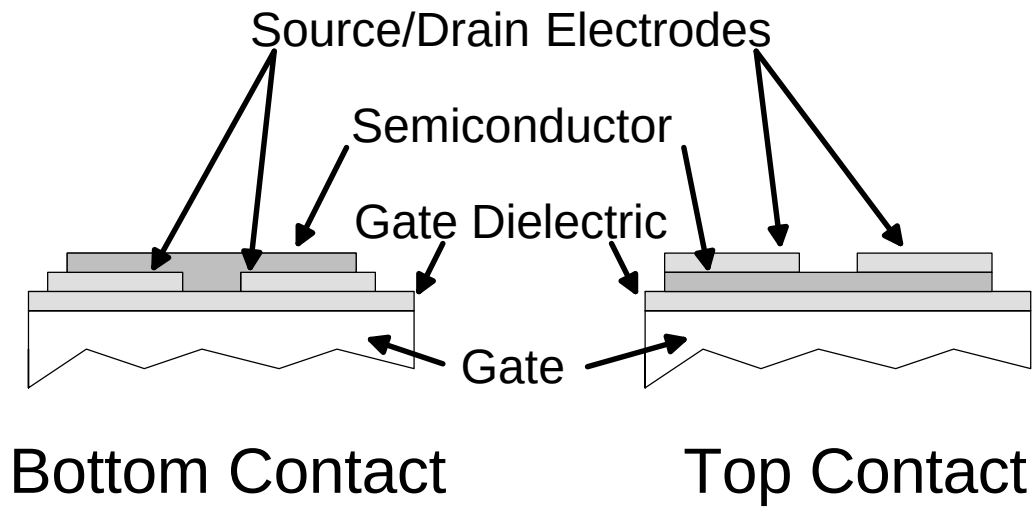


Figure 2: Transistor Layout, Showing Two Layout Alternatives.

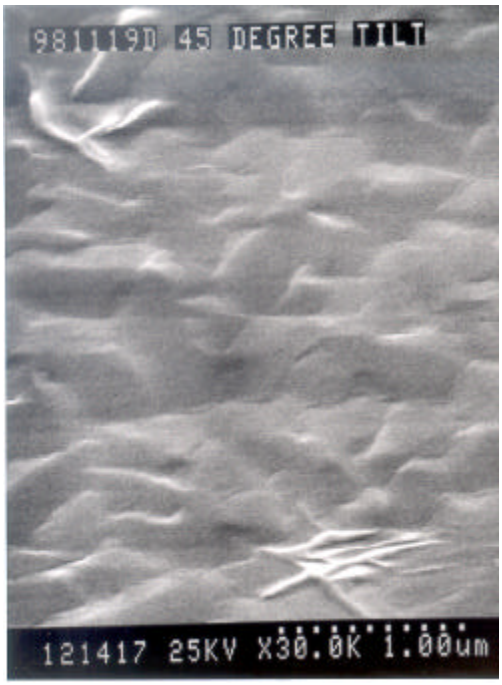
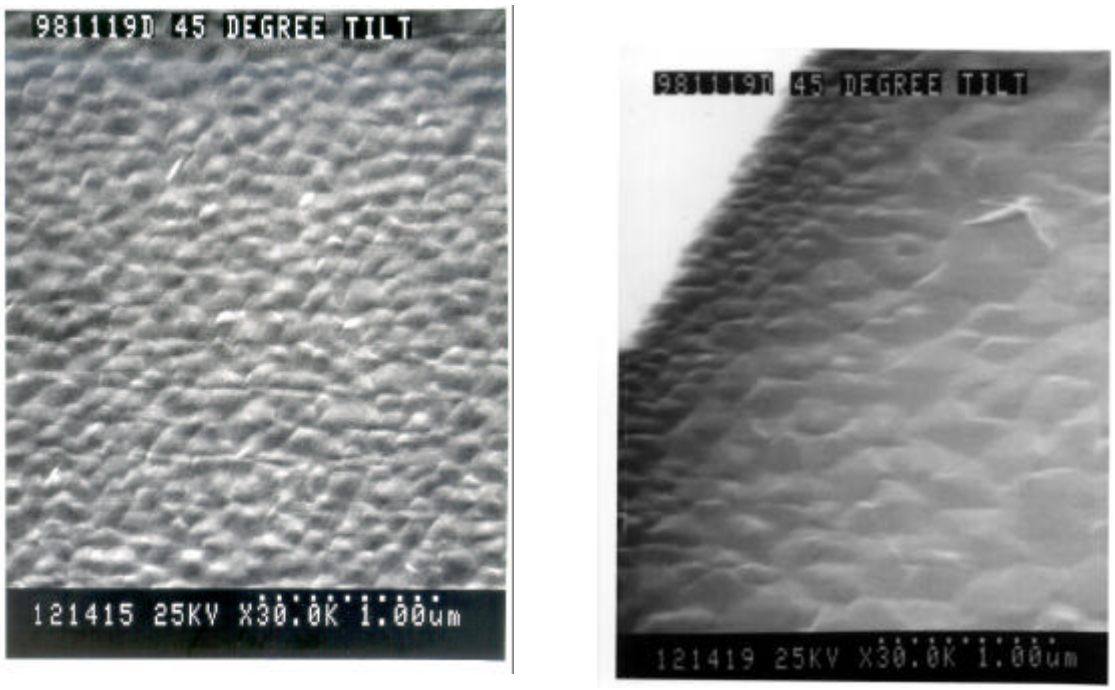


Figure 3: Micrograph of Pentacene grown on typical oxide.



(a) (b)

Figure 4: These micrographs were taken from a bottom contact sample. Pentacene was deposited on SiO_2 with patterned Au electrodes on it. Fig. 4a shown the microcrystalline growth of pentacene on Au. The edge of the Au electrode is in the upper-left corner of Fig. 4b. To the right the large-grained pentacene structure expected towards the center of the channel (on SiO_2) is seen. From the edge of the Au towards the center of the channel a transition region exists containing the microcrystalline form of pentacene. This form is believed to be the cause of inferior performance for bottom contact devices.

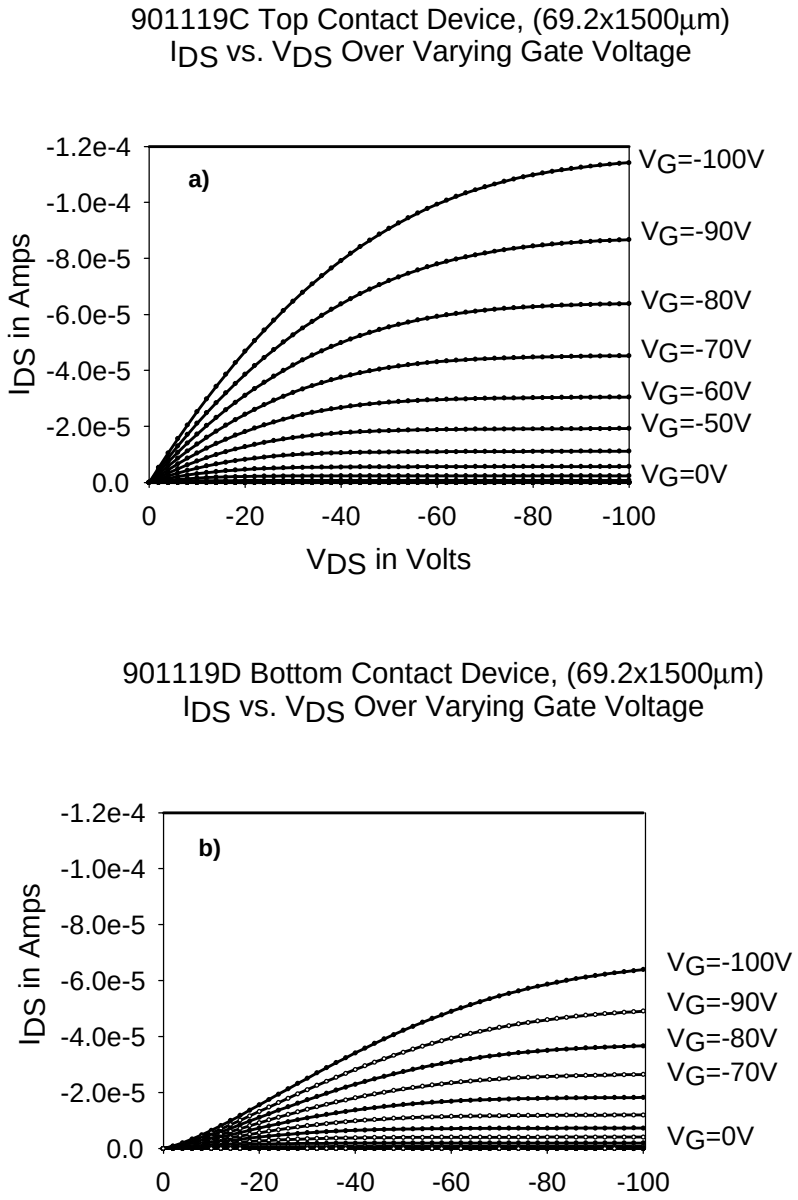
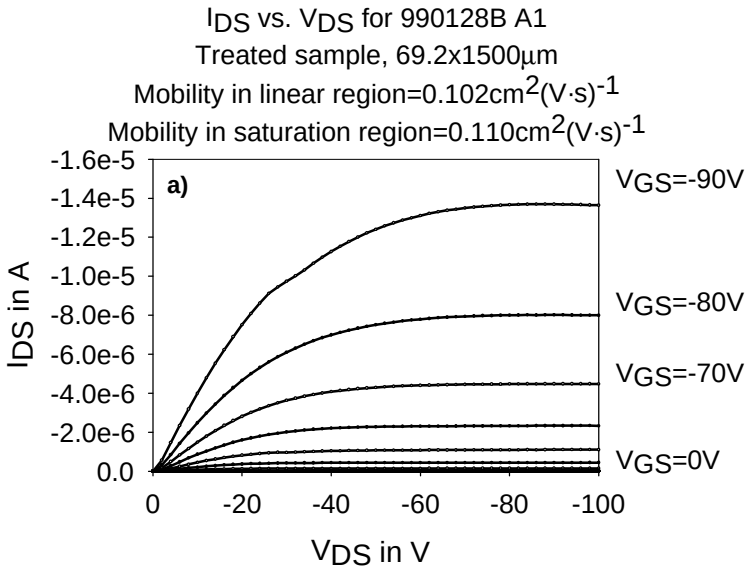
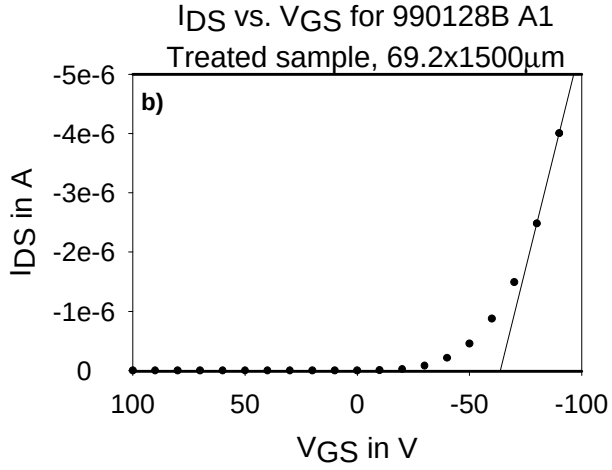


Figure 5: Performance curves for simultaneously deposited untreated top (a) and bottom (b) contact devices. The top contact device exhibits superior performance with almost double the mobility and current carrying capability--0.25cm^2(V×sec)$^{-1}$ vs. 0.13cm^2(V×sec)$^{-1}$. Also note the sigmoidal non-linear turn-on in the bottom-contact device, which we believe is a product of the non-linear charge conduction in the trap barrier.


I_{DS} vs. V_{DS} for 990128B A1
Treated sample, 69.2x1500µm
Mobility in linear region=0.102cm^2(V·s)$^{-1}$
Mobility in saturation region=0.110cm^2(V·s)$^{-1}$
a)
V_{GS}=-90V
V_{GS}=-80V
V_{GS}=-70V
V_{GS}=0V
I_{DS} in A
-1.6e-5
-1.4e-5
-1.2e-5
-1.0e-5
-8.0e-6
-6.0e-6
-4.0e-6
-2.0e-6
0.0
0
-20
-40
-60
-80
-100
V_{DS} in V


I_{DS} vs. V_{GS} for 990128B A1
Treated sample, 69.2x1500µm
b)
I_{DS} in A
-5e-6
-4e-6
-3e-6
-2e-6
-1e-6
0
100
50
0
-50
-100
V_{GS} in V

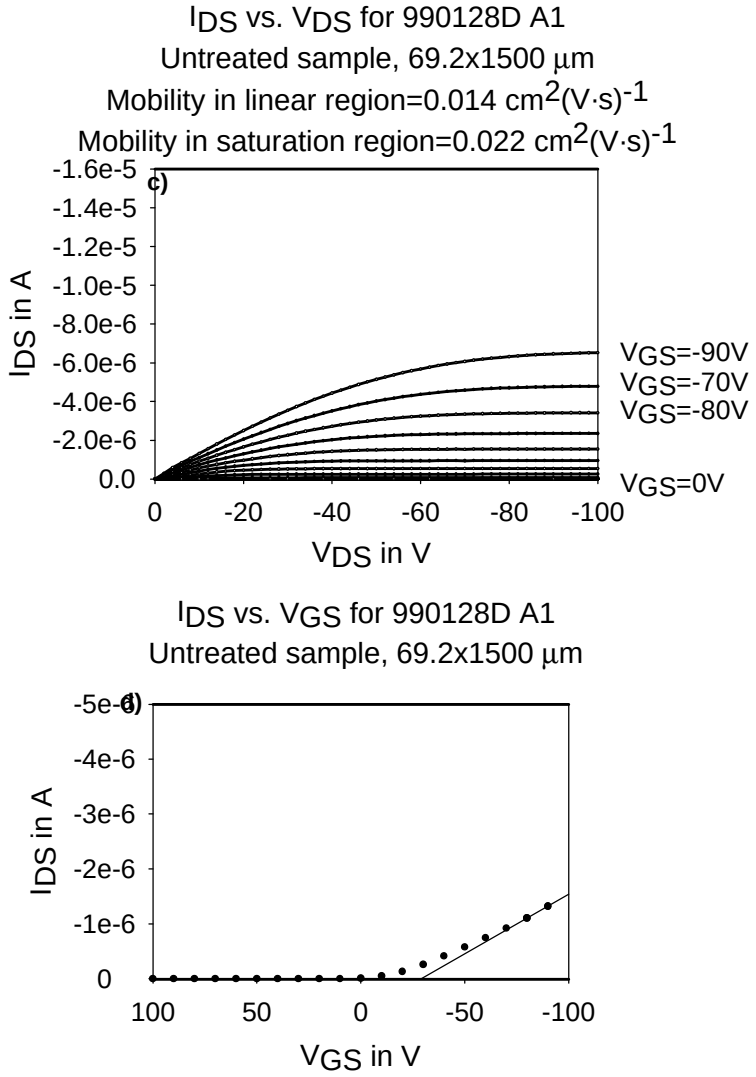


Figure 6: Linear region I_{DS} vs. V_G graphs of treated (a,b) and untreated (c,d) devices shown drawn to the same scale for comparison. The treated device exhibits significantly higher current carrying ability, and has a mobility of $0.102 cm^2(V \times sec)^{-1}$ in the linear region. The control device, which was soaked in pure ethanol instead of the thiol solution, has a mobility of $0.014 cm^2(V \times sec)^{-1}$ in the linear region. The size of the devices is 69.2x1500µm. In saturation the effective mobility is higher: $0.11 cm^2(V \times sec)^{-1}$ for the treated device and $0.022 cm^2(V \times sec)^{-1}$ for the untreated device. This increase in performance clearly demonstrates the effectiveness of the process.

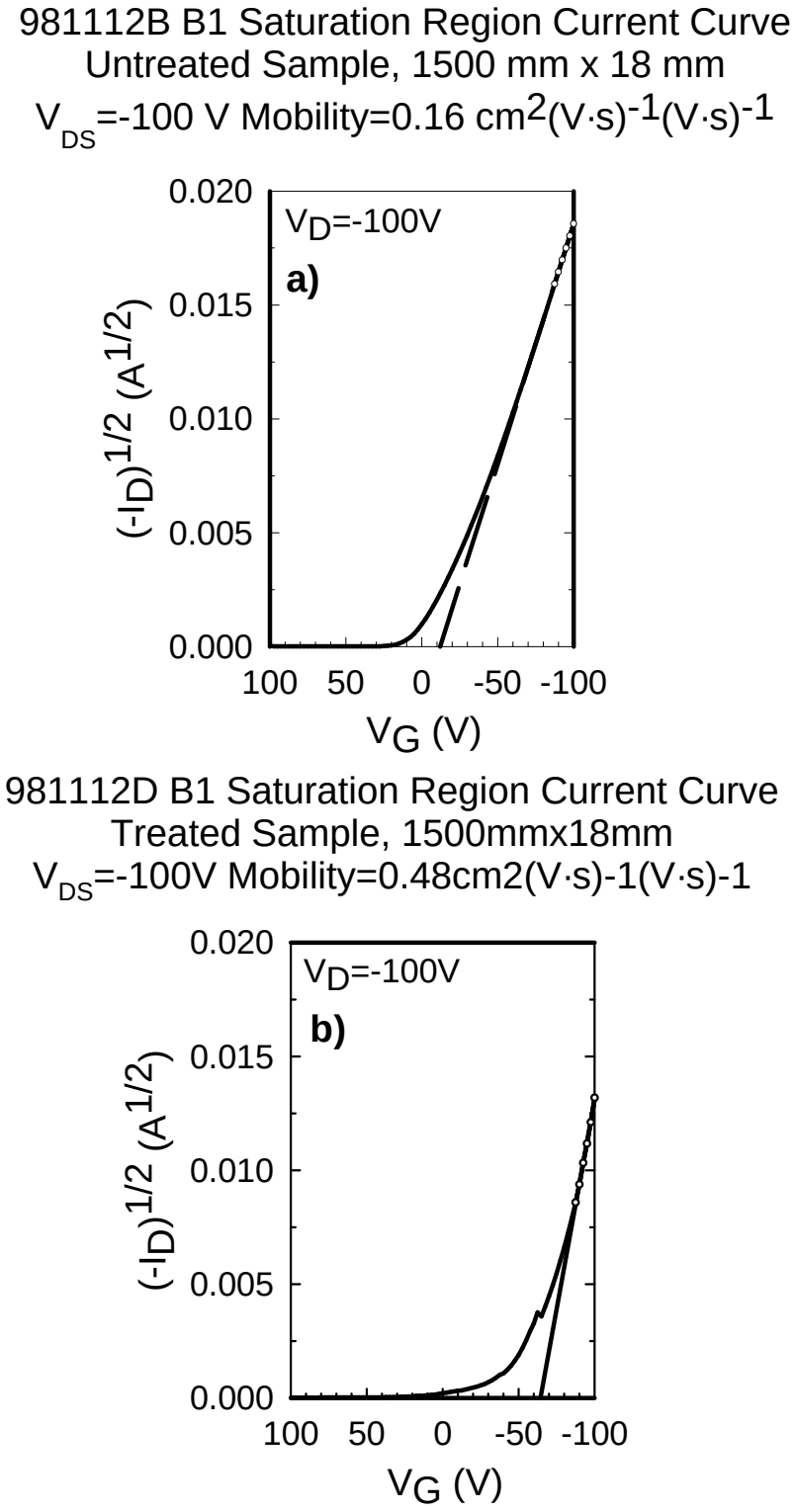


Figure 7: Saturation region characteristic curves of two samples produced using the process of Figure 6. Both graphs are on the same scale for comparison. A significantly higher slope and sharper turn-on is

seen in the treated sample (b). Here the mobility is significantly enhanced by the use of the treatment process--by a factor of three - even in a situation where the material deposition parameters are very favorable to high performance and the untreated device is performing relatively well (a).

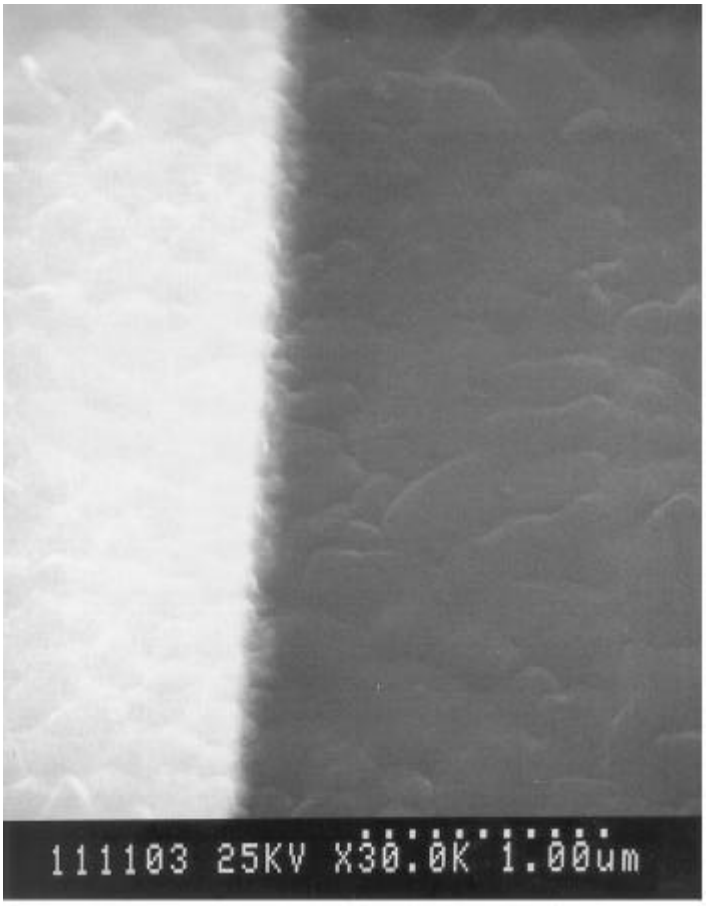
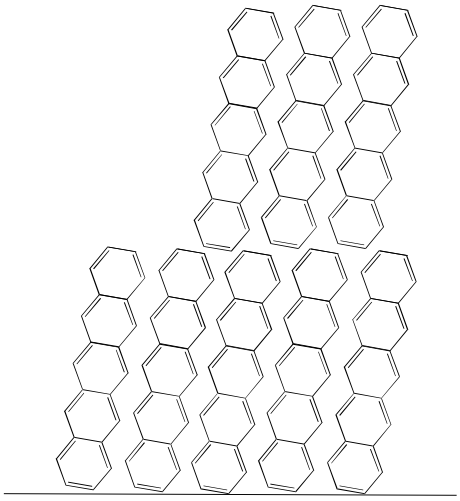
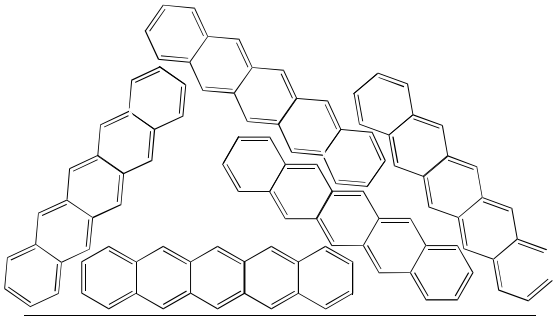


Figure 8: Micrograph of thiol treated edge
This image is from a sample (981112D, discussed in Fig. 7b). A 1-hexadecanethiol SAM was deposited on Au followed by pentacene. The pentacene forms large grains on top of the electrode, which can be seen on the left-hand side of the micrograph, and the grain boundary frustration observed in Fig. 4 is not seen. The lack of small grain structure material in the channel is believed to lead to reduced trap density and the higher performance seen in these devices.



a)



b)

Figure 9: (a) Schematic diagram of ordered packing state, with substrate repelling pentacene molecules. (b) When the pentacene is attracted to the substrate material, as is the case with metals, the ordered packing state cannot form.