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IBM Research Report

Investigations of UHV/CVD Deposition of SiGe Alloys on Silicon-on-Sapphire Substrates for Application to Device Fabrication Technology

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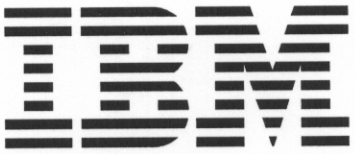

Introduction

Epitaxial silicon-on-sapphire (SOS) has microtwin densities in the 10^5-10^6 cm^{-2} range resulting in an equal density of large facated pits on UHV/CVD-grown SiGe p-MODFET wafers. Although individual devices have been fabricated and tested on such wafers, the high density of pits makes these substrates unsuitable for integrated circuits. Additionally, it is necessary to first grow a strain-relaxed SiGe buffer layer (1-2 micrometers-thick) underneath the active device layers reducing the advantages of using a sapphire substrate. Therefore wafer bonding methods are being investigated to achieve high quality Si and SiGe-on sapphire substrates for these devices. A collaboration has been established between IBM and Prof. Tom Kuech at the University of Wisconsin (UW) for these investigations.

Joint Project with University of Wisconsin

A meeting was held at UW in September with Pat Mooney and Jack Chu of IBM and Tom Kuech and Pete Moran of UW to discuss the initial wafer bonding results and to plan the next set of experiments. Initial experiments are aimed at learning how to transfer a thin (100 nm) Si layer to sapphire. Subsequently the same method will be used to transfer a thin SiGe layer to sapphire. Relaxed SiGe buffer layers of various alloy composition will be prepared at IBM for the latter experiments. It was decided to explore using an interfacial SiO_2 layer to address problems of blister formation at the bonding interface when heating the bonded wafer above 250 °C. An oxide film will be deposited on both the Si and the sapphire wafers and the oxide films will be bonded together. The tooling at UW is for 4" diameter substrates. To achieve a uniform thickness Si layer on sapphire, the starting material will be bonded SOI substrates purchased from SOITEC.

Preparation of SiGe Wafers for Bonding Experiments

Relaxed SiGe buffer layers have a cross-hatch surface roughness and therefore need to be polished flat prior to wafer bonding. A 4"wafer holder for IBM's chemical-mechanical polishing (CMP) tool was purchased and experiments were done to determine the polishing times needed to smooth SiGe (15% Ge) films on 4" substrates. Figs. 1 and 2 show atomic force microscopy (AFM) measurements and analysis of the surface of an as-grown SiGe (x=0.15) relaxed film and after CMP polishing for 8 minutes. The root-mean square (RMS) value of the roughness is reduced from 5 nm to 0.4 nm. Although these SiGe films were grown on bulk Si substrates rather than SOI substrates, the polished SiGe wafers were sent to UW to verify that the polished surface was suitable for wafer bonding, i.e. to confirm that the SiGe surface would stick to sapphire at room temperature.

Although the RMS surface roughness after polishing is within the limits required for wafer bonding, there will be occasional voids at the bonding interface where very deep grooves or pits remain after polishing. In addition, better control the final SiGe layer thickness can be achieved if the SiGe layer is not polished prior to bonding. These objectives can be achieved by depositing an oxide film on the as-grown SiGe film and then polishing the oxide surface prior to bonding. This will also provide an interfacial oxide film to facilitate bonding SiGe to sapphire as mentioned above.

Good quality thermal oxide cannot be grown on SiGe; therefore a low temperature deposited oxide must be used. Since 4" substrates are needed for wafer bonding experiments at UW, the only available low temperature oxide at IBM is a plasma-enhanced chemical vapor deposition (PECVD) oxide. Even when deposited on a Si substrate, the PECVD oxide surface is rough and must therefore be polished flat prior to wafer bonding. The polishing rate for PECVD oxide films on 4" Si wafers was determined to be 15 nm/min. Polishing for 2 min is sufficient to achieve a smooth surface on both 200 and 400 nm-thick oxide films on 4" Si substrates.

Figs. 3 and 4 show AFM images of a SiGe (x=0.15) wafer, similar to the one shown in Fig. 1, after deposition of 700 nm of PECVD oxide and after polishing for 8 min. The RMS roughness on the oxide surface was about 5 nm and was reduced to 0.4 nm after polishing for 8 min. Relaxed SiGe (15% Ge) films with 560 nm deposited oxide overlayers on SOI substrates will polished and sent to UW for bonding experiments.

Summary

A collaboration with UW to investigate fabricating Si- and SiGe-on-sapphire substrates has been established and experiments were planned at a meeting held at UW in September. CMP polishing of SiGe films and SiO_2 films deposited on both Si and SiGe (15% Ge), all on 4" substrates, has been demonstrated. Oxide coated SiGe (15% Ge) films on 4" SOI wafers are being prepared for wafer bonding experiments at UW.

Recent Publications and Presentations Relevant to this Project:

1. "SiGe MOSFET Structures on Silicon-on-Sapphire Substrates Grown by Ultra-High Vacuum Chemical Vapor Deposition", P.M. Mooney, J.O. Chu and J.A. Ott, J. Electron. Mater. **29**, 921 (2000).

2. "SiGe Technology: Heteroepitaxy and High-Speed Microelectronics" P.M. Mooney and J.O.Chu, Annual Reviews of Materials Science **30,** 335-362 (2000).

3. " RF Systems Based on Silicon-on-Sapphire Technology," I. Lagnado, P.R. de la Houssaye, W.B. Dubbelday, S.J. Koester, R. Hammond, J.O. Chu, J.A. Ott, P.M. Mooney, L. Perraud, K.A. Jenkins, 2000 IEEE International Silicon-on-Insulator (SOI) Conference, Wakefield, MA, October 2-5, 2000.

Roughness Analysis

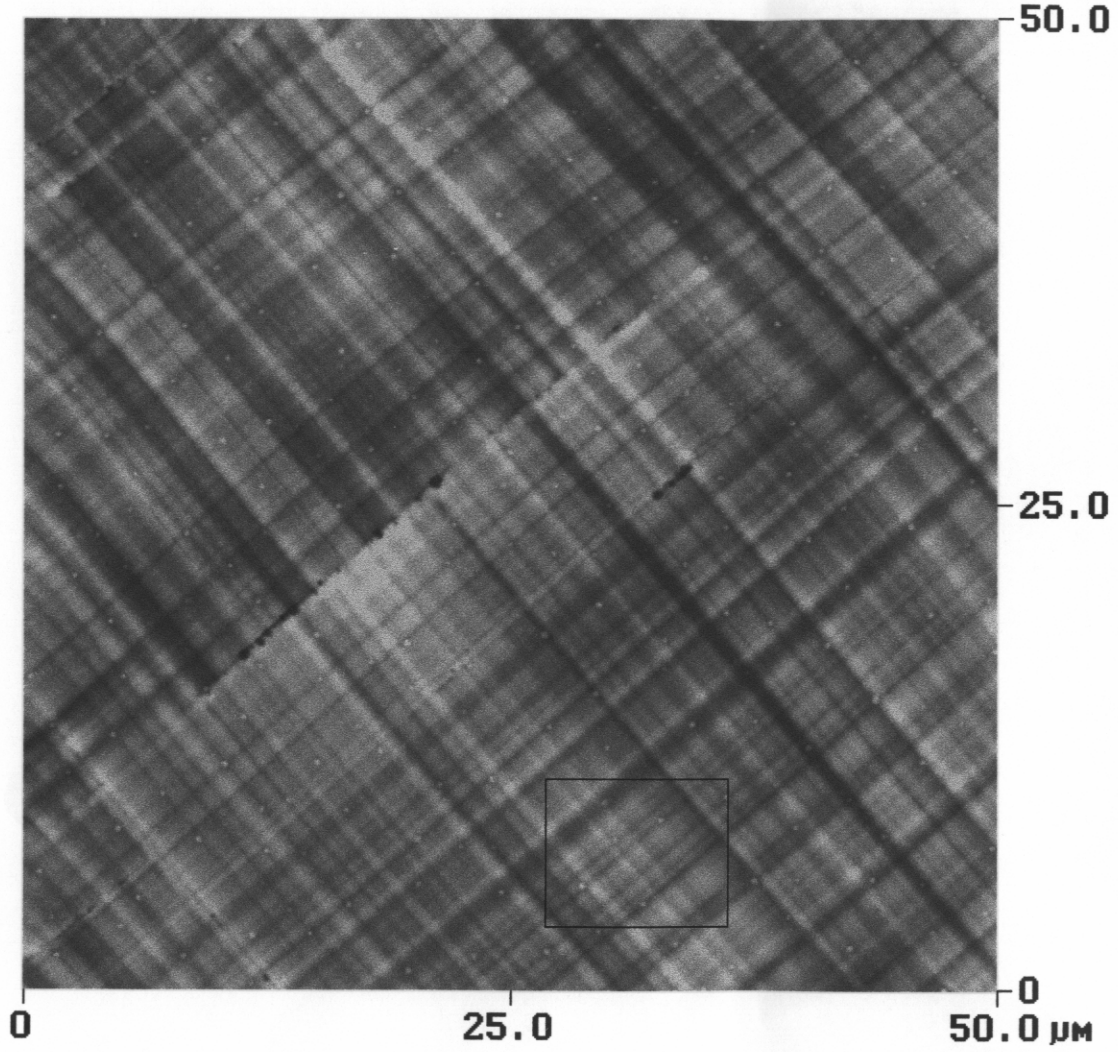

Image Statistics

Img. Z range	56.952 nm
Img. Mean	-0.000001 nm
Img. Raw mean	43.378 nm
Img. Rms (Rq)	4.814 nm
Img. Ra	3.784 nm

Box Statistics

Z range	25.785 nm
Mean	0.879 nm
Raw mean	44.257 nm
Rms (Rq)	4.073 nm
Mean roughness (Ra)	3.294 nm
Box x dimension	9.393 µm
Box y dimension	7.632 µm

Fig. 1. AFM image and analysis of an as-grown strain-relaxed SiGe (15% Ge) film.

Roughness Analysis

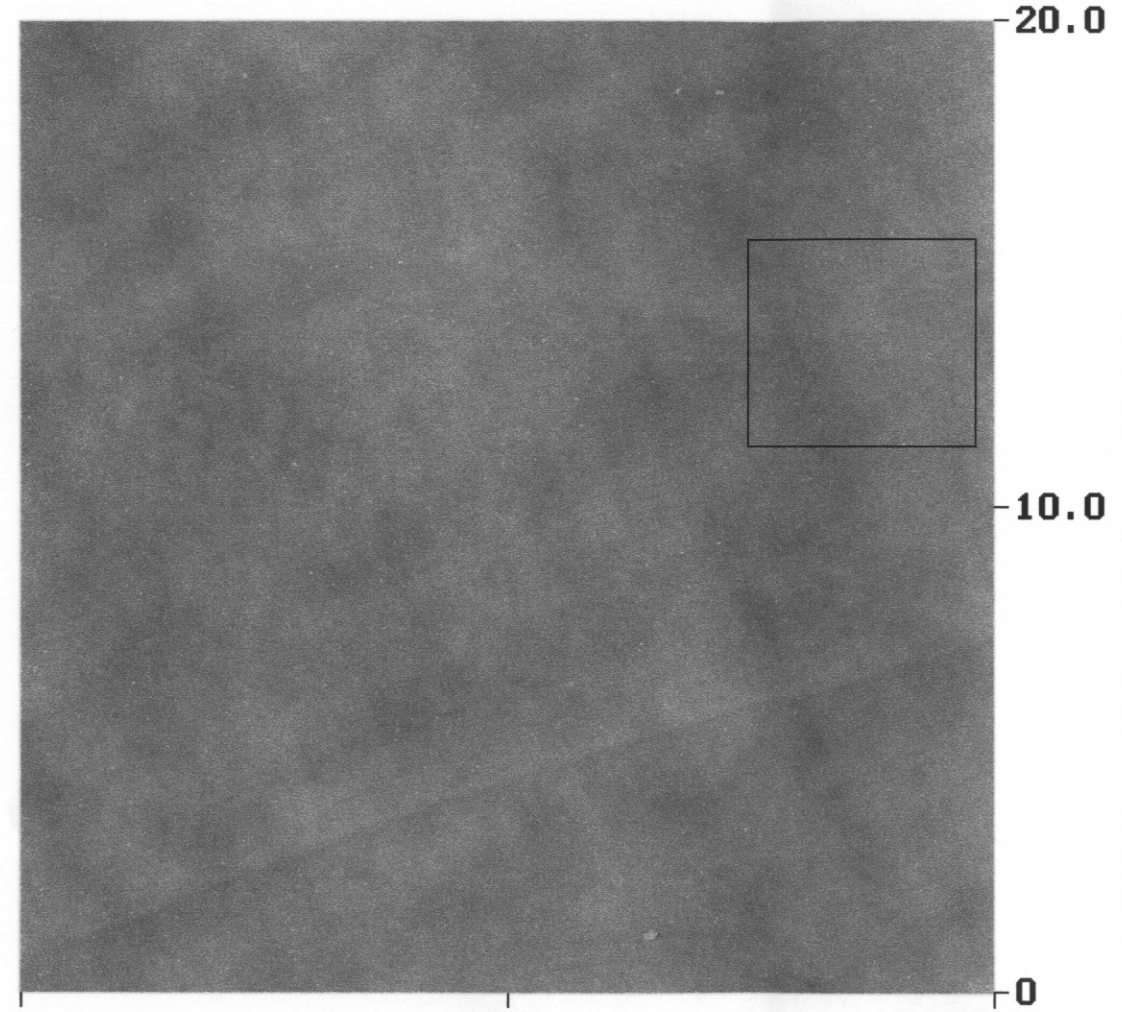

Image Statistics

Img. Z range	51.595 nm
Img. Mean	-0.001 nm
Img. Raw mean	-23.651 nm
Img. Rms (Rq)	0.401 nm
Img. Ra	0.182 nm
Img. Srf. area	400.02 µm²
Img. Prj. Srf. area	400.00 µm²

Box Statistics

Z range	2.865 nm
Mean	-0.024 nm
Raw mean	-23.674 nm
Rms (Rq)	0.163 nm
Mean roughness (Ra)	0.125 nm
Max height (Rmax)	2.739 nm
Box x dimension	4.697 µm
Box y dimension	4.266 µm

Fig. 2. AFM image and analysis of a relaxed SiGe (15% Ge) film after polishing for 8 min.

Roughness Analysis

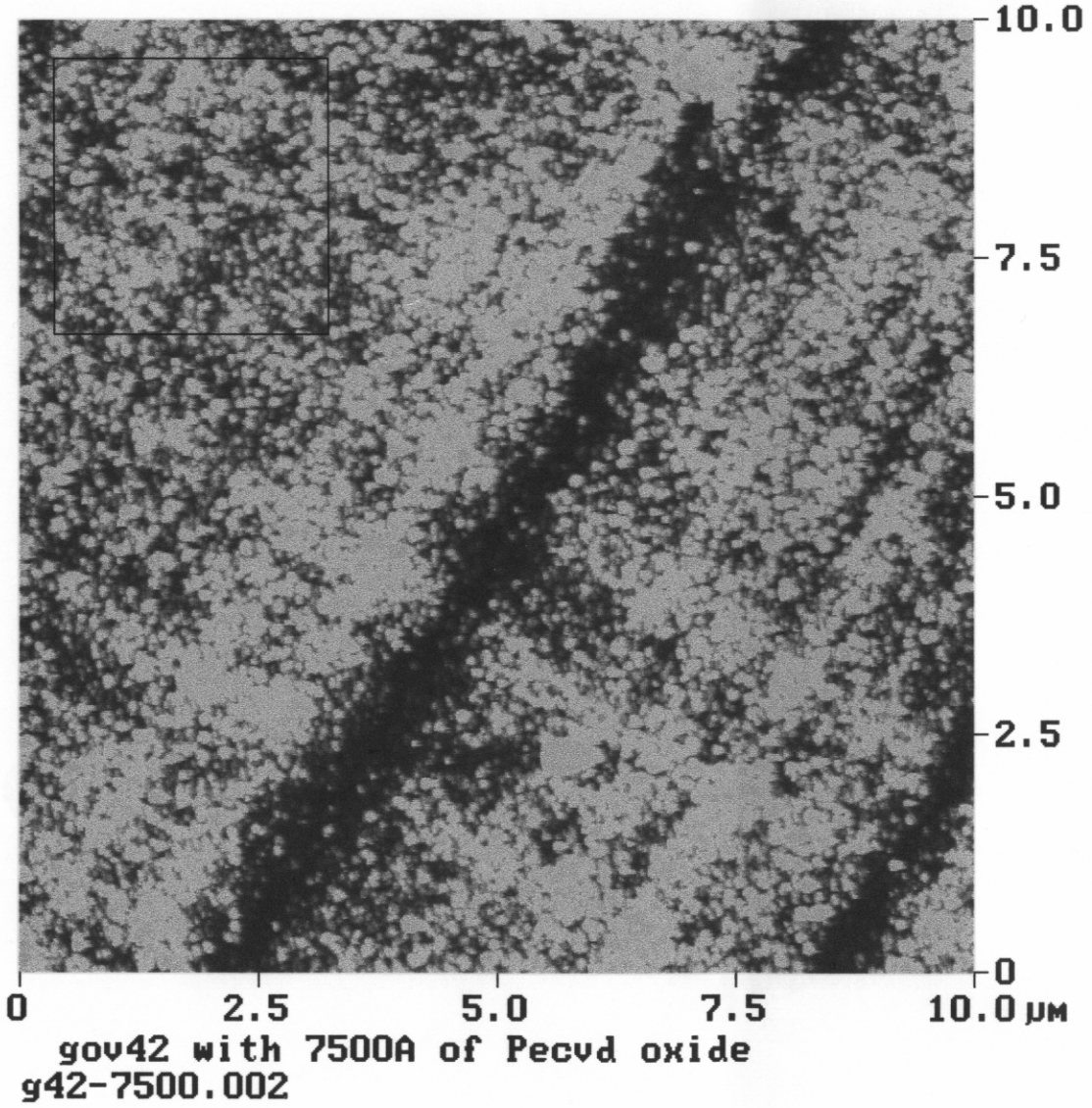

Image Statistics

Img. Z range	75.177 nm
Img. Mean	0.000000 nm
Img. Raw mean	-11.479 nm
Img. Rms (Rq)	5.307 nm
Img. Ra	4.023 nm
Img. Srf. area	101.03 µm²
Img. Prj. Srf. area	100.00 µm²

Box Statistics

Z range	27.270 nm
Mean	-0.033 nm
Raw mean	-593.97 nm
Rms (Rq)	3.840 nm
Mean roughness (Ra)	3.079 nm
Max height (Rmax)	27.605 nm
Box x dimension	2.877 µm
Box y dimension	2.896 µm

Fig. 3. AFM image and analysis of a relaxed SiGe (15% Ge) film with 700 nm PECVD oxide as-deposited.

Roughness Analysis

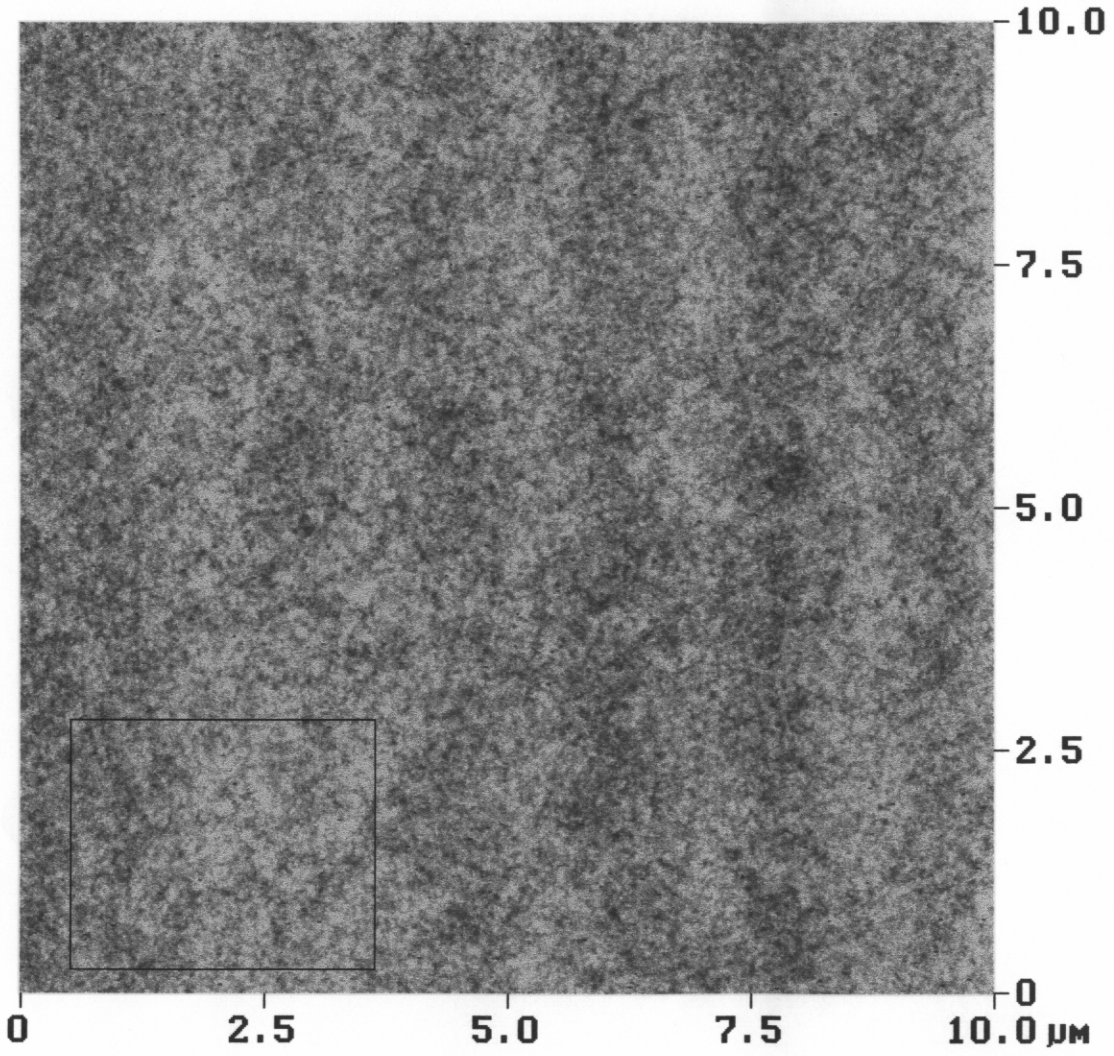

Image Statistics

Img. Z range	8.667 nm
Img. Mean	-0.000000 nm
Img. Raw mean	0.908 nm
Img. Rms (Rq)	0.389 nm
Img. Ra	0.307 nm
Img. Srf. area	100.03 µm²
Img. Prj. Srf. area	100.00 µm²

Box Statistics

Z range	6.291 nm
Mean	0.080 nm
Raw mean	6.792 nm
Rms (Rq)	0.383 nm
Mean roughness (Ra)	0.303 nm
Max height (Rmax)	6.222 nm
Box x dimension	3.131 µm
Box y dimension	2.583 µm

Fig. 4. AFM image and analysis of a relaxed SiGe (15% Ge) film with 700 nm PECVD oxide after polishing for 8 min.