RC 21915 (98559) 19 December 2000 **Physics**

IBM Research Report

Low-Voltage Electron Transport in Self-Assembled Nanocrystal Arrays

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ABSTRACT

Electrons traverse two-dimensional nanocrystal arrays by sequential tunneling between neighboring nanocrystals. Analysis of array conductance at zero bias-voltage gives information about underlying nanocrystal uniformity, as well as the relevant single-electron charging energy. We discuss low-temperature measurements of two-dimensional self-assembled superlattices composed of 10 nanometer diameter cobalt nanocrystals, with ~2 nm inter-nanocrystal spacing.

INTRODUCTION

Electron transport through two-dimensional (2D) arrays has long been a subject of experimental interest. The body of experimental work in this area can be broadly separated into two categories, based on the method of sample fabrication. In one case it is possible to fabricate 2D arrays using lithographic means (for example, [1, 2]). In these experiments, array properties are controlled precisely, however dimensions are restricted to larger than ~100 nm. In another experimental realization, electronic conduction in metallic granular thin-films can be understood in terms of a highly non-uniform array [3, 4]. In this system the characteristic length scale can be on ~1-10 nm (the average grain size in the film), however array properties such as number of nearest neighbors and intergrain spacing are not well-controlled. By using self-assembly of chemically-synthesized nanocrystals, we combine the precision of lithographically-defined arrays with the nm size-scale of granular thin films. We discuss the low-voltage conductance of our devices, and its relationship to the uniformity of our nanocrystal building blocks.

EXPERIMENT

A full discussion of fabrication and electrical measurements of these magnetic nanocrystal superlattices has already been detailed [5]. We fabricate our tunneling devices by first using electron beam lithography and metal liftoff of a 15 nm thick AuPd film. The resulting electrodes are roughly 100 nm wide, and are spaced ~100 nm apart (Fig. 1a). Subsequent deposition of a nanocrystal monolayer on top of the electrodes (Fig. 1b) results in a hexagonal array situated between the electrodes (as well as everywhere on the wafer). For this particular device, the shortest path between the two electrodes contains ~15 nanocrystals in series.

Nanocrystal diameters are 10 nm (±5%) in this experiment, and analysis by transmission electron microscopy (TEM) shows a 2 nm inter-nanocrystal spacing. Details of the cobalt nanocrystal synthesis can be found elsewhere [6]. We form nanocrystal monolayers using a Langmuir-Blodgett technique [7]; we deposit a drop of solvent (hexane) containing the nanocrystals onto a water surface. After the solvent evaporates, the nanocrystals remain confined to a single layer due to surface tension. We can then compress the 2D film to form large areas of

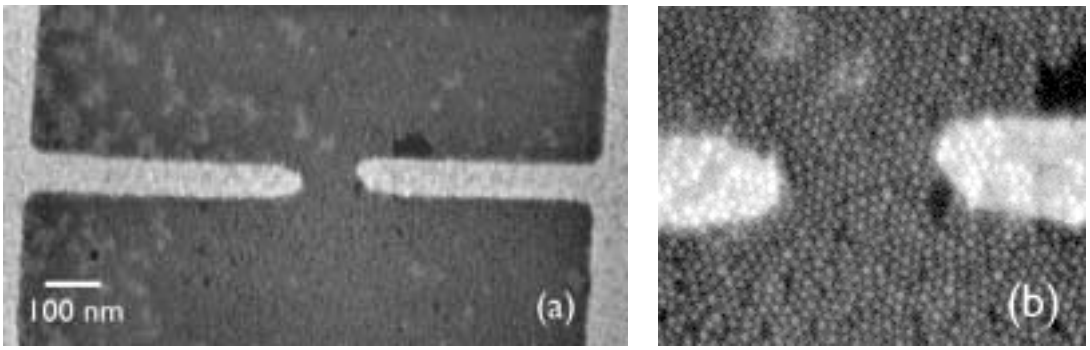

Figure 1. (a) SEM image of nanocrystal superlattice device. 100 nm AuPd electrodes are spaced ~100 nm apart. (b) Closeup of region between electrodes, showing hexagonal lattice of 10 nm diameter nanocrystals.

close-packed nanocrystal monolayer. Finally, we transfer the nanocrystal film from the water subphase by dip-coating a solid substrate.

A series of scanning electron microscope (SEM) images (Figure 2) details the nanocrystal film morphology for various stages of compression. At low surface pressures (Fig. 2a), the film contains large voids and regions of close-packed nanocrystals are only loosely interconnected. Compressing the film (Figs. 1(b)-(c)) shrinks the size of the voids. For sufficiently-high surface pressures (Fig. 1(d)), we can achieve large areas of polycrystalline nanocrystal monolayers. Notice that significant areas of nanocrystal bilayers form as we continue to compress the film.

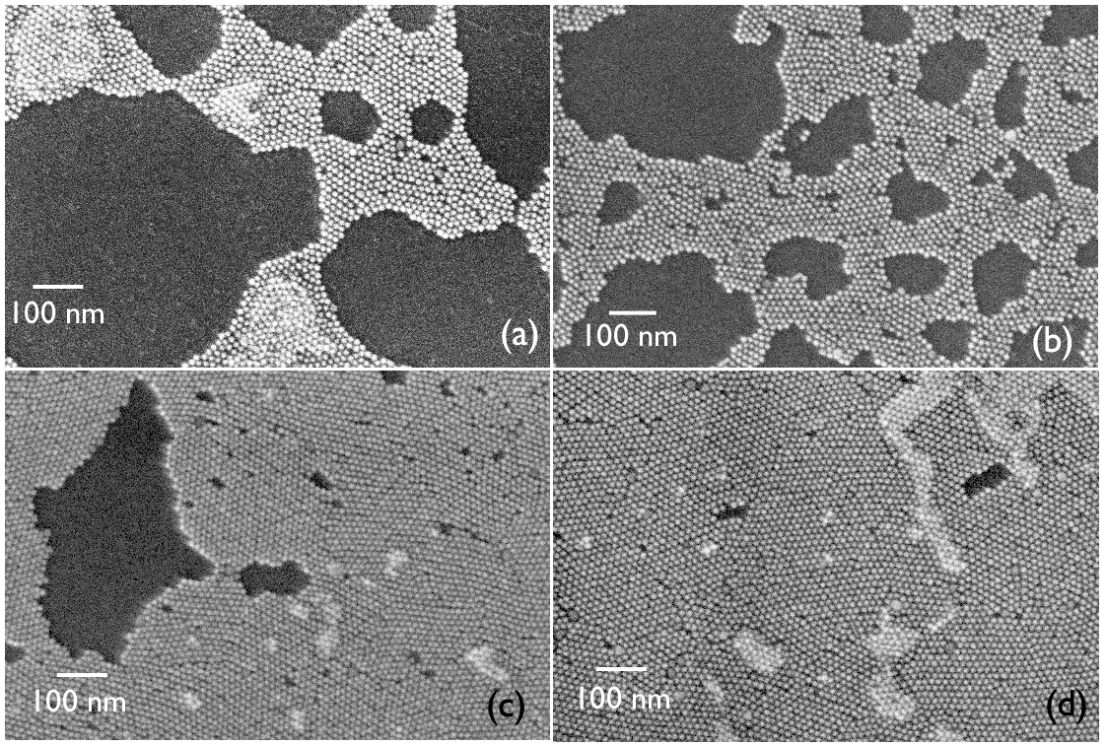

Figure 2. Nanocrystal film in various stages of compression. (a) At low surface pressure, the film contains large voids, and monolayer areas are loosely connected. (b, c) Increasing surface pressure reduces the size and number of voids in the monolayer film. (d) At sufficiently-high pressure there are large areas of close-packed nanocrystal monolayers.

The zero-bias conductance ($G_{V=0}$) of our nanocrystal-superlattice devices decreases monotonically with decreasing temperature (T). For T less then ~15K a finite voltage is required to generate any measurable current through the array. A complete Coulomb blockade of current occurs when there is insufficient energy supplied by the voltage bias for electrons to charge nanocrystals in the array [8]. In the following discussion we focus on the T-dependence of $G_{V=0}$, where the energy for electrons to overcome the Coulomb blockade is provided by temperature.

A plot of $\ln(G_{V=0})$ versus 1/T (Figure 3) elucidates the functional form of array conductance on T. For the two devices shown (and for all 10 of the devices we have measured to date), we determine a linear relationship between $\ln(G_{V=0})$ and 1/T, implying a single activation energy for tunneling electrons. As we will discuss further, we interpret the simple thermally-activated behavior, shown in Figure 3, as direct evidence of the nanocrystal uniformity in our devices.

DISCUSSION

Electrons move through the superlattice device by sequentially tunneling between neighboring nanocrystals in the array. Although the nanocrystals in our devices are all nominally the same size, it is instructive to consider the effect of a size distribution on device conductance. A model based on tunneling through an array of identically-sized and -spaced nanocrystals predicts the device conductance as [9]:

$$G_{V=0} \propto \exp\left[\frac{-U}{k_B T}\right] \qquad (1)$$

where U is the activation energy to charge an electrically-neutral nanocrystal. In this model $U \equiv e^2/2C$, where *C* is the total capacitance of the nanocrystal to its surroundings and *e* is the charge of the electron. The Arrhenius form (Eq. 1) successfully describes $G_{V=0}$ for lithographic tunnel-junction arrays [1, 2], because junction areas can be precisely defined. We estimate that for a 10 nm diameter nanocrystal with 6 nearest neighbors, U~10 meV [5]. By accounting for distributions of nanocrystal sizes and spacings it can be shown that [10, 11]:

$$G_{V=0} \propto \exp\left[-\sqrt{\frac{U^*}{k_B T}}\right] \qquad (2)$$

U* can be thought of as an average activation energy for the film, and is closely-related to U (although U is not unique in a system of different-sized islands). The $T^{-1/2}$ dependence of $G_{V=0}$ is observed in most granular metal thin-films, and is a signature of grain-size nonunifomity.

We can understand the evolution of (1) to (2) using a simplified model system. Although current paths through the array are composed of several serial tunneling events (*n+1* events, where *n* is the number of nanocrystals in the path), we will assume that the resistance of each path is dominated by a *single rate-limiting step*. As a further simplification, we assume that differences in tunneling rates are caused only by variations in nanocrystal charging energy U. Because $U \equiv e^2/2C$ and *C* is determined by nanocrystal size [5], we note that our model focuses only on the effect of a nanocrystal *size* distribution. Variations in nanocrystal spacing affect both the device activation energy and overall resistance, and are not considered here. We describe $G_{V=0}$ for any path *i* through the device as:

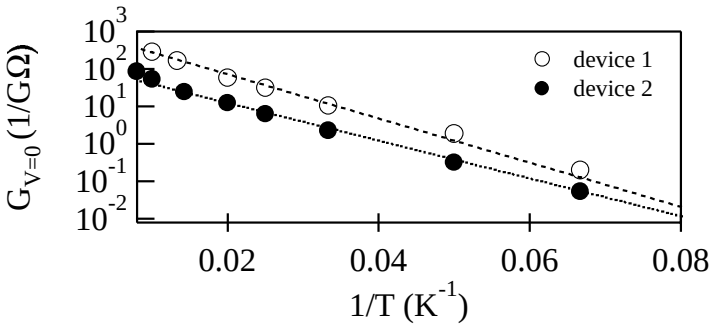

Figure 3. Plot of $\ln(G_{V=0})$ versus 1/T for two different nanocrystal superlattice devices. Dotted and dashed lines are fits of the data to an Arrhenius form.

$$G_i \propto \exp\left[\frac{-U_i}{k_B T}\right] \tag{3}$$

where U_i is the activation energy for the rate-limiting step in the path. The total device conductance is then the sum of all path conductances:

$$G_{total} = \sum G_i = \int G_i \rho(U) dU \tag{4}$$

In Eq. 4, $\rho(U)$ is the number density of conductance paths characterized by an activation energy U. If we assume a gaussian distribution for $\rho(U)$ (with mean value U_0 and width in energy σ), then the total device conductance can be written as:

$$G_{total} \propto \sqrt{\frac{1}{2\pi\sigma^2}} \int \exp\left\{\left[\frac{U-U_0}{4\sigma}\right]^2 - \frac{U}{k_B T}\right\} dU \tag{5}$$

A plot of Eq. 5 for different nanocrystal distributions shows directly their effect on $G_{V=0}$. For identical nanocrystals ($\sigma/U_0=0$), we recover the Arrhenius form (solid line). Increasing the distribution of charging energies (σ/U_0= 20%, 30%, 50% in Figure 4) creates successively higher device conductance at the lowest T. We understand this behavior by noting that current paths through the device freeze out when $k_B T<U$. Larger distributions of nanocrystal charging energies will increase the number of contributing paths (those for which $U<k_B T$) at low-T. Finally, the dotted curve in Figure 4 is a plot of Eq. 2, which is the characteristic $T^{-1/2}$ behavior of highly non-uniform systems [10, 11].

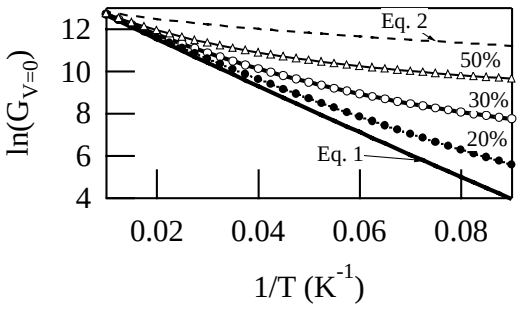

Figure 4. Effect of nanocrystal uniformity on device conductance. Calculated plots of $\ln(G_{V=0})$ versus 1/T, showing the evolution from a completely uniform array (solid line) to a highly-disordered array (dotted line). Intermediate curves show the effect of 20%, 30%, and 50% variations in nanocrystal charging energy.

CONCLUSIONS

The T-dependence of $G_{V=0}$ for our devices (Figure 3) is best described by a thermal activation process involving a single activation energy. We determine U from the slope of a theoretical fit to Eq. 1, and for the two devices shown in Figure 3 we find U=10.0 and 11.8 meV. Both of these values are in reasonable agreement with our estimate of U~10 meV [5] for a 10 nm diameter nanocrystal in a 2D hexagonal array. We have measured 10 devices composed of similar-sized nanocrystals, and in all devices we find 10<U<14 meV. The variation in U from device to device (shown in Fig. 3) results from variability in nanocrystal size and/or spacing.

We have further discussed in detail the evolution of $G_{V=0}$ for uniform systems (Eq. 1) into $G_{V=0}$ for highly non-uniform arrays (Eq. 2). Like our nanocrystal superlattice devices, this analysis based on a simplified model makes a connection between the behavior of highly-uniform lithographically-defined arrays [1, 2] and that of disordered granular thin-films [3, 4]. Estimates based on our model indicate that $G_{V=0}$ deviates measurably from Eq. 1 when nanocrystal size distribution exceeds 15 percent (10.0 ±1.5 nm).

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