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Monte Carlo Simulation of Double Gate Silicon on Insulator Inversion Layers: The Role of Volume Inversion.

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Abstract

The electron mobility in a double-gate silicon on insulator (DGSOI) device is studied as a function of the transverse electric field and silicon layer

thickness. The contributions of the main scattering mechanisms (phonon scattering, surface roughness scattering due to both $Si - SiO_2$ interfaces, and Coulomb interaction with the interface traps of both interfaces) are taken into account and carefully analyzed. We demonstrate that the contribution of surface scattering mechanisms is by no means negligible; on the contrary, it plays a very important role which must be taken into account when calculating the mobility in these structures. The electron mobility in DGSOI devices as T_w decreases is compared with the mobility in Single-Gate Silicon On Insulator (SGSOI) structures, i) when only phonon scattering is considered; ii) when the effect of surface roughness scattering is taken into account, and iii), when the contribution of Coulomb interaction with charges trapped at both interfaces is taken into consideration (in addition to phonon and surface roughness scattering). From this comparison, we determined (in the three cases above) the existence of the following three regions: i) A first region for thick silicon layers ($T_w > 20 - 30nm$), where mobility for both structures tends to coincide, approaching the bulk value -ii) As T_w decreases, we show that volume inversion modifies the electron transport properties by reducing the effect of all the scattering mechanisms. Accordingly, the electron mobility in a DGSOI inversion increases by an important factor which depends on the silicon thickness and the transverse

effective field. iii)Finally, for very small thicknesses, the limitations to electron transport are due to geometrical effects, and therefore the two mobility curves, which again coincide, fall abruptly.

We show the existence of a range of thicknesses of silicon layer (between $5nm$ and $20nm$) in which electron mobility is improved by 25 % or more.

1. Introduction

Silicon-On-Insulator (SOI) technology is considered for future electronic technology because of the many advantages that these devices present when compared to their bulk counterparts[1],[2],[3],[4], and because of its compatibility with existing fabrication facilities. Thus, a lot of effort has been spent in recent years to study carrier transport in these devices.

In this respect, Double-Gate Metal-Oxide-Semiconductor-Field-Effect-Transistors (DGMOSFETs) are currently considered a serious alternative to standard-bulk MOSFETs to increase the integration capacity of silicon technology in the near future. A Dual-Gate-Silicon-On-Insulator (DGSOI) structure consists, basically, of a silicon slab sandwiched between two oxide layers. A metal or a polysilicon film contacts each oxide. Each one of these films acts as a gate electrode (front and back gate), which can generate an inversion region near the $Si - SiO_2$ interfaces, if an appropriate bias is applied. Thus, we would have two MOSFETs sharing the substrate, source and drain. The outstanding feature of these structures lies in the concept of volume inversion, introduced by Balestra et al.[5]: if the Si film is thicker than the sum of the depletion regions induced by the two gates, no interaction is produced between the two inversion layers, and the operation of

this device is similar to the operation of two conventional MOSFETs connected in parallel. However, if the Si thickness is reduced, the whole silicon film is depleted and an important interaction appears between the two potential wells. In such conditions the inversion layer is formed not only at the top and bottom of the silicon slab (i.e., near the two silicon-oxide interfaces), but throughout the entire silicon film thickness. It is then said that the device operates in *'volume inversion'*, i.e., carriers are no longer confined at one interface, but distributed throughout the entire silicon volume. Several authors have claimed that volume inversion presents a significant number of advantages, such as: i) enhancement of the number of minority carriers; ii) increase in carrier mobility and velocity due to reduced influence of scattering associated with oxide and interface charges and surface roughness; iii) as a consequence of the latter, an increase in drain current and transconductance; iv) decrease of low-frequency noise, and v) a great reduction in hot-carrier effects [5].

In addition, like other dual-gated devices, DGMOSFETs are claimed to be more immune to short channel effects (SCE) than bulk silicon MOSFETs and even than single gate fully depleted SOI MOSFETs. This is due to the fact that the two gate electrodes jointly control the carriers, thus screening the drain field from the channel[6]. This latter feature would permit a much greater scaling down

of these devices than ever imagined in conventional MOSFETs.

Some steps have already been taken in the theoretical study of these devices:

i) Ouisse has solved Poisson's and Schroedinger's equations self-consistently in ultrathin silicon-on-insulator structures, and has studied the interaction between the front and back inversion layers as a function of the silicon film thickness, electron concentration and temperature[7].

ii) Frank et al.[6] have performed a Monte Carlo simulation of a 30 nm gate length DGMOSFET with a channel thickness of $T_w = 5nm$. The main result of this study is that these ultrashort devices present excellent properties for use in digital logic.

iii) Shoji et al.[4],[8] have also studied the electronic structure of these devices. In addition, using a relaxation time approximation method, they have calculated the phonon-limited electron mobility in double gate devices. In particular, they have shown that in DGMOSFETs, as silicon thickness is reduced, phonon-limited mobility increases gradually to a maximum around $T_w = 10nm$, decreases in the $T_w = 5nm - 10nm$ range to values below the value this parameter presents in conventional bulk MOSFETs, rises rapidly to another maximum in the vicinity of $T_w = 3nm$ and finally falls. They have also shown that the value of these maxima strongly depends on the total electron concentration. According to these results,

the optimum thickness of the silicon layer in DGMOSFETs is around $T_w = 10nm$ (from the phonon-limited mobility viewpoint).

However, phonon scattering is not the only scattering mechanism present in these devices. Other scattering mechanisms (namely, those associated with the coulombic interaction with oxide and interface charges and with the roughness of the silicon-oxide interface) are likely to be weakened by volume inversion operation[5]. This latter is justified, at least a priori, by the spread of the electrons throughout the whole silicon region. Nevertheless, we must not forget that in order to achieve volume inversion, both channels must interact strongly, and this only happens in the medium-high transverse electric field range when the silicon slab between the two oxides is thin enough (below 20 nm as pointed out by [4],[7]).

In such thin devices, although electrons are certainly spread along the whole silicon layer, they may not be far enough from the interfaces, and therefore they may be strongly affected by surface scattering mechanisms; in fact, much more so than in bulk MOSFETs, since they now interact with two interfaces. This means that scattering mechanisms play a very important role in the electron mobility in ultra-thin DGMOSFETs, on the contrary to what was previously thought. This fact poses a serious limitation on the minimum silicon thicknesses which should

be used in these devices, in addition to the limitations already presented by other physical and technological issues, as detailed elsewhere [4],[6].

The influence of surface scattering mechanisms on electron mobility in DG-MOSFETs has not yet been studied in depth. However, in view of the above reasoning such a study is strongly required.

We used a one-electron Monte Carlo method to study the stationary electron transport properties in DGSOI inversion layers, focusing our attention on the evaluation of the stationary drift velocity and the low-field mobility at room temperature. Electron quantization in the inversion layer was appropriately taken into account, self-consistently solving Poisson's and Schroedinger's equations assuming a simple non-parabolic band model for the silicon. Once the electron distribution in the silicon layer was determined, the Boltzmann transport equation was solved by the Monte Carlo method, simultaneously taking into account phonon, surface-roughness and Coulomb scattering. To do so, it was necessary to improve upon the existing scattering models. The presence of two close silicon-oxide interfaces in a DGMOSFET is a significant difference with respect to its standard-bulk counterparts. Therefore, we had to develop a new model capable of taking into account the effect of the roughness of both interfaces on the total scattering rate. This model had been recently applied to single-gate SOI MOSFET[9]. The calculation

of mobility curves in DGSOI devices in which Coulomb scattering is accurately included is another novelty of this paper. Section 2 includes details of the numerical simulation and of the distribution of electrons in the structure and their influence on the transport properties. Section 3 provides mobility results, together with a thorough explanation. Finally, in Section 4, the main conclusions of our work are drawn.

2. Numerical simulation

The structure we have studied consists of an undoped (100)-silicon film sandwiched between two oxide layers. The oxide thickness was taken as 5 nm in both cases. Polycrystalline Si (poly-Si) gates were assumed as front and back electrodes. Different thicknesses of the silicon film (T_w), ranging from 50 nm to 1.5 nm, were considered. To evaluate accurately the electron distribution in the structure, we must self-consistently solve the Schroedinger and Poisson equations. For the sake of simplicity, calculations are made in the Hartree approximation. Although this approximation can have serious drawbacks, the results obtained in its approach do not vary significantly when the more complicated calculation procedure necessary to take into account many-body effects is used. (For a detailed discussion of this issue see Refs. [7],[10],[11]). To solve Poisson's equation we

considered a non-uniform adaptive mesh, employing an iterative-Newton scheme. The actual band-bending through the whole structure and the finite height of the barrier at the Si-SiO_2 interfaces were considered. A simple non-parabolic band model for the silicon was taken into account assuming $\alpha = 0.5\ eV^{-1}$, where α is the parameter of non-parabolicity[12]. This limited our study to low-electron energies (below 0.5 eV) . The electron effective masses were assumed to be those of bulk silicon [13]. One may well question the use of effective-mass approximation for electronic states whose spatial extent is limited to a few atomic layers. However, on the one hand, it is claimed that four or five atomic layers are enough to recover the complete bulk bandstructure, and consequently, the same effective-mass-approximation parameters; on the other hand, as pointed out by Ando et al.[10], it is thought to be the lack of knowledge about the physical parameters and uncertainties of the problem, rather than the effective-mass approximation itself, that limits the accuracy of electron mobility calculations. A detailed description of the self-consistent solution of the Poisson and Schroedinger equations can be found elsewhere [14], [15], [16], [17]. In this work, only the symmetric operation of the device has been considered, that is to say, the same bias was applied to each of the gates. Figure 1 shows the potential distribution in the structure and the electron concentration for two silicon thicknesses ($T_w = 3nm$ (a), and $T_w = 20nm$ (b))

and for two electron concentrations (solid line $N_{inv} = 1.3x10^{12}cm^{-2}$ and dashed line $N_{inv} = 8.5x10^{12}cm^{-2}$). In this case, N_{inv} is defined as:

$$N_{inv} = \int_{x_0-}^{\frac{T_w}{2}} n(z)dz \tag{1}$$

where $n(z)$ is the electron distribution, T_w the silicon thickness and x_0- the position inside the oxide where electron concentration vanishes. Note that as a consequence of the finite height of the barrier at the silicon-silicon dioxide interface, penetration of carriers inside the oxide occurs. In the case of the thinner sample, electrons are distributed throughout the silicon even for high inversion charge concentrations.

For the sake of comparison, Figure 2 shows the electron distribution for different silicon layer thicknesses at two values of the effective transverse effective field, defined in this case as

$$E_{EFF} = \frac{\int_{x_0-}^{\frac{T_w}{2}} n(z)E(z)dz}{\int_{x_0-}^{\frac{T_w}{2}} n(z)dz} \tag{2}$$

$E(z)$ being the local transverse electric field.

The front $Si - SiO_2$ interface is assumed in all cases to be located right at $z = 0$. Consequently, the position of the back interface depends on the silicon

layer thickness in each case. In order to clearly appreciate the relative position of the carriers with respect to the interface, we do not show intentionally the whole electron concentration for the thicker devices. Moreover, this could be easily reconstructed by taking into account the symmetry of the problem. We see in this figure that for the smallest silicon thicknesses, electron density distribution expands throughout the whole Si layer, and reaches a maximum at the center of this layer. However, it can also be observed that the thinner the silicon film, the greater the proximity of the electrons to the interface.

From the self-consistent solution of the Poisson and Schroedinger equations, the following conclusion can be drawn:

a) As in ultra-thin single-gate SOI MOSFETs (SGSOI), the *subband modulation effect* is an important effect caused by the reduction of the silicon film thickness[17], [18]. This effect is related to the redistribution of the carriers among the different electric subbands originated by the size-quantization[17]. The self-consistent solution of the Poisson and Schroedinger equations in a SGSOI inversion layer shows that the separation between the energy levels of the two subband ladders produced by the splitting of the degeneration of the silicon valleys, as a consequence of size quantization, increases as the thickness of the silicon layer is reduced. An important consequence of this fact is that the population of non-

primed subbands increases at the expense of the prime subband population as the silicon layer thickness is reduced[10].

For thicker samples, most of the electrons populate the ground-state subband of the primed ladder at low inversion-charge concentrations, and only at high electron sheet densities is the non-primed ladder more highly populated than the non-primed one. In this case, therefore, most of the electrons have a conduction effective mass equal to m'_c. Meanwhile, for thinner samples, the majority of the electrons populate the non-prime ladder throughout the inversion-charge concentration range, thus showing a conduction effective mass equal to m_c. Therefore, as $m'_c > m_c$, a reduction in the conduction effective mass occurs as T_w is reduced.

In DGSOI inversion layers the picture is much more complicated since we must account for the fact that, as the silicon layer is reduced, the quantum interaction between the upper and lower channels produces a modification of the subband structure, and therefore of their occupation [4], as shown in Figure 3. In the thickest slabs the two inversion layers are sufficiently separated and there is no interaction (or at least only a very slight one) between them. Therefore, in the symmetric situation considered here, the subband structure is degenerate, but the distribution of the energy levels remains as that of a bulk-silicon inversion layer. As the transverse effective field increases, the inversion layers of the thickest

DGSOI structures present the same behavior as a bulk inversion layer, that is to say, a larger separation between the energy levels of the two subband ladders, and therefore a greater population of non-primed subbands with a lower conduction effective mass.

For the thinnest samples, the situation is even more complicated. At low inversion charge concentrations, electrons are distributed throughout the silicon slab (volume inversion). In this situation, the energy level distribution is quite different from that observed in the thickest samples[4]. As the electric field increases, the silicon conduction band is bent near both Si/SiO_2 interfaces, and a potential barrier begins to appear in the middle of the silicon slab. As a consequence of this, two channels, one in the vicinity of each interface, are formed (see Figure 1). When this situation is reached, the distribution of energy levels must be similar to the thickest samples, since there is no interaction between the two inversion layers: when the effective field increases, energy levels change differently from in the thickest slabs. For example, Fig. 4 shows that for $T_w = 3nm$ the separation between the ground subbands of each ladder decreases as E_{EFF} increases, instead of increasing as it happens in the thickest samples ($T_w = 7.5nm$, dashed line). As a consequence, the average conduction mass increases as the transverse effective field increases (this behavior is different from what is expected). Figure 5 shows

the average conduction effective mass as a function of silicon thickness for different inversion charge concentrations. For thinner samples, the conduction effective mass increases as the electric field increases. However, for thicker samples, the conduction effective mass decreases as the electric field increases. Note that for $N_{inv} = 10^{13} cm^{-2}$, there is a range of T_w in which the conduction effective mass increases as T_w decreases.

b) Another important effect that appears in SGSOI inversion layers with decreasing thickness of the silicon layer is an increase of the phonon-scattering rate, i.e., the uncertainty in the location of the electrons in the direction perpendicular to the interface is lower in SOI samples than in bulk samples. By the uncertainty principle, there is a wider distribution of the electron's momentum perpendicular to the interface. In other words, due to size quantization, the electron's interface-directed momentum does not have a single value (as in 3-D electrons), but rather a distribution of likely values that expands as the silicon layer thickness is reduced. Taking into account momentum conservation, there are more bulk phonons available that can assist the transitions between electronic states, and therefore the phonon-scattering increases. Thus, for the same inversion-charge concentration, the phonon-scattering rate is greater in thinner films than in thicker ones (since the confinement is greater), and therefore we expect a reduction of the mobility.

Numerically, this effect is reflected in the following form factor

$$I_{\mu\nu} = \int_{-\infty}^{\infty} \left|\psi_{\mu}(z)\right|^2 \left|\psi_{\nu}(z)\right|^2 dz \tag{3}$$

which multiplies the phonon scattering rates [19], where $\psi_{\nu}(z)$ is the envelope of the electron wavefunction in the direction perpendicular to the interface in the $\nu - th$ subband. When confinement is greater (the overlap integral of envelope wavefunctions is also larger) the phonon scattering rate increases. In point a) above, we have seen that the energy-level distribution (and therefore the wavefunctions) of electrons in thinner DGSOI inversion layers is quite different from the energy-level distribution in thicker films and, therefore, it is also different from those in SGSOI inversion layers.

The above form factor plays an important role in the transport properties of electrons in inversion layers since it is the dominant factor determining the phonon scattering rate. Figure 6 shows the form factor for the ground subband as a function of silicon thickness for two different values of the transverse effective field. The form factor corresponding to SGSOI inversion layers is also shown(dashed line).[20]. For thinner samples, the form factor is very large, due to the geometrical confinement of electrons in a very narrow space (no differences are

observed between DGSOI and SGSOI). As the silicon slab thickness increases, the form factor is quickly reduced, until a minimum is reached in the region between $5nm - 15nm$. Then, it increases to approach, for thick samples, ($T_w > 20nm$), the value presented in SGSOI inversion layers (and in bulk inversion layers). As can be seen in the figure, in the range $T_w = 5nm \rightarrow 15nm$ the form factor for DGSOI is lower than the one corresponding to SGSOI for the same thicknesses, and even lower than the one corresponding to bulk inversion layers ($T_w \rightarrow \infty$). Consequently, in the range ($T_w = 25nm \rightarrow 5nm$, for $E_{EFF} = 1x10^5 V/cm$; and $T_w = 15nm \rightarrow 5nm$, for $E_{EFF} = 5x10^5 V/cm$) the phonon scattering rate in DGSOI inversion layer decreases, instead of increasing as expected.

This is an important result, a direct consequence of the volume inversion effect. This fact is important in explaining the behavior of the transport properties, in the next section.

3. Electron Mobility

To study electron mobility behavior in ultrathin DGSOI inversion layers, we used a one-electron Monte Carlo simulator [14], [15].

Phonon, surface-roughness and Coulomb scattering have been taken into account in this work. We used bulk electron-phonon scattering models considering

acoustic deformation potential scattering and intervalley scattering (both between equivalent and non-equivalent valleys). The coupling constants for the intervalley phonons and the acoustic deformation potential are the same as in bulk silicon inversion layers [11], [13]. The phonon-scattering rates for inversion layers were deduced by using Price's formulation [19]. Here again, the use of bulk phonons is questionable, as the presence of Si-SiO_2 interfaces undoubtedly alters the dispersion of the phonons, their nature and their coupling to the electrons. Previous studies [21] accounting for these effects in idealized conditions showed that phonon-limited mobility is reduced by 20 % or less [11] due to the presence of the Si/SiO_2 interfaces. Nevertheless, if such idealized conditions are relaxed, an even lower reduction is expected. For these reasons and due to the difficulty in dealing with the effects of the interfaces on the phonon-scattering rate [11], [21], we have assumed that the bulk phonons are not influenced by the layered structure. In any case, the presence of the two Si/SiO_2 interfaces becomes more important as the silicon layer thickness is reduced. This effect is to be the object of future studies. Finally, the effect of SiO_2 polar-phonon remote scattering has also been ignored.

In this simulation the electron energy was limited to 0.5 eV, since for higher electron energies the results obtained by the simulation are not likely to be very

accurate, as a detailed bandstructure was not used. Accordingly, as the silicon bandgap was set to 1.12 eV at room temperature (thus setting the energy threshold for the impact ionization process), impact ionization was not included.

By using this simulator, we were able to calculate the electron mobility in DGSOI inversion layers for different silicon film thicknesses (T_w). Our attention was focused on evaluating the stationary drift velocity and the low-field mobility. A comprehensive description of this simulator can be found elsewhere [9],[14],[17],[22],[23].

3.1. Phonon scattering

Figure 7 shows electron mobility curves versus the transverse effective field for different silicon layer thicknesses, calculated at room temperature and taking into account only phonon scattering. For comparison, the electron mobility in a bulk silicon inversion layer at room temperature is also shown. It can be observed in this figure that there is more than one trend in electron mobility as the silicon slab thickness is reduced and that, in addition, this behavior strongly depends on the value of the electric field. To illustrate this more clearly, Fig. 8 shows the electron mobility versus silicon layer thickness for two different electric field values. Also shown are the mobilities corresponding to SGSOI inversion layers. Basically,

our Monte Carlo results reproduce, qualitatively, the results obtained by Shoji et al.[4],[8] for DGSOI inversion layers using the relaxation time approximation.

As silicon thickness is reduced, the phonon-limited mobility increases gradually to a maximum around $T_w = 10nm$ (for $E_{EFF} = 1x10^5 V/cm$), decreases in the $T_w = 5nm - 10nm$ range to values below those of this parameter in conventional bulk MOSFETs, rises rapidly to another maximum in the vicinity of $T_w = 3nm$ and finally falls. For higher electric fields, mobility maximum is smaller and is shifted to lower Si thicknesses.

A comparison between the phonon-limited mobility curves relative to DGSOI inversion layers (solid lines) and those corresponding to SGSOI inversion layers (dashed lines) in Fig. 8, reveals the existence of three regions of different behavior:

i) The first region corresponds to thick silicon slabs. In DGSOI inversion layers the two channels are sufficiently separated and no interaction appears between them. This situation corresponds to two conventional inversion layers in parallel, separated by a large potential barrier. The behavior of electrons in each of these inversion layers is the same as that observed in a bulk silicon inversion layer. As a consequence, the electron mobilities in DGSOI and SGSOI inversion layers coincide. As the silicon thickness is reduced, the interaction of the two inversion layers causes the electrons to occupy the entire silicon volume. This does not

happen in SGSOI (where only one inversion layer exists) and therefore mobility curves begin to differ. This is the beginning of the second region, which strongly depends on the value of the transverse effective field, since for high electric fields a potential barrier, which obstructs the mutual influence of the two channels, is formed in the middle of the silicon slab.

ii) In the second region, the electron mobility in DGSOI inversion layers is larger (up to 20%) than the mobility in SGSOI inversion layers. The limits of this region and the values of the mobility depend on the electric field considered. This is the region in which volume inversion occurs. In section 2 above, we have seen that both energy levels and wavefunctions vary significantly as a consequence of the mutual interaction of the two channels. This is the reason why the form factor (Eq.3) (and therefore the phonon scattering rate) is lower in this region (see Fig. 6). This happens down to a certain value of silicon thickness. For lower thicknesses, although the electrons are distributed throughout the entire silicon layer, their confinement is greater (due to the geometrical confinement), and therefore, the form factor and the phonon scattering rate increase, as shown in Fig. 6. This marks the beginning of the third region.

iii) In the third and last region ($T_w < 4nm$), the mobilities for DGSOI and SGSOI inversion layers again coincide. In this zone, the mobility is limited by the

thickness of the silicon slab; that is to say, limitations to mobility are imposed by the geometrical confinement of the carriers. The limits of this region do not depend on the transverse electric field. In fact, the electron mobility in this region is hardly modified by the transverse electric field. As can be appreciated in the mobility curves of Fig. 8, the electron mobility abruptly increases in the range $4nm \rightarrow 3nm$. This fact is a little surprising since, as stated above, the form factor and the phonon scattering rate were expected to increase. However, the sharp increase in electron mobility can be understood by taking into account the results shown in Figures 3 and 6. In Figure 6, it is shown that from $T_w = 4nm$ to $T_w = 3nm$ the form factor (and therefore the phonon scattering rate) increases by about 20% (as expected from the discussion above). However, Figure 3 shows that the relative population of the non-prime ladder (where electrons have a lower conduction effective mass) also increases by more than 30%, reaching almost 90% of the total. Thus we have two diverging trends, and in the case $T_w = 4nm \rightarrow 3nm$, the reduction in the conduction effective mass dominates over the increase in the phonon scattering rate. As a consequence, mobility increases. When a smaller silicon slab is considered, the increase in the phonon scattering rate is larger than the reduction in the conduction effective mass, and therefore the electron mobility abruptly falls.

Thus far, we have seen that the volume inversion operation increases the electron mobility by up to 20 %. Nevertheless, phonon scattering is not the only scattering mechanism in a silicon inversion layer. We have seen in Section 2 that in a DGSOI structure and in certain conditions, electrons are spread throughout the silicon volume. However, we have also seen that in order for this to happen the silicon slab has to be so narrow that electrons are very close to the interfaces and therefore must be affected by surface scattering mechanisms, namely surface roughness and Coulomb scattering due to the charges trapped at the $Si - SiO_2$ interface. The question now is to determine how these scattering mechanisms affect the mobility, and whether the volume inversion plays a role, by modifying the contribution of the surface scattering mechanisms to the total scattering rate.

3.2. Surface Roughness Scattering

If the scattering mechanisms related to the presence of the Si-SiO_2 interface significantly affect the electron transport properties in bulk silicon inversion layers [11],[24],[25] one can easily understand that this effect should, at least a priori, be taken into account in those physical systems where electrons are simultaneously affected by two such Si-SiO_2 interfaces. This is the case of the ultrathin DGSOI inversion layers studied here.

It has recently been proved that in ultra-thin SGSOI inversion layers the presence of a second interface plays a very important role, both by modifying the surface roughness scattering rate due to the gate interface, and by providing a non-negligible scattering rate[9]. On the other hand, the usual surface roughness scattering model in bulk silicon inversion layers has been shown to overestimate the effect of surface roughness scattering arising from one of the interfaces as a consequence of the presence of the other. Therefore, it was necessary to improve the surface roughness model in order to calculate the scattering rate due to both interfaces (which are assumed not to be correlated [26]). Such a model is detailed in Ref.[9]. Although that model was developed for SGSOI devices, no assumption was made explicitly involving such a structure. This means that the model is a general one and therefore may be applied to the case of the DGSOI devices considered here. In order to evaluate the scattering rate due to the roughness of an interface, we only need to know the perturbation to the potential well in the direction perpendicular to that interface, $\Delta V_m(z)$, caused by a displacement Δ_m of that interface from an ideal plane (Δ_m being the rms value of the interface roughness). Given $\Delta V_m(z)$, the surface-roughness scattering rate for an electron with wavevector $\mathbf{k}$ in the μ-subband and final state in the ν-subband is given by:

$$\frac{1}{\tau_{SR}(\mathbf{k})} = \frac{m_d e^2 \left|\int \psi_\nu(z) \frac{\Delta V_m(z)}{\Delta_m} \psi_\mu(z) dz\right|^2 \Delta_m^2 L^2}{2\hbar^3} \int_0^{2\pi} \frac{d\theta}{\epsilon(q)\left(1+\frac{L^2 q^2}{2}\right)^{3/2}} \tag{4}$$

$$q^2 = 2k^2 (1 - \cos\theta) \tag{5}$$

where $\epsilon(q)$ takes into account the effect of screening [27]:

$$\epsilon(q) = 1 + \frac{e^2 m_d}{2\epsilon_s q \pi \hbar^2} F(q) \tag{6}$$

and

$$F(q) = \sum_m \int dz \int dz' \left|\psi_m(z)\right|^2 \left|\psi_m(z')\right|^2 e^{(q|z-z'|)} \tag{7}$$

In equation 12, $\psi_\nu(z)$ is the envelope of the electron wavefunction in the subband $\nu - th$, e the electron charge, m_d the density of state effective mass in the final valley after the scattering event, and L the autocovariance length of the roughness fluctuations.

By using this model, we have calculated mobility curves in DGSOI structures for different thicknesses of the silicon slab (Figure 9). ($\Delta_{m1} = \Delta_{m2} = 0.25nm$,

$L_1 = L_2 = 1.5nm$). We can see the effect of the surface roughness at high transverse effective fields, where mobility decreases as the transverse effective field increases. Here again, we observe that there is no clear trend of electron mobility as the silicon slab thickness is reduced. Figure 10 shows the variation of the mobility versus silicon thickness for two values of the transverse electric field. For comparison, mobilities corresponding to SGSOI inversion layers are also shown.

The first feature to note is that mobility curves fall significantly as a consequence of the contribution of surface roughness scattering. This confirms that the role played by this scattering mechanism is very important and must be taken into account.

Secondly, the structure of the three regions detailed for phonon-limited mobility is also valid here: There exists a region for large T_w, where no interaction between the two channels is produced, and mobility curves for DGSOI and SGSOI coincide.

In the second region, (intermediate values of T_w) electron mobility of DGSOI inversion layers is greater than that corresponding to SGSOI inversion layers (up to 25% at $E_{EFF} = 5x10^5 V/cm$, and up to 100% at $E_{EFF} = 1x10^6 V/cm$. This is the region where the volume inversion occurs. Although the upper limit in this

region depends on the transverse electric field considered, we could say this region lies between $3nm < T_w < 15nm$. In the section above devoted to phonon-limited mobility, we saw that phonon scattering was reduced in this region. The mobility values shown in Figure 10 suggest that the surface-roughness scattering is also reduced in this region as a consequence of the spread of electrons throughout the silicon volume(volume inversion). To clarify this fact, we calculated the perturbation Hamiltonian due to a displacement of one of the interfaces of $\Delta_m = 0.25nm$, and the scattering matrix element[9]:

$$|M_{\mu\nu}(\mathbf{q})|^2 = |\langle \nu, \mathbf{k}\, | H_{SR} | \, \mu, \mathbf{k}' \rangle|^2 = e^2 \left| \int \psi_\nu(z) E(z) \psi_\mu(z) dz \right|^2 \frac{\pi \Delta_m^2 L^2}{\left(1 + \frac{q^2 L^2}{2}\right)^{3/2}} \quad (8)$$

A DGSOI inversion layer with $T_w = 10nm$ was considered. These results were compared to those obtained for the same displacement of one of the two interfaces in a SGSOI inversion layer of the same thickness (Figure 11). It can be seen that the perturbation Hamiltonian and, therefore, the scattering matrix element are lower in the case of a DGSOI structure. We conclude that in this region the surface-roughness-limited mobility is also improved as a consequence of volume inversion.

Finally, for $T_w < 3nm$, the electron mobility curves of both structures again coincide. In this region, controlled by geometric effects, the mobility decreases abruptly, and we do not see the abrupt growth in phonon-limited mobility observed in Figure 8.

3.3. Coulomb scattering

Finally, the effect of the Coulomb scattering due to the charges trapped at the $Si - SiO_2$ interfaces was considered. Figure 12 shows mobility curves for different silicon slab thicknesses versus the transverse effective field. The same interface charge concentration, N_{it}, has been assumed in both interfaces. ($N_{it} = 5x10^{10}cm^{-2}$). When Coulomb scattering is considered, it is the main scattering mechanism at low inversion charge concentrations (low transverse effective field) rather than phonon scattering. Here again, it is necessary to note the effect of surface scattering mechanisms on DGSOI mobility. Even for such a low interface trap concentration, Coulomb scattering significantly reduces electron mobility (mainly at low transverse effective fields), as a consequence of a weak screening of charged centers. As the effective field increases, the Coulomb scattering rate is reduced by the effect of the screening of scattering charge centers by the electrons themselves. As seen, Coulomb scattering has to be taken into account if we want to accurately

obtain the electron mobility in these devices.

We have used Matthiessen's rule to isolate the effect of Coulomb scattering, and thus to see the effect of the silicon slab thickness. Figure 13 shows the Coulomb limited mobility for two values of T_w and two different interface charge concentrations. From this figure the following facts can be observed:

i) As the electric field increases, the Coulomb-limited mobility increases due to the screening of the charged centers by the carriers in the channel.

ii) For larger N_{it}, the Coulomb-limited mobility is lower as a consequence of a stronger Coulomb interaction.

iii) The Coulomb-limited mobility increases more quickly for smaller T_w. This means that screening is more effective for thinner silicon slabs. Here again, volume inversion plays an important role.

We have also compared the electron mobility in DGSOI and in SGSOI inversion layers when the contribution of Coulomb scattering is considered. Fig. 14 shows the total electron mobility as a function of the silicon layer thickness for both DGSOI (solid line) and SGSOI (dashed line) inversion layers. In this figure the electric field was assumed to be $E_{EFF} = 5x10^4 V/cm$ (small enough so that Coulomb scattering was not screened by the other scattering mechanisms). For higher values of the transverse electric field, the picture is similar to that shown

in Figure 10.

As seen, the shapes of the curves are similar to the ones observed in Figure 8, when only phonon scattering was taking into account. Therefore we can still refer to the three regions detailed above. Nevertheless, the differences between the electron mobility for both types of structures are greater in this case in the volume inversion region (region ii). This is due to a more efficient screening of the trapped centers by the carriers in the DGSOI structure, which agrees with the third comment we made regarding Fig. 13.

4. Summary

We have studied the electron mobility behavior in double-gate silicon on insulator silicon inversion layers, and compared it to the mobility in single-gate silicon on insulator devices. In this study, the effects of phonon scattering, surface roughness scattering, and finally, Coulomb scattering were taken into account. The role played by each scattering mechanism was carefully analyzed as a function of silicon slab thickness and transverse effective field. Our Monte Carlo results reproduce the phonon-limited electron mobility in the relaxation time approximation shown by Shoji et al.. We have demonstrated that the contributions of surface scattering mechanisms are by no means insignificant.

The electron mobility in DGSOI devices as T_w decreases was compared with the mobility in SGSOI structures, i) when only phonon scattering was considered; ii) when the effect of surface roughness scattering was taken into account (in addition to phonon scattering), and finally, when the contribution of Coulomb interaction with the charges trapped at the interfaces was also taken into consideration (in addition to phonon and surface roughness). We have thus determined (in the three cases above) the existence of the three following regions:

- A first region for thick silicon slabs ($T_w > 20 - 30nm$), where mobility for both structures tends to coincide. For these thicknesses, an inversion layer near each interface is formed. Electrons in these inversion layers behave as they do in bulk or SGSOI inversion layers.

-As T_w decreases, an interaction between the two inversion layers is produced. As a result, the subband structure and wavefunctions are strongly modified with respect to bulk silicon inversion layers. As a consequence, electrons are spread throughout the silicon volume (volume inversion). We have shown that volume inversion modifies the electron transport properties by reducing the effect of all the scattering mechanisms. Accordingly, electron mobility in a DGSOI inversion is increased significantly. This increase depends on the silicon thickness and on the transverse effective field.

-Finally, for very small thicknesses, the limitations on electron transport are due to geometrical effects, and therefore the mobility in SGSOI and in DGSOI inversion layers, which again coincide, fall abruptly. This fact poses a serious limit to the minimum silicon thickness which can be used in these structures. Taking into account the contribution of the main scattering mechanisms, this limitation was estimated to be around 5 nm.

In conclusion, we have shown that there exists a range of silicon layer thicknesses in which electron mobility in DGSOI inversion layers is significantly improved as compared to bulk-silicon or SGSOI inversion layers.

5. Acknowledgments

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6. References

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6.1. Figure Captions

Figure 1.- Potential well and electron distribution in a DGSOI inversion layer for two different inversion charge concentrations: (solid line $N_{inv} = 1.3x10^{12}cm^{-2}$ and dashed line $N_{inv} = 8.5x10^{12}cm^{-2}$). The oxide thickness was assumed to be 5nm.

Figure 2.- Electron distributions for different thicknesses of the silicon slab in a DGSOI structure. Two different effective electric field values were considered.

Figure 3.- Relative population of each subband ladder versus the transverse effective field for different silicon layer thicknesses of DGSOI inversion layers.

Figure 4.- Energy difference between the ground subband of the two ladders versus the transverse effective field for two silicon slab thicknesses: solid line: $T_w = 3nm$, dashed line: $T_w = 7.5nm$

Figure 5.- Evolution of the average conduction effective mass with the silicon slab thickness, for different inversion charge concentrations.

Figure 6.- Evolution of form factor for the ground subband as a function of the silicon thickness for two values of the electric field. Solid line: for a DGSOI inversion layer; Dashed line: for a SGSOI inversion layer.

Figure 7.- Phonon-limited mobility in a DGSOI versus the transverse effective field for different thicknesses of the silicon slab.

Figure 8.- Evolution of phonon-limited mobility for a DGSOI (solid line) and a SGSOI (dashed line) with the thicknesses of the silicon layer. Two different values of the electric field were considered.

Figure 9.- Electron mobility curves in a DGSOI versus the transverse effective field for different thicknesses of the silicon slab. Only phonon and surface-roughness scattering were taken into account.

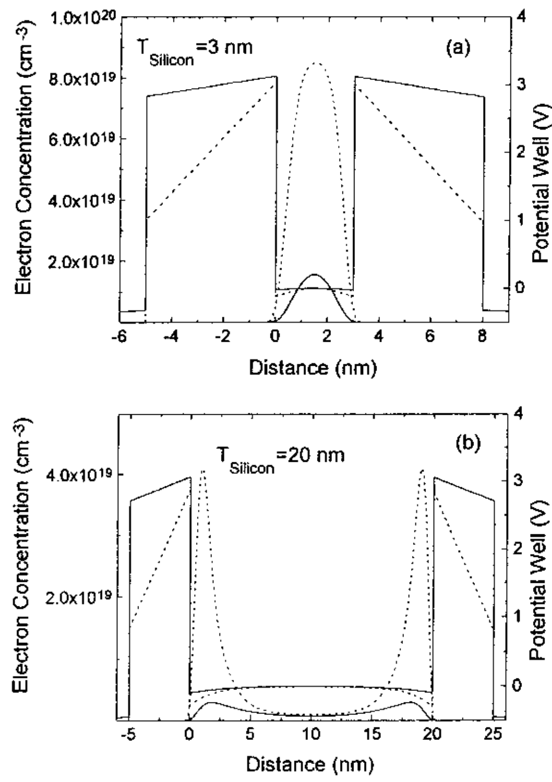
Figure 10.- Evolution of electron mobility for a DGSOI (solid line) and a SGSOI (dashed line) with the thicknesses of the silicon layer. Two different values of the electric field were considered. Only phonon and surface-roughness scattering were taken into account.

Figure 11.- (a) Perturbation Hamiltonian due to the Δ_m displacement of one of the interfaces of a DGSOI structure inversion layer from an ideal plane (solid line). Idem for a SGSOI structure (dashed line). (b) Matrix element $|M_{00}(\mathbf{q})|^2$ for surface roughness scattering. (solid line - DGSOI ; dashed line - SGSOI)

Figure 12.- Electron mobility curves in a DGSOI versus the transverse effective field for different thicknesses of the silicon slab. Phonon, surface roughness and Coulomb scattering were all taken into account.

Figure 13.- Coulomb limited mobility obtained by applying Matthiessen's rule to the mobility curves of Figure 12.

Figure 14.- Evolution of electron mobility for a DGSOI (solid line) and a SGSOI (dashed line) with the thicknesses of the silicon layer. All the scattering mechanisms were taken into account.



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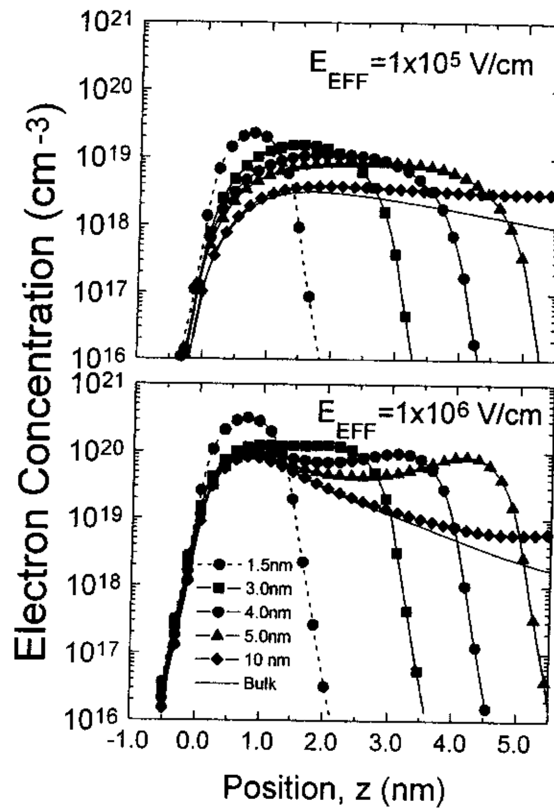

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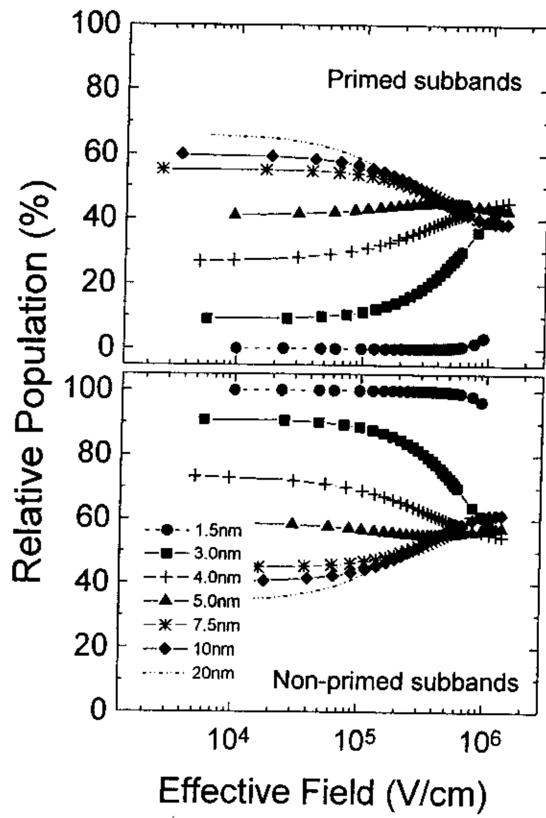

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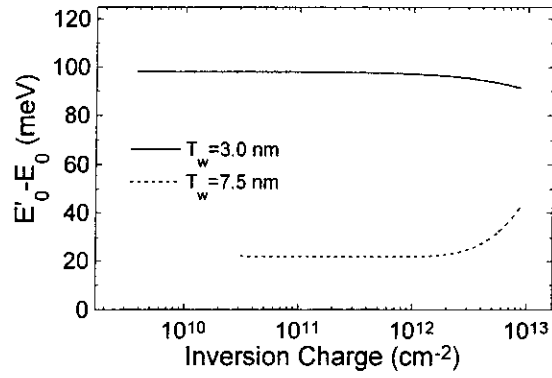

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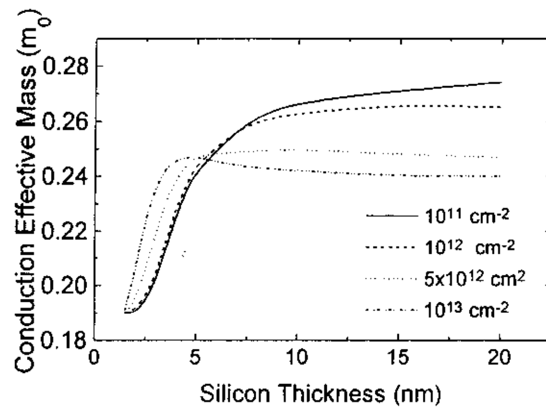

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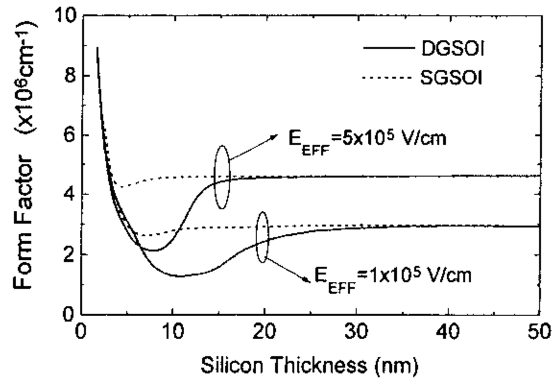

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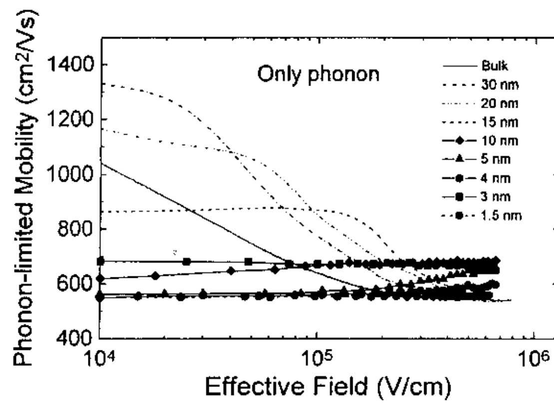

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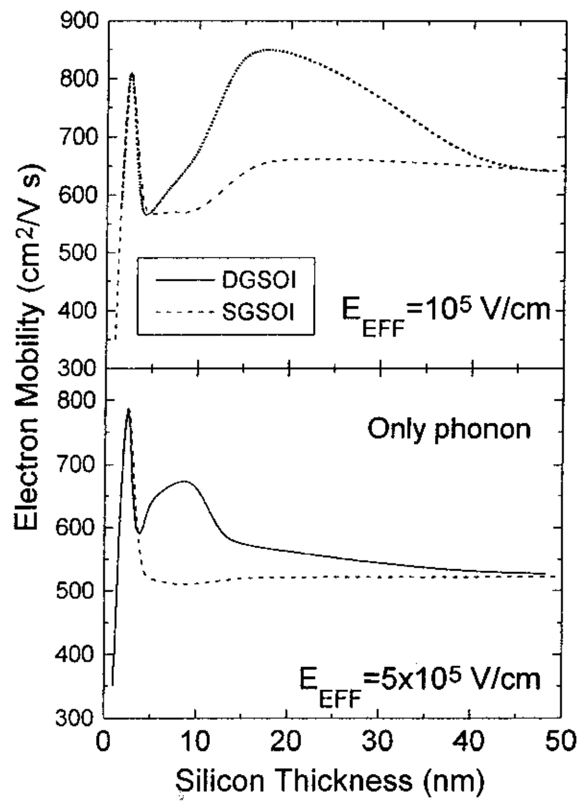

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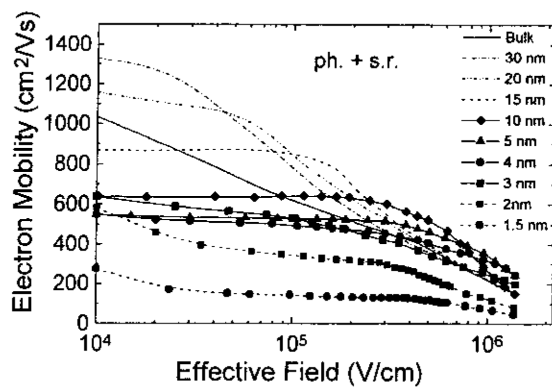

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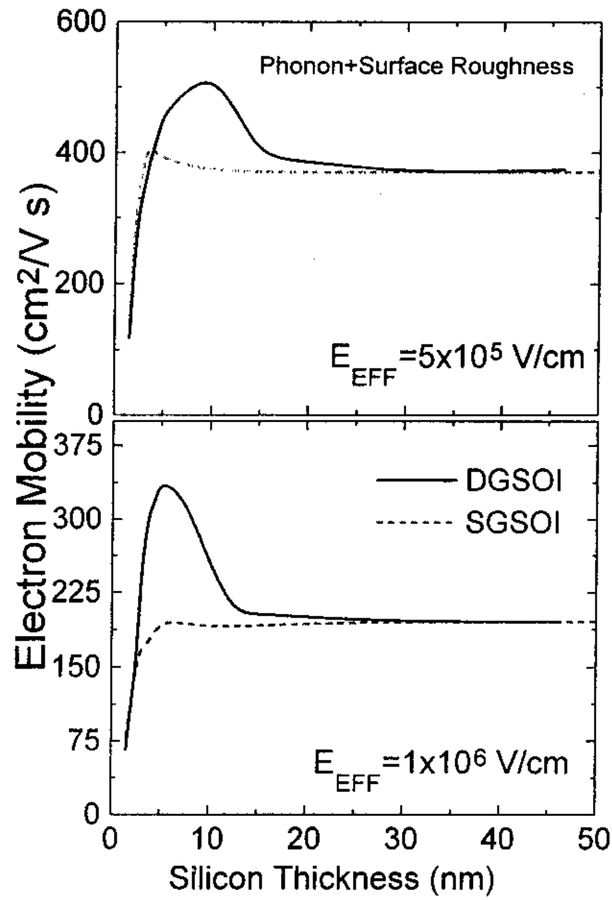

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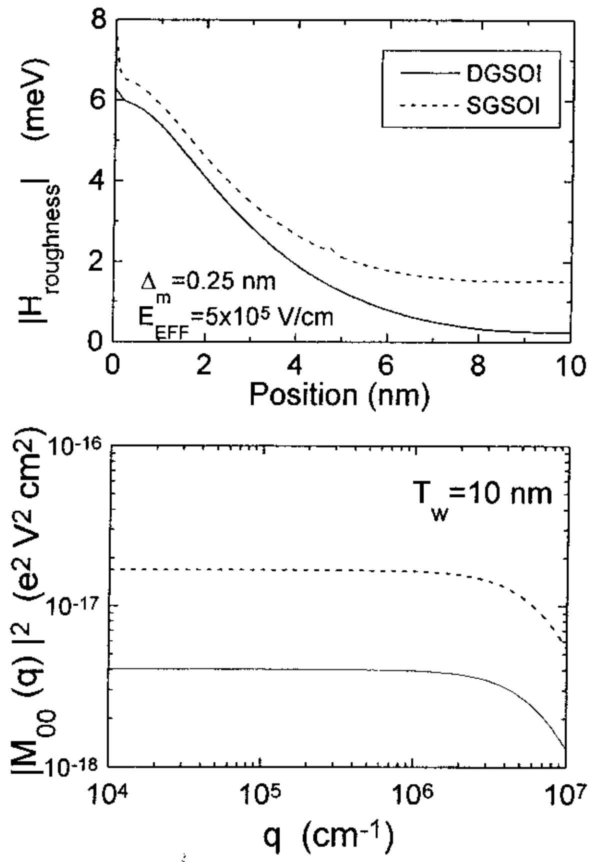

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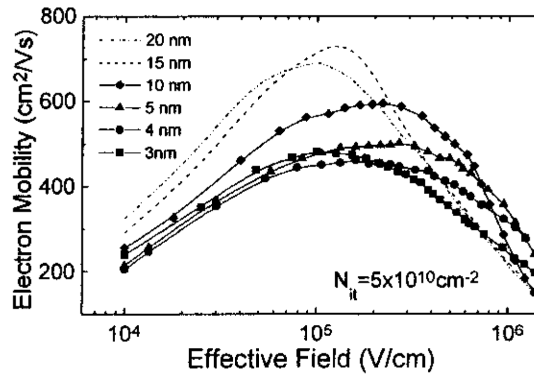

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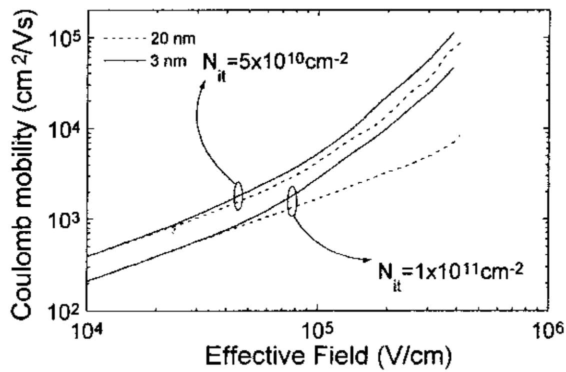

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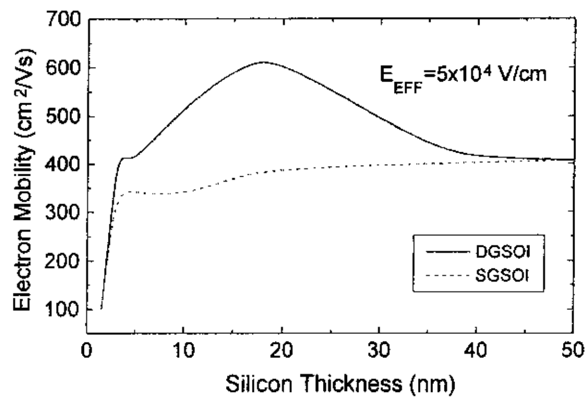

Figure 6.14: