13.7. Hydrogenated and fluorinated diamondlike carbon as the interconnect dielectric for VLSI chips.

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A. INTRODUCTION

The signal delay along the back end of the line (BEOL) interconnect structure of a VLSI circuit is controlled by the RC of the structure which, at a certain metallization level, is given by:

$$RC=2\rho k(4L^2/P^2+L^2/T^2)$$

where R is the resistance of the metal line, C the line capacitance, L the line length, P the metal pitch, T the metal line thickness, ρ metal resistivity and k the dielectric constant of the insulator between the lines. The continuous shrinking of the dimensions of the electrical devices in the VLSI circuits results in reduced P and T and increased RC delays of the electrical signals. The switching performances of the circuit can be improved by replacing the insulators with materials having lower dielectric constants than the historically used SiO_2 (k=4). The reduced capacitance will also reduce the power consumption of the device which is given by:

$$Power=CV^2f$$

where V and f are the operating voltage and frequency of the circuits.

Diamondlike carbon (DLC) has found a variety of applications based on its attractive mechanical, tribological, optical and chemical resistance properties [1,2]. The materials are also dielectrics whose electrical resistivities can reach values of 10^{16} Ω.cm at low fields. The DLC type materials are attractive dielectrics because of their isotropic properties and the ability to deposit them by plasma enhanced CVD (PECVD) techniques.

The integration of a new low-k dielectric material in a VLSI device imposes a significant number of requirements that such a material has to satisfy, among which are: low-k, low leakage current, and low dissipation factor, thermal stability at 400 °C, low stresses, minimal Young's modulus and minimal hardness, adhesion and compatibility with other materials, patternability, chemomechanical polishing (CMP) capability [3].

Hydrogenated diamondlike carbon (DLC) films, typically prepared as a wear and corrosion resistant coating, can be modified by the adjustment of the PECVD deposition conditions to obtain materials with lower dielectric constants than SiO_2 Incorporation of fluorine in DLC (FDLC) films further reduces their dielectric constant. The properties of low-k DLC and FDLC films and the ability to integrate them in VLSI devices will be discussed next.

B. EXPERIMENTAL

The low-k hydrogenated DLC and fluorinated DLC (FDLC) films discussed here have been prepared by RF plasma assisted CVD (PACVD) in a parallel plate reactor using a 13.56 MHz rf power supply. The deposition was performed on Si substrates placed on the powered electrode,

thus being at a negative self bias. The deposition was performed at pressures of 100 to 300 mtorr and negative substrate bias in the range of 80 V to 300 V. The hydrogenated DLC films were deposited from a pure hydrocarbon, while the FDLC films were deposited from fluorinated hydrocarbon ("fluorocarbon" in the following), or mixtures of the fluorocarbon with hydrogen. FDLC films have also been prepared from mixtures of fluorocarbons with hydrocarbons in PECVD or in high density plasma systems [4-6].
The thermal stability of the investigated materials was initially investigated by measuring changes of film thickness as result of annealing. It was, however, found that negligible thickness reductions or even thickness increases can be associated with significant material loss during annealing. The characterization of the thermal stability was, therefore, subsequently supplemented with measurements of material loss by Rutherford backscattering (RBS) analysis [7]. The RBS spectra were used to calculate the density of atoms in the deposited films, before and after annealing and the change in mass during annealing was calculated from these values. The dielectric constants were measured at 1 MHz, on MIS Al/xDLC/Si (xDLC=DLC or FDLC) capacitors fabricated on 0.002 Ω-cm, n-type Si substrates. Details of the electrical characterization techniques can be found elsewhere [8].

C. RESULTS AND DISCUSSION

C.1. FDLC

Fluorinated FDLC films deposited from the pure fluorocarbon can have fluorine concentrations up to 42%, a values which may be too high, with the potential to cause reactions of F with the materials in contact with the FDLC layers in the BEOL interconnect structure. Dilution of the fluorocarbon precursor with hydrogen decreased the fluorine concentration in the films down to 20%, with the hydrogen concentration increasing up to 12% [7]. However, the incorporation of H in the films caused an increase of the dielectric constants of the as-deposited films from 2.6 for [H]=0% to 3.2 for [H]=12%. Thus, in order to obtain FDLC films with low k values, the hydrogen dilution has to be kept low. Addition of argon to the precursor mixture can improve film uniformity and growth rates, without affecting adversely the dielectric constant or the intrinsic stresses which were less than 200 MPa and almost independent on precursor mixture or substrate bias [7]. The as-deposited FDLC films were thermally unstable and had thickness change in the range from -2.5% to about +4% and mass losses in the range of -20% to - 7% after a first anneal of 4 hours at 400 ^{o}C. After a second anneal at 400 ^{o}C the thickness changes was within the experimental error of about 1%. The mass losses after the second anneal were significantly lower than after the first anneal and, for certain deposition conditions, they were within the experimental errors [7]. Addition of Ar to the precursor mixture improved the thermal stability of the FDLC films. It thus appeared that FDLC films deposited from fluorocarbon diluted with hydrogen and argon can be stabilized by an initial anneal at 400 ^{o}C and remain apparently stable to subsequent anneals at same temperature.
The dielectric constant of the apparently stabilized FDLC films is in the range of 2.4 - 2.6. The leakage current though these films is about $2x10^{-8}$ A/cm^2 at an operating field of 0.5 MV/cm [7].

The integration of the low-k FDLC films in a BEOL interconnect structure requires good adhesion of FDLC to other Si based dielectrics, such as silicon oxide, silicon nitride, and to metals, such as Ta. The adhesion between FDLC and these materials has been investigated for layered structures Si/FDLC/X (described from bottom to top in this notation) with X=SiN, SiO_2, Ta. SiN, SiO_2 and Ta, each 50 nm thick, have been deposited on top of stabilized FDLC films deposited on Si substrates. A scotch tape test showed that the as-deposited films had good adhesion to FDLC, but the adhesion failed after annealing at 400 ^oC. The delamination took place either between the top film and FDLC or between the FDLC layer and the substrate. XPS study of the delamination interface showed that the failure was caused by the formation of weak SiF_x bonds on the delaminated surface of the SiN and SiO_2 films and TaF_5 bonds on the surface of the Ta films [9]. Thus, in spite the fact that the FDLC films appeared to be thermally stable according to the stability evaluation based on mass loss and thickness changes, at 400 ^oC the FDLC interacted with the materials in contact with it and weakened the interface between the layers.

While most of the free or weakly attached fluorine is removed from the FDLC films during the initial stabilization anneal, residual fluorine is still released from FDLC in the Si/FDLC/X structures during the processing at the high temperature and accumulates at the FDLC/X and Si/FDLC interfaces until it reaches concentrations sufficiently high to weaken these interfaces. Thus, the “stabilized” FDLC is not really stable at further exposures to 400 ^oC. Work is still going on in different places on preparation and characterization of FDLC type low-k films [10], other authors claim to have fabricated FDLC films thermally stable at 400 ^oC [5,6], and some integration of FDLC with Al [11] and with Cu [12] has been demonstrated at temperatures below 350 ^oC. However FDLC films do not appear to have the potential to become the low-k BEOL dielectric for VLSI devices.

C.2. DLC

The amorphous tribological carbon materials with diamondlike properties are characterized by dielectric constants that are not lower than that of SiO_2 (k=4). Furthermore, the high intrinsic stresses of tribological DLC films can cause wafer bowing, thus interfering with the patterning process in the fabrication of VLSI circuits, and can cause adhesion failures.

Nevertheless, it is possible to reduce significantly the dielectric constants of PECVD deposited hydrogenated DLC (a-C:H) films by adjusting the deposition conditions [13]. As shown in Figure 1 (from [14]) the dielectric constants of the as-deposited low-k DLC films span the range of 3.8 to 2.7 and decrease with decreasing bias. The compressive stresses in the same films spanned the range of 800 MPa to 200 MPa, the latter being acceptable for a BEOL dielectric. The dependence of the dielectric constant on the deposition conditions is similar to that of the intrinsic stresses and, as shown elsewhere [15] and the thermal stability of these films follows the same trend. Films characterized by dielectric constants k >3.3 appeared to be stable at 400 ^oC while films characterized by k=2.7 showed a reduction in thickness of about to 50% after annealing at this temperature.

(Insert Figure 1)

The low-k DLC films contain from 40 % - 46 % hydrogen, the amount of hydrogen decreasing with increasing substrate bias and decreasing pressure, and is mainly controlled by the substrate bias [7,14]. The similar dependence of dielectric constant, stress and thermal stability of DLC films on the deposition condition may be explained by the effect of the latter on the film structure. DLC films are amorphous crosslinked structures, whose degree of crosslinking and carbon hybridization depends on the ion bombardment of the growing films. Higher substrate bias, higher powers, and lower pressures in the plasma result in stronger crosslinking in the films and produce films characterized by higher thermal stability, higher stresses, and higher dielectric constants.

While low-k DLC films of practical interest, with $k<3$, are not thermally stable in the as-deposited state, they can be stabilized by an annealing treatment at temperatures typical for the integration processing (400 ^oC) [16]. The hydrogen content of the films decreased to about 40% after the stabilization anneal, independent on the concentration in the as-deposited films [14]. The dielectric constant may increase slightly after the stabilization anneal but can be maintained below 3. The leakage current trough a stabilized film having a dielectric constant $k=2.7$ was 10^{-7} A/cm^2 at 0.5 MV/cm, sufficiently low to make the material usable as the interconnect dielectric. The stabilization anneal has an additional beneficial effect, causing a significant reduction of the intrinsic stresses in the films to values as low as 60 MPa [9].

The integration of low-k dielectrics in a damascene interconnect process involves the steps of metal removal from the top of the dielectric by chemomechanical polishing (CMP). DLC is generally known as a hard material with a high Young's modulus and high chemical inertness. [1]. While the stabilized low-k DLC films are significantly softer than the hard, wear resistant DLC coatings, they are still characterized by nanohardness values $H \sim 1.3\text{-}3$ GPa, and Young's modulus $E \sim 10\text{-}27$ GPa [16], as compared to $H < 0.5$ GPa and $E < 5$ GPa for most polymeric dielectrics. The mechanical and chemical properties of DLC enable efficient removal of the metallization and good planarization of the damascene structures by CMP.

The integration of DLC with copper metallization is illustrated in Figure 2 (from [14]), which shows a cross-section of two levels of Cu wires embedded in three levels of DLC dielectric. The M2 Cu wires have an imperfect shape because the etching process of the DLC was not yet optimized for the patterned structure on 200 mm wafers. Nevertheless, the micrograph illustrates the integrity of the structure up to the third DLC level. While significant efforts have still to be invested in optimizing the integration processes of DLC in the BEOL interconnect and characterizing its reliability, the obtained results indicate that DLC could be used as a low-k interconnect dielectric with Cu metallization in the BEOL of VLSI chips.

(Insert Figure 2)

D. CONCLUSIONS

Hydrogenated (DLC) and fluorinated (FDLC) amorphous carbon films with dielectric constants as low as 2.7 have been prepared by RF PACVD. The hydrogenated DLC films with $k > 3.3$ are stable at 400 ^oC and have high internal stresses. The as-deposited low-k films are unsatble at temperature above 400 ^oC. However, an anneal at this temperature seemed to stabilize both DLC

and FDLC films against further changes by subsequent exposures at this temperature. The dielectric constant of the stabilized FDLC films reached values < 2.5.
In spite the fact that mass loss and thickness change measurements seemed to indicate that the annealed FDLC films are stable at 400 ºC, it was found that these films react with silicon oxide, silicon nitride, and Ta when exposed again to this temperature forming SiF_x and TaF_x bonds. These bonds weakened the interface between FDLC and the other layers and resulted in delaminations of the structures.
In contrast to the fluorinated material, the stabilized DLC films with dielectric constants < 3.0 have shown good adhesion to the materials mentioned above and multilevel structures incorporating such films maintained their integrity at 400 ºC. Cu/DLC interconnect structures have been demonstrated up to two levels of metallization indicating that DLC is a potential candidate for the low-k interconnect dielectric.

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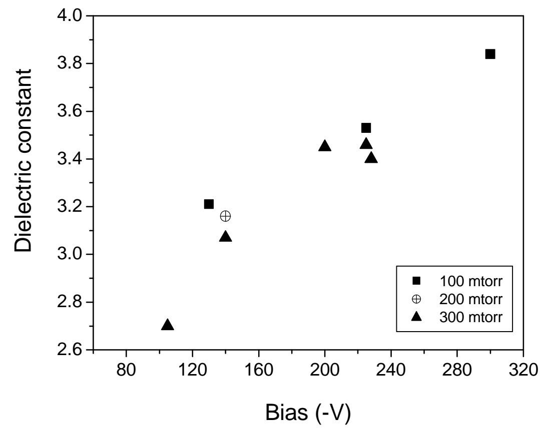

Figure 1 . Dielectric constants of as-deposited DLC films (from [14]).

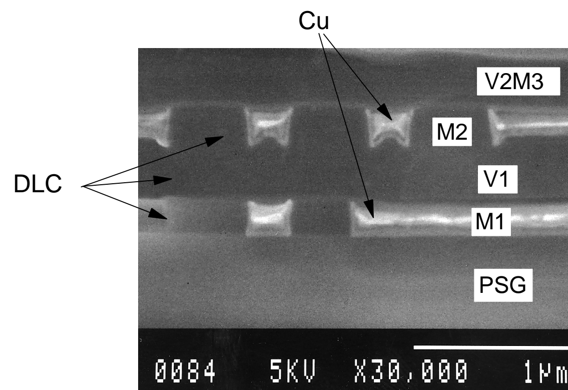

Figure 2. SEM micrograph of two level Cu wiring with DLC dielectric (from [14]).