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Technology and Design of an Active Matrix OLED on Crystalline Silicon Direct View Display for a Wrist Watch Computer

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Technology and design of an active matrix OLED on crystalline silicon direct view display for a wrist watch computer

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ABSTRACT

The IBM Research Division and eMagin Corporation jointly have developed a low-power VGA direct view active matrix OLED display, fabricated on a crystalline silicon CMOS chip. The display is incorporated in IBM prototype wristwatch computers running the Linux operating system. IBM designed the silicon chip and eMagin developed the organic stack and performed the back-end-of line processing and packaging. Each pixel is driven by a constant current source controlled by a CMOS RAM cell, and the display receives its data from the processor memory bus. This paper describes the OLED technology and packaging, and outlines the design of the pixel and display electronics and the processor interface. Experimental results are presented.

Keywords: Organic light emitting diode, OLED, display, emissive display, wearable computer, wristwatch computer.

1. INTRODUCTION

Computer components can, today, be found in many electronic devices, such as mobile phones, cameras or personal digital assistants. Over time, components have become more powerful, smaller in size and lower in cost. Technology improvements, also, continue to develop in short and long range wireless communications, enabling higher bandwidth connectivity and new applications. In order to better understand these technology requirements, a computer wristwatch research project was started. Various design challenges include power management, packaging, developing applications and improving the user interface [1].

The wristwatch display is the primary means in which the appliance outputs information to the user. Audio may also be used, but as a secondary means. As a key aspect of the user interface, the display needs to be easy to read and to show a useful amount of information. High contrast is needed for legibility, while higher resolution improves readability. Additionally, a wristwatch display should be viewable at night as well as in direct sunlight. For night viewing, an illuminator or emissive technology is required. A balance of the above attributes is needed with low power operation.

In general, liquid crystal (LC) displays do not satisfy the above objectives. Small direct view liquid crystal displays, as found in mobile telephones, are passively driven having small formats and low contrast. While suitably sized active matrix LC displays having larger formats and higher contrast are used in projection displays, the power for refreshing for either a passive matrix display or active matrix display is several milliwatts. To reduce power for mobile telephone displays, an active matrix with static memory LC display has been developed using low temperature polysilicon, but power levels exceed 1 milliwatt [2]. LC displays, also, require illumination for nighttime viewing. Either the illuminator is continuously on or a push button switch is used. The use of a switch is suitable for momentary viewing, but not for extensive use. An illuminator adds bulk and requires substantial power when used.

Power dissipation may be less with small sized organic light emitting diode (OLED) displays. OLED technology has high luminance and high contrast and is relatively efficient with low voltage operation. For LCDs, the backlight must illuminate all the pixels in the display whether or not the pixels are on. With an OLED display, power for illumination is dissipated in only the 'on' pixels. OLED display power can be very low if used with a black background. For showing time, which a wristwatch computer does 99% of the time, only 1% of the pixels would need to be on. In addition, the display brightness can be suitably adjusted depending upon lighting conditions for sufficient contrast. For conveying information to the user, a page of text may have 10-15% of the pixels on. The power to sustain the image can be lowered by using static memory to avoid display refreshing. The device leakage currents of crystalline silicon can be much lower than with a polysilicon back plane. Crystalline silicon also allows more function to be designed into the display.

The combination of OLED technology with crystalline silicon incorporating static memory would satisfy the display goals for the wristwatch computer. Using this approach, IBM Research and eMagin Corporation have jointly developed a VGA monochrome display. An IBM 0.35micron 3.6V CMOS process is used. The OLED is deposited on top of the silicon and is designed for top emission through a transparent cathode consisting of an electron injection material and indium tin oxide. The pixel pitch is 34.3 microns giving a 1.08 inch diagonal. Maximum luminance is 500 cd/m². While this is not the first OLED on crystalline silicon display to be reported, we believe that it is the first OLED on crystalline silicon display designed for direct view having this pixel density [3,4,5].

2. DESIGN

2.1 Physical

Previous experience that was obtained from designing and fabricating 1.3 inch diagonal LCOS, liquid crystal on silicon, displays, that incorporated mask stitching with a 0.8 micron CMOS process, lead to thinking that the OLED display could be similarly built using a newer 3.6V 0.35 micron CMOS process. Upon further study, the schedule and resource needed to develop mask stitching proved to be beyond the scope of this project. As a result, the chip size was limited to a single mask field size or 31.1 mm diagonal. With the mask field size constrained, sealing design optimization allowed an acceptable display size to be achieved [6]. Epoxy is used to attach the cover glass to the silicon chip. Figure 1 shows the resulting chip dimensions and top-level metal features. The chip size is ~23.4mm by ~19.8mm. This allows an array size of ~22mm by ~16.5mm having a 27.4mm diagonal. The pixel pitch is ~34.3 microns for a resolution of 741 dots/inch.

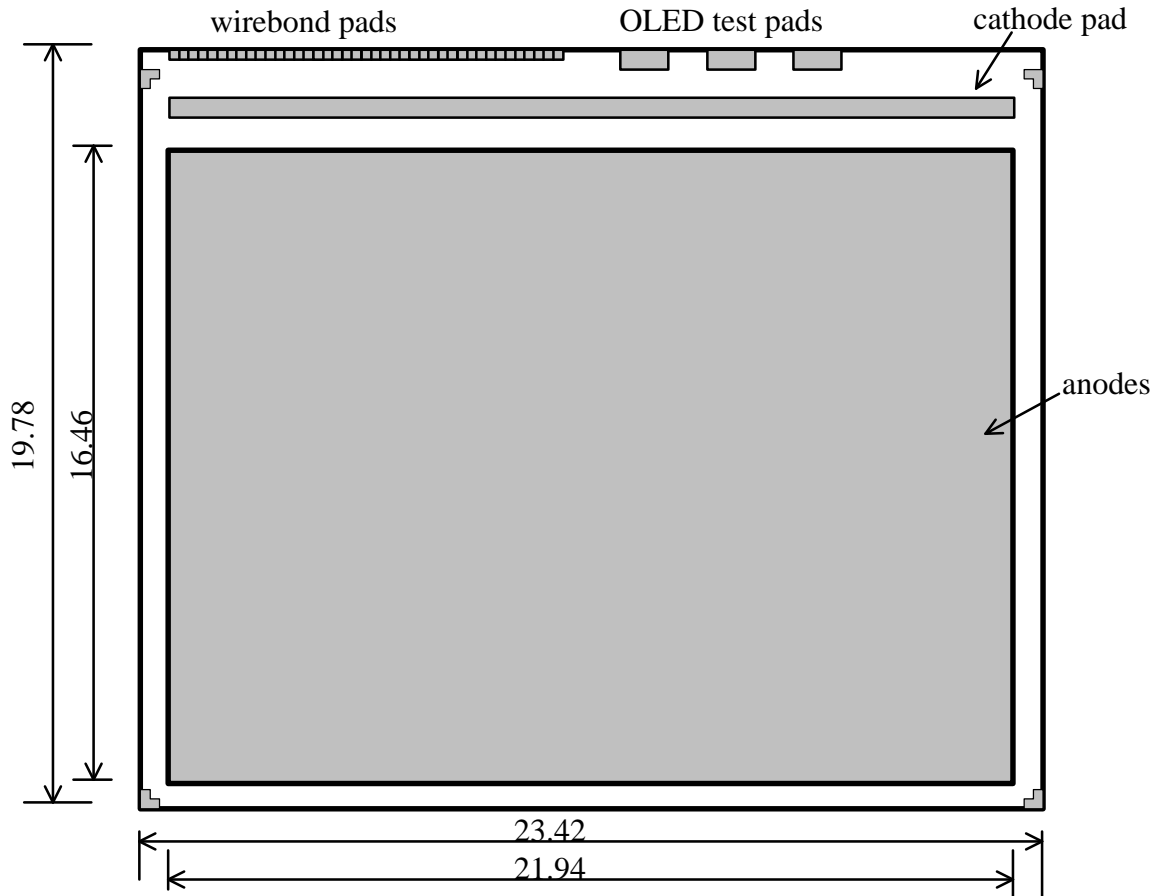


Figure 1: Wristwatch display chip showing main features and dimensions

Figure 2 shows the edge seal details. The OLED deposition overlaps the array by 0.5mm. The electron injector similarly overlaps the array. In order for the ITO to fully cover the reactive injecting material, the ITO overlaps the previous layers by

0.25 mm. The rigid seal is 0.25mm wide along 3 edges. The cover glass is 9mm thick. A groove in the cover glass is provided for a moisture absorbing getter.

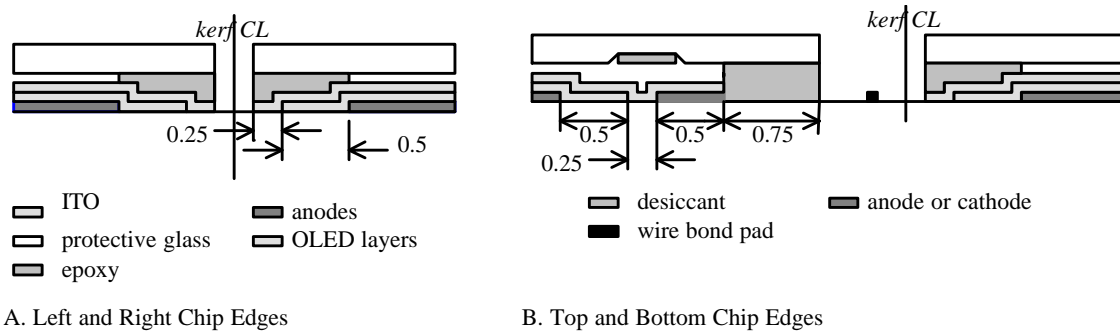


Figure 2: Details of cover glass sealing at the wafer level along A. left and right chip edges and along B. top and bottom edges.

The maximum design luminance was set at 500 cd/m^2 to minimize power dissipation and for other watch system design issues. The circular polarizer was initially specified to give good contrast in direct sunlight. However, the transmittance of a plastic film circular polarizer is only about 33% and would thus impact the power dissipation by 300%. Since OLED displays inherently have high contrast, the display contrast, if designed properly, should be sufficient for viewing in sunlight. Instead of using a circular polarizer, good optical design practices are used. The cover glass is anti-reflection coated on both sides. The thickness of each OLED layer is adjusted so that reflections from external illumination sources are minimized.

The pixel circuitry, discussed later, requires a -5V cathode power supply voltage. Due to the negative battery terminal being connected to ground in the watch, the cathode power supply circuitry utilizes -2x inverting charge pumps. Requiring 7 components, each charge pump is rated for 15mA. The high component count and low current capability limited the amount of allowable cathode current. Three charge pumps are used in parallel for a maximum current of 45 milliamps assuring 500 cd/m^2 of luminance.

Before starting the design, additional design details regarding the OLED characteristics, array/pixel structure and system interface were specified. In order to proceed, the OLED color, operating voltages and currents needed to be determined. Small molecule OLED devices are used due to their long lifetimes. To determine the color suitable for the display, an experiment was performed. Blue, green, and yellow/orange textual images with different fonts and font sizes on a black background were printed out on transparent foils using a 600dots/inch color printer. Using a fluorescent backlight to illuminate the foils, the luminance of each color using large area blocks was adjusted so that the brightness of colors was similar at $\sim 50 \text{ cd/m}^2$. It was readily apparent that the yellow/orange color was more readable than the green or blue.

Previous fabrication experience has shown that green OLED devices are the most efficient while blue and yellow OLED devices are somewhat less efficient, and the efficiency of orange or red OLED devices are not as good as blue or yellow. With its high visual contrast on a black background and its reasonable efficiency, a yellow-colored OLED was chosen.

The organic stack structure deposited directly on pixel circuitry consists of top emitting amber OLED comprises of a layer of copper phthalocyanine (CuPc) followed by a layer of naphthyl benzidine (NPB) for hole injection and transport. A doped emitter layer consisting of 8-hydroxyquinoline (Alq_3) host molecule is then co-deposited with dopant molecules. To complete the organic stack, a layer of Alq_3 is deposited for electron transport. The transparent cathode is finally deposited through the appropriate shadow masks in dedicated deposition chambers with in a robotic cluster system. Figure 3 shows the normalized spectral radiance distribution exemplifies a amber color with $\text{CIEx} = 0.48$ and $\text{CIEy} = 0.5$ and spectral peak near 570 nm. Typically these devices achieve current and luminous efficiencies of 5.7 cd/A and 3.5 lm/W at 2 mA/cm^2 . The operating lifetime – defined as the time required to reach 50% of the initial luminance at time zero when driven continuously at 20 mA/cm^2 exceeds 10,000 hrs. These lifetimes correspond to much longer expected typical product lifetimes for products run at predicted lower current densities and duty cycle as in wristwatch computer.

Figure 4 shows the current density and luminance as a function of voltage for the OLED devices used. For luminance of 500 cd/m^2 , the forward voltage is $\sim 6.7\text{V}$ and current density is 11 ma/cm^2 . The current per pixel is $\sim 130 \text{ nA}$.

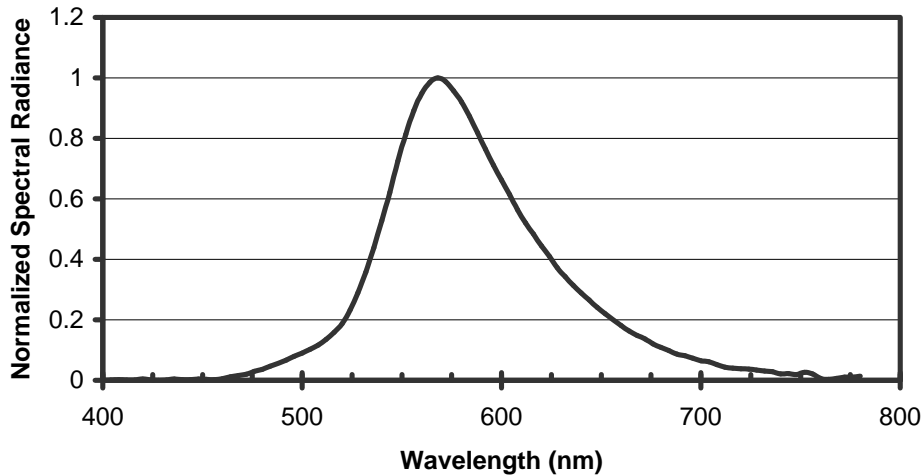


Figure 3. Normalized spectral radiance distribution of amber OLED.

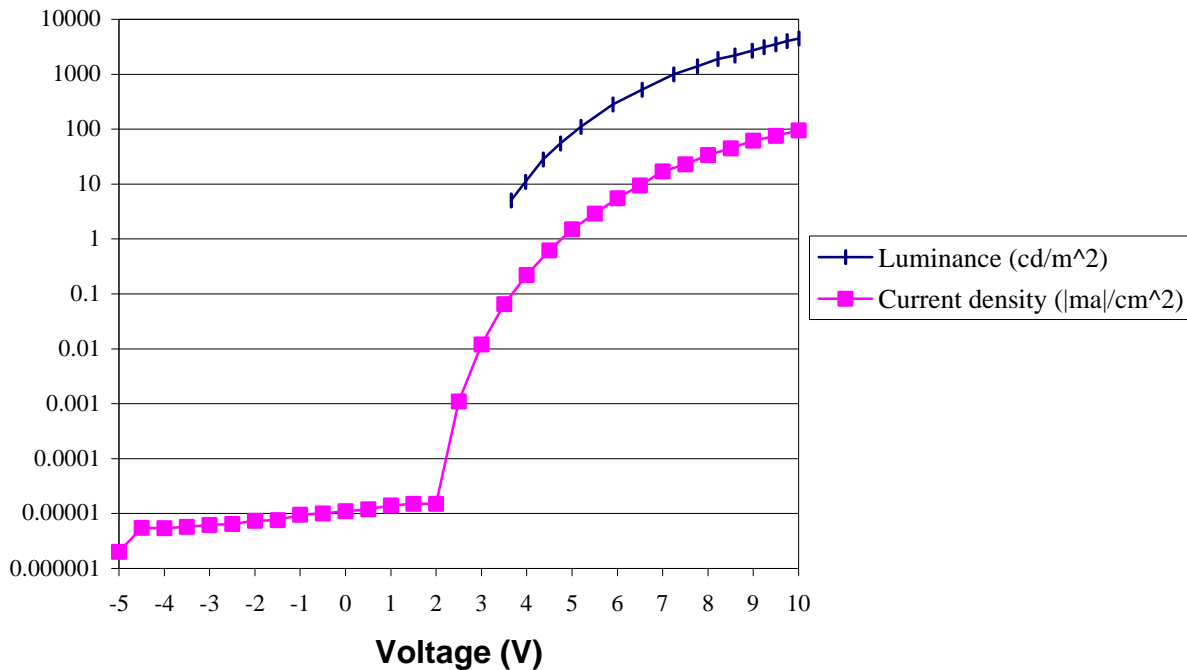


Figure 4: OLED absolute value current density and luminance as a function of OLED voltage.

2.2 Chip structure

Most displays use raster scan for addressing. Raster-scan drivers write data to every pixel in a row while sequencing the rows from top to bottom. A display controller, which generates the sequential data and proper timing signals, and additional inputs from the processor are needed. There are some definite advantages to using random access memory with an SRAM cell at each pixel. While it may require more inputs, random access memory has the ability to address any word in the array without sequencing. Since the number of pixels in a word is much less than a row, power is saved by writing only the words that need to be updated. The memory bus interface can also be used to send display control information that can further reduce power dissipation.

A logic block diagram shown in Figure 5 depicts the electrical functions of the display chip. There are 16 data input or output lines. The 16 bits of data form a word. Nine address lines are used to decode each of the 480 word rows of the array. Each

word row decoder has separate word row read and word row write outputs that allow use of a single bit line SRAM cell that is discussed later. An additional six address lines are needed to select the forty word columns in the array. Embedded in each word in the array are word select circuits. The memory control inputs include an active low chip enable, `_CE`, an active low write enable, `_WE`, and an active low output enable, `_OE`.

A single 16 bit addressable control register is used for controlling the display attributes. Eight bits are used to define the luminance. The luminance is controlled by pulse width modulation at a frequency of 60Hz using an external clock or an internally generated clock. With the maximum luminance set at 500cd/m², the luminance can be adjusted from 0 to maximum in 4cd/m² increments. Each of another 4 bits selects an external clock, clears the display, puts the display into a standby mode and reverse biases the OLED pixels. The `CLEAR*` or `_POR` signals set all the word row write lines and all word column lines high while resetting all data write driver outputs low. This forces the entire array data to be low. The `CLEAR*` bit can be used to reduce the energy when writing new images. The old image is erased by setting the `CLEAR*` bit high. After resetting the `CLEAR*` bit low, a new image can be written using only the words having 'on' pixels. Since the `WORD` locations having all bits off do not have to be written, the energy to write new images can be significantly reduced.

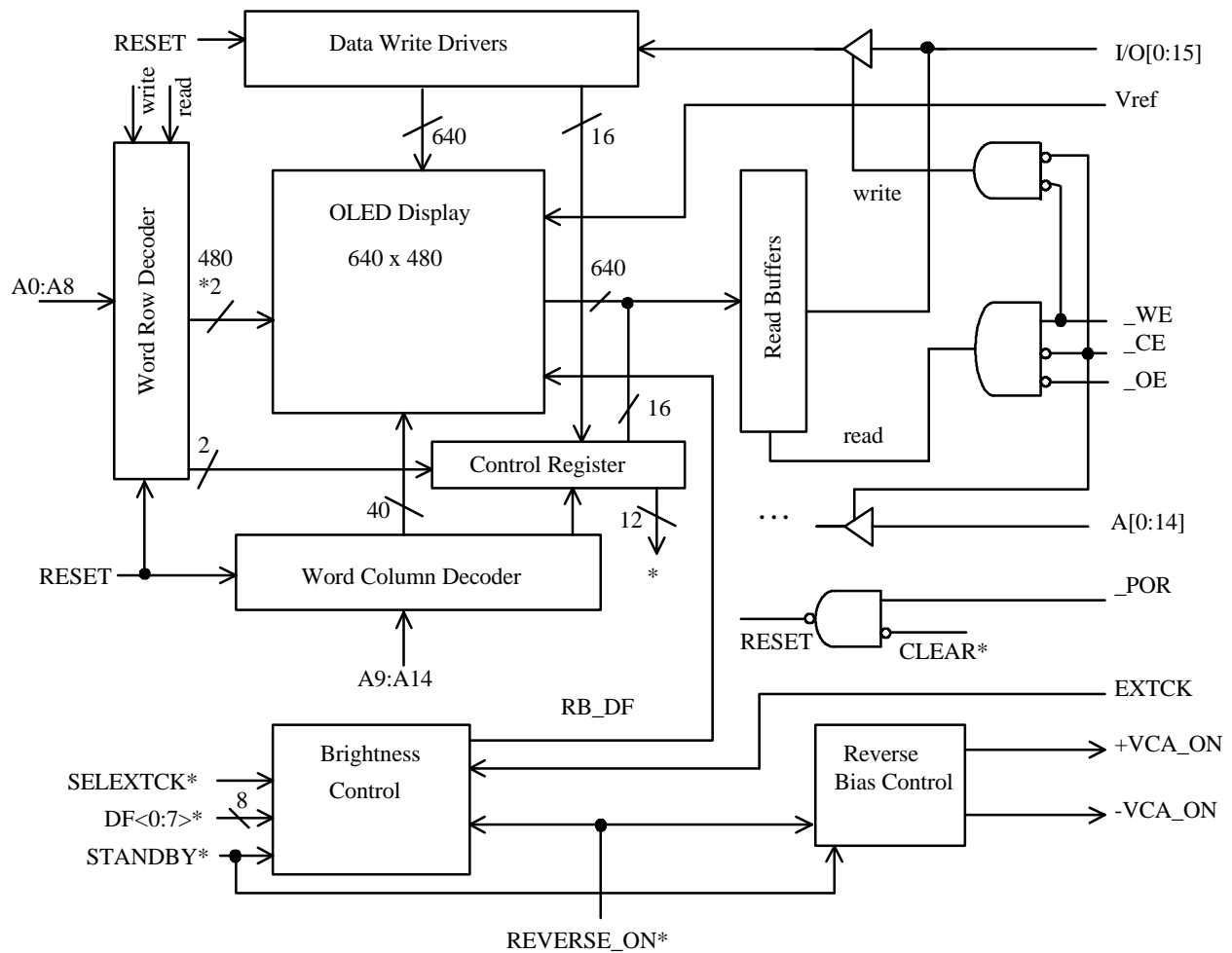


Figure 5: Block diagram of the display chip electrical structure

The read buffer circuit consists of a half latch, an inverter and a PMOS transistor, driving a second inverter. The PMOS is used to pull the bit line voltage up to +3V when high state data is being read out. The display has much longer data, control and address lines requiring more power to read and write than regular memory. As a result, reading is used for testing purposes and not used by the processor as an image buffer. Design emphasis is put on low power writing.

The brightness control block includes an eleven-stage ring counter, 21-stage counter, a 7-bit pulse width signal generator and a pair of switches to select an external clock input while switching off the ring oscillator. A high SELEXTCK* or STANDBY* signals switches the ring oscillator off. A high state on signals STANDBY* and REVERSE_ON* switches all the pixel current sources in the array off.

The reverse bias control block provides delays in the edges of +VCA_ON and -VCA_ON signals to the system board so that the positive cathode voltage is not shorted momentarily to the negative cathode voltage. A high +VCA_ON signal connects the cathode to +6V power. A high -VCA_ON signal connects the cathode to -5V power.

The VREF input, which is adjustable, is used to set the maximum brightness to 500 cd/m². VREF directly controls the OLED current in each pixel in the array. In this manner, the initial OLED brightness and initial circuit tolerances are adjusted out.

The word structure in array is shown in Figure 6. The row decoder outputs, world row write, WRW, and word row read, WRR, are connected to each of the 40 word decoder circuits in the row. The word column signal, WC, is connected to all the 480 words in the word column. The word decoder simply consists of two AND gates which drive the local pixel capacitance for a divided word line structure [7]. The WRW and the WC signals are inputs to one AND gate with the output connected to the local word write line, WW. The WRR and WC are inputs to the other AND gate whose output is connected to WR line, the local word read signal. The width of each pixel circuit is reduced to make room for the word decoder. Since the anode-to-anode pitch in x and y is constant, the wiring connection from each pixel circuit to its anode is adjusted for the pixel circuit displacement.

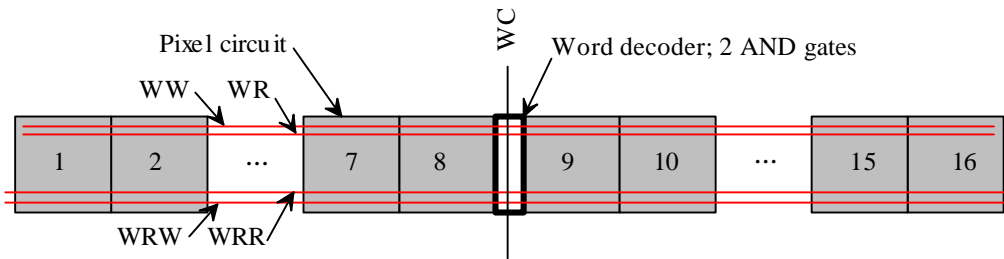


Figure 6: Physical layout of the word structure in the array.

2.3 Pixel Circuit

The pixel circuit has an SRAM and a switching current source to drive the OLED. Since the area available for the pixel is quite large, 1,157 square microns, the function can be designed in a manner that is best suited for the application.

A single bit line SRAM is used with a savings in power since only one bit line is driven as compared to driving the more typical complimentary bit lines. The pixel circuitry is shown in Figure 7. The single bit line SRAM circuit consists of NMOS Q1 and NMOS Q2 and inverters I1, I2 and I3. To write data into the SRAM cell, the word write input is brought high while word read input is low. The data on the bit line is connected to the input of inverter I1 and output of I2 by Q1. The strength of the inverter I1 is normally sized while strength of inverter I2 is twelve times less. The weak strength of I2 allows easy writing of data into the I1-I2 latch. In order to read the data stored in the SRAM, the word write input is low and the word read input is brought high. The output state of inverter I3 is passed onto the bit line by Q2. Inverter I3 isolates the capacitive loading of the bit line from the output of inverter I1.

Inverter I3 may not be necessary if inverter I1 is strong enough or Q2's W/L is reduced to avoid changing the latch data. Reducing Q2's W/L would increase the read times. A similar circuit arrangement using a sequence of pulses on the gates of Q1 and Q2 for reading and writing has previously been published [8]. The weak latch used in the pixel SRAM eliminates the need for reading and writing pulse sequencing.

The current generating device in the current source circuitry is PMOS Q3. Most pixel current source circuits, that are fabricated using crystalline silicon, are required to operate in the sub-threshold regime. Since the pixel current is very small and CMOS transistor transconductance is very high, operation in the saturation regime is not usually possible. However, due to Q3's very small W/L ratio, Q3 operates in the saturation regime. In saturation where $|V_{ds}| > |V_{gs} - V_t|$, threshold voltage variations have less effect on the drain to source current variations. For the available area in the pixel, Q3's width and gate to source voltage is optimized with regard to the impact of channel width and threshold variations on the drain current variation.

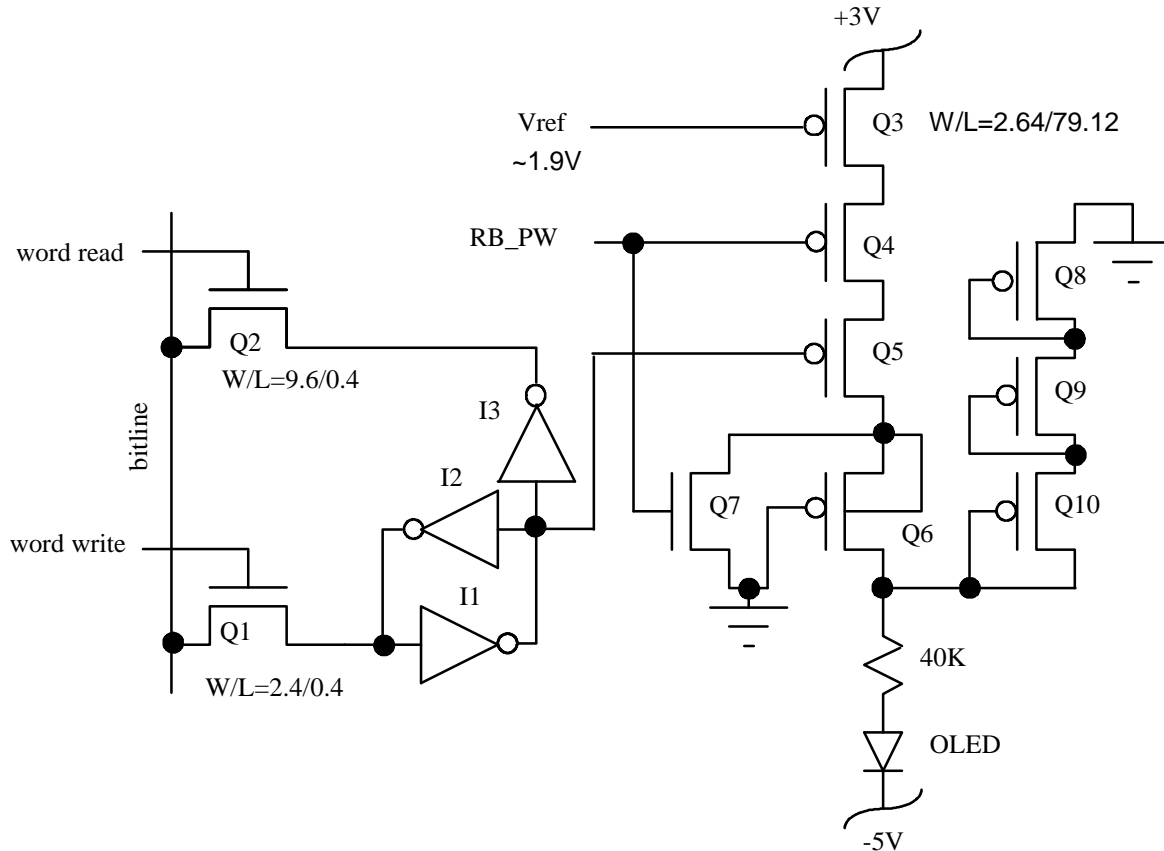


Figure 7: Circuit diagram showing the pixel circuitry.

PMOS transistor Q5 is the pixel on and off switching transistor. A low state on the output of inverter I1 turns Q5 on. The input signal RB_PW drives the gates of PMOS Q4 and NMOS Q7. A low state on the gate of Q4 allows current to flow into Q5. If Q4 and Q5 are both on, then the current will flow into Q6. An active low pulse on the RB_PW input provides width modulation of OLED luminance. Initially as current flows into PMOS Q6, Q6 operates as a cascode transistor extending the current source compliance 3V below ground. As the OLED capacitance charges and the anode voltage rises above ground, Q6 changes over to a switch. When the RB_DF is switched high, NMOS Q7 turns on, grounding the source of Q6, turning Q6 off and quickly discharging any stray capacitance. During reverse biasing of the OLED to remove forward bias trapped charge, Q7 is turned on and the cathode voltage is switched to +6V. The OLED anode is connected by Q7 via Q6's drain or p diffusion to n-well, which is a forward biased diode, to ground.

PMOS Q8, Q9 and Q10 form a -3V clamp to assure that the Q6 terminal voltages do not exceed 3.6V when the OLED is off. An un-doped poly-silicon resistor is used to limit current and resulting thermal energy from shorts.

Circuit simulations using BSIM3 version 3 transistor models provided performance estimates. Transient analysis showed the maximum time needed to write is 15 nanoseconds while the maximum time for reading is 30 nanoseconds. The current source circuit simulations show that the 3 sigma current variation is +/- 2.5% across the chip. An OLED circuit model for an individual pixel is derived from the OLED technology current versus voltage data shown in figure 4. The circuit simulations for the pixel cathode current as a function of cathode voltage are shown in Figure 8 for the current-source-on, for the current-source-off and for a shorted OLED with the current-source-off conditions. The cathode current for the current-source-on condition is 137nA and constant within 0.1% for cathode voltages between -4.5V and -7V. Q3's long channel length reduces the channel length modulation with drain to source voltage, providing excellent current source compliance.

The current-source-off cathode current increases sharply with cathode voltage more negative than -5V and is <1pA for cathode voltages more positive than -5V. The ratio of the 'on' to 'off' current is >100,000 with a -5V cathode voltage. If the

OLED is shorted, the cathode current increases sharply with cathode voltages more negative than $-3V$ and is approximately $1\mu A$ at $-5V$.

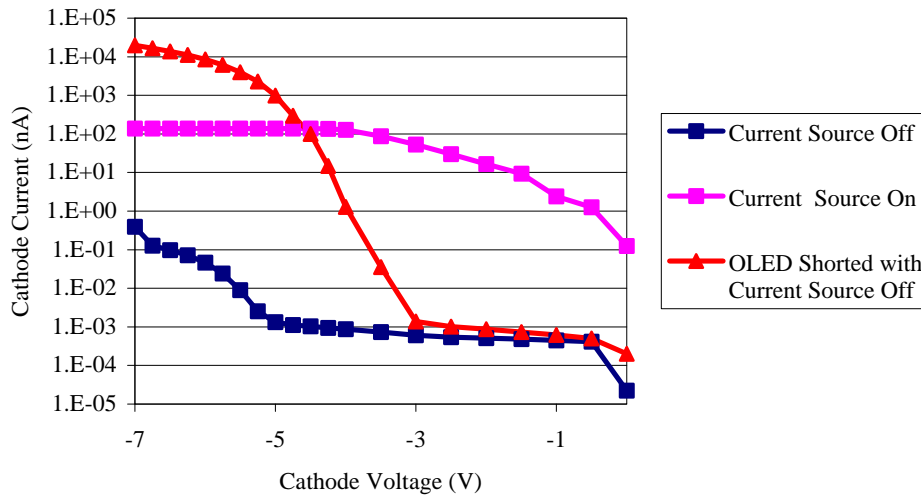


Figure 8: Circuit simulation results showing OLED current with cathode voltage.

These simulations show that good operation is obtained with a $-5V$ cathode voltage. For $-5V$ cathode voltage, there is $0.5V$ of excess current source compliance to allow for voltage variations within the display. Such variations would include the distribution for $+3V$ power, the cathode voltage distribution and OLED voltage variations across the chip due to initial tolerances and forward bias charge build up.

3. RESULTS

The performance of the display is characterized by power supply current measurements, by optical measurements and display images. During electrical wafer testing prior to OLED deposition, the read and write functions were verified statically and dynamically using a memory tester. After all 0's or all 1's are written, the $+3V$ current in steady state is $\sim 5\mu A$. With the internal clock on, the $+3V$ current is $0.95mA$. The $+3V$ current is $3mA$ when writing all 0's or 1's at $20MHz$. Writing a worse case single pixel checkerboard pattern, the $+3V$ current is $10.08mA$. The static power consumed by the display is $\sim 15\mu W$. The power consumed by the internal clock is higher than expected at $\sim 3mW$. To avoid this power dissipation, an external $32.768KHz$ clock would be preferred. The external clock frequency is low enough that $<1\mu W$ would be dissipated. Although high currents were measured for writing, the typical and maximum power for writing a new image every second is $\sim 10\mu W$ and $\sim 29\mu W$, respectively. Using the CLEAR function, $<1\mu W$ image writing power is expected.

A number of displays were packaged onto printed circuit boards. A large area photodiode was used to monitor the relative OLED light output. The cathode current and photodiode current with luminance set at $250cd/m^2$ was measured with all pixels set off. The display measured had about 300 dark pixels indicating shorted OLED pixels. The all off photodiode and cathode voltage current measurements are shown in figure 9. At $-5V$, the cathode current is quite high at $200\mu A$. From the simulations, the expected cathode current would be about $0.5\mu A$ if there were no shorts. The cathode current would be about $300\mu A$ for 300 OLED pixels having shorts. For low power operation, the display would have to be fabricated without shorts or the $-3V$ clamps would have to be removed. For off pixels, the photodiode current became significant for cathode voltages below $-5V$.

In another measurement with the cathode voltage at $-5V$, the cathode current was measured with 1% of the pixels turned on and with the luminance reduced to $30cd/m^2$; a condition suitable for showing time. The OLED pixels that were on had sufficient contrast to be viewed in normal room light conditions. The incremental current above the all off condition cathode current was $27\mu A$. With $8V$ across the chip, the incremental power is $216\mu W$. Including the static memory power and power for writing new images, the power dissipation for showing time would be $<250\mu W$ if the display were free of shorts.

The cathode current was measured for different cathode voltages using 1 in 16 pixels on, using a checkerboard pattern having half the pixels on and for all pixels on. The current measurements were corrected for the appropriate percentage of off pixel current, obtained from figure 9, and are shown in figure 10. The current is within 1% for cathode voltage between -4.5V and -6V for the 1 in 16 on case. The current is within 1% for cathode voltages between -5V and -6.5V for the checkerboard and all on conditions.

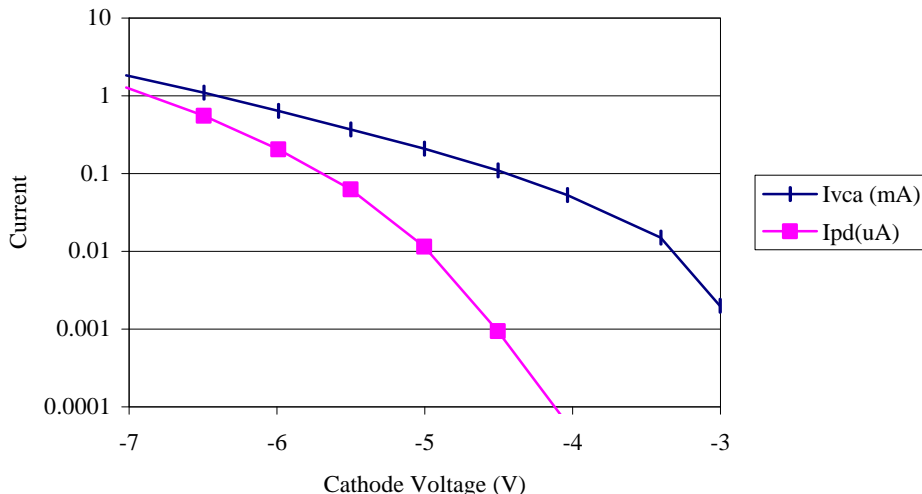


Figure 9: All OLED off photodiode current and cathode current with cathode voltage.

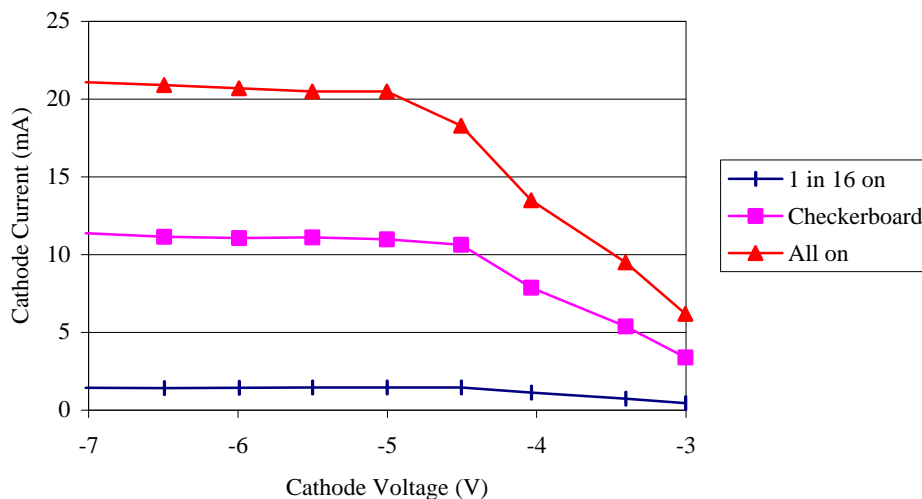


Figure 10: Corrected cathode current measurements with cathode voltage for all on, checkerboard, 1 out of 16 on and all off conditions.

In a similar manner, the photocurrent measurements were corrected for appropriate percentage of off pixel photocurrent for the same three ‘on’ pixel conditions and are shown in figure 11. The photocurrent is within 1% for cathode voltage between -4.5V and -6V for the 1 in 16 on case. The photocurrent is within 0.3% for cathode voltages between -5V and -7V for the checkerboard and all on conditions. As expected, the photocurrent measurements and cathode current measurement results are very similar. These measurements show that the compliance of the pixel current source is within 1% for all conditions for cathode voltages between -5V and -6.5V . The on to off contrast is ~ 4200 . While these results are not nearly as good as the circuit simulations, the measurements do show very good contrast and luminance control with variation in cathode voltage.

The luminance of 112 adjacent pixels was measured using a large area photodiode. A histogram showing the normalized luminance is shown in figure 12. The luminance is within 1.5% of the mean. The standard deviation is 0.62% of the mean.

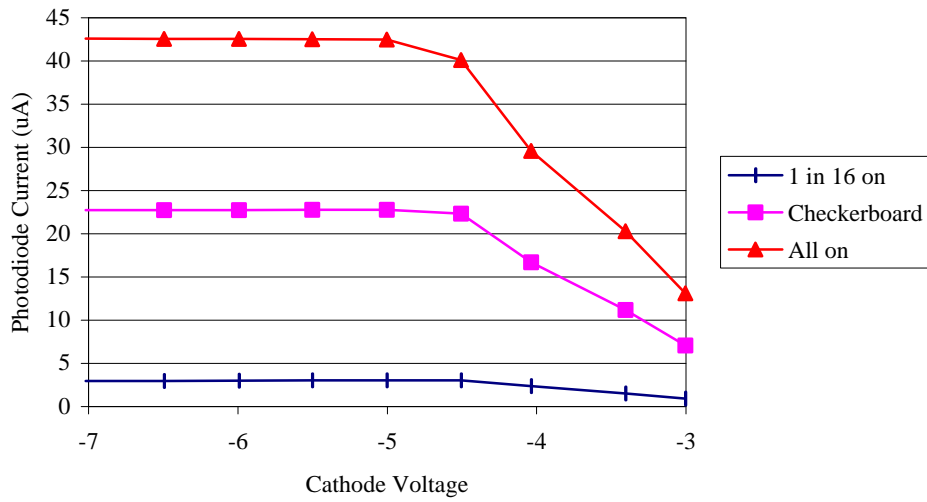


Figure 11: Corrected photodiode current as with cathode voltage for 1 pixel in 16 on, checkerboard and all on conditions.

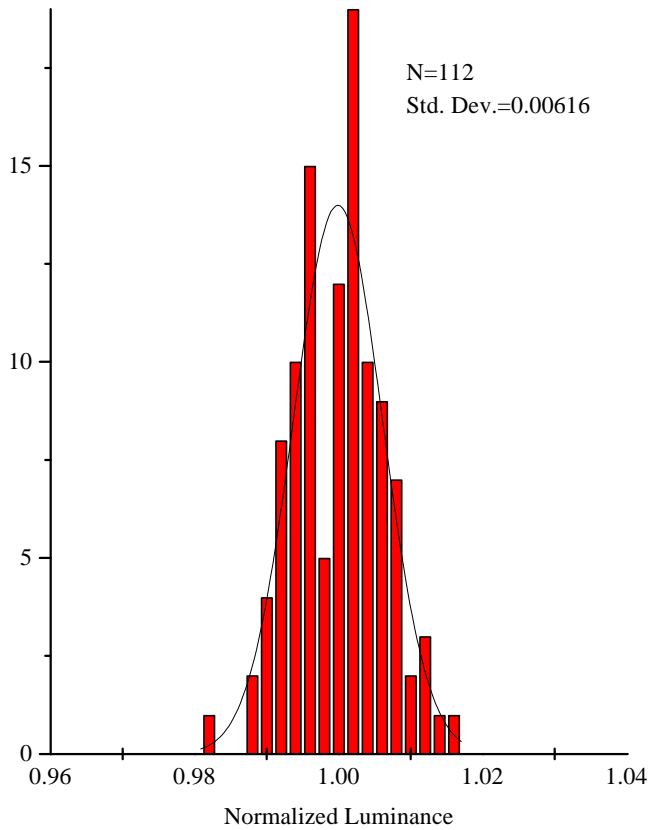


Figure 12: Histogram for normalized luminance of 112 adjacent OLED pixels.

In order to determine the across chip uniformity, a Minolta CS-100 spot meter was used to measure the luminance uniformity in 9 different positions over the viewing area. The uniformity was within 2.9%. The combination of measurements implies

that the pixel uniformity over the entire display is uniform within 3% of the mean. This shows that the combination of current source uniformity and OLED uniformity is very good.

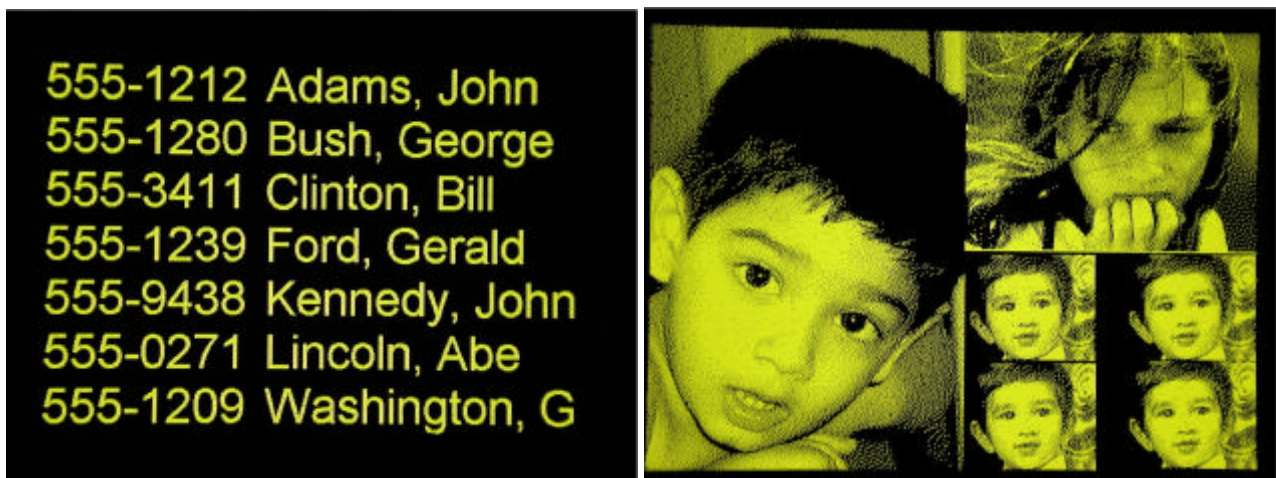
The displays are viewable, and the contrast was measured, in direct sunlight. The display 'off' pixel luminance is 93 cd/m². Sufficient sunlight viewing contrast, greater than 4:1, is obtained when the 'on' pixel luminance is above 375cd/m².

The displays have been assembled into computer wristwatch prototypes as is shown in photograph 1. The computer has an ARM 7 processor, 8 Megabytes of DRAM and 8 Megabytes of flash memory. The Linux operating system with the X11 graphics package is running on the computer. The watch uses a touch screen and a scroll wheel for interaction. An infrared data port and a serial port can be used to upload data into the watch. A simple organizer function is running on the watch demonstrating various applications.

Photographs 2 and 3 are enlarged digital camera images showing high quality text and a collage of photograph images. The gray levels in the images are obtained by using spatial dithering. Both the text and photo images are quite striking.



Photograph 1: The OLED VGA on crystalline silicon display is shown in a Linux computer wristwatch prototype.



Photographs 2 and 3: Display images enlarged showing text and collage of photographs which use spatial dithering for gray levels.

4. SUMMARY

A direct view OLED on crystalline silicon high resolution has been developed as part of a Linux wristwatch computer project. The silicon design uses a single bit line SRAM at each pixel to store data. Instead of addressing by raster scan, a memory bus interface incorporating random access is used. The leakage current of crystalline silicon and the system design resulted in low power data storage and writing operations. A summary of the display characteristics is shown in table 1.

Viewing area diagonal	0.864" x 0.648" (21.94mm x 16.46mm); 1.08 inch (27.4mm)
Format	VGA (640 x 480)
Pixel pitch	34.3 microns
Resolution	741 dots per inch
Structure	1 SRAM cell per pixel with a memory bus interface
OLED forward voltage	~6.7 V
OLED color	Yellow; CIE(x=0.473, y=0.508)
OLED efficiency	~2 lumens/watt
Emitting area to pixel area ratio	89%
Luminance range	0 to 500 cd/m ² in 4 cd/m ² increments

Table 1: Summary of the OLED on crystalline silicon display characteristics.

Measurements taken show that the luminance uniformity and contrast are very good. This is apparently due to the combination of pixel current source design and OLED design and processing. While attempting to protect the current source circuitry from excessive voltage, the clamp circuits dissipate significant power with shorted OLED pixels. While shorted OLED pixels should not be a manufacturing issue, the combination of shorts and clamp circuits did not allow low power OLED operation. However, it was shown that without shorts that display power for displaying time with 1% on pixels at 30cd/m² could be <250uW. This is significant since low power with an emissive display is possible for this application. The power levels can be lower than LCDs having a similar size and format.

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