

# IBM Research Report

## Superconducting Bandpass Delta-Sigma Modulator with 2.23GHz Center Frequency and 42.6GHz Sampling Rate

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# Superconducting Bandpass $\Delta\Sigma$ Modulator with 2.23GHz Center Frequency and 42.6GHz Sampling Rate

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Digitization of RF signals in the GHz range remains a challenge for any technology. Flash ADCs can digitize signals above 1GHz, but their dynamic range is inadequate for most radio systems. Semiconductor bandpass  $\Delta\Sigma$  modulators digitize IF signals with high resolution, but their performance at GHz frequencies is limited by comparator delays and the low Q of integrated inductors. Superconducting technology based on Josephson junctions features valuable components for implementing bandpass  $\Delta\Sigma$  modulators: high-Q resonators, multi-GHz comparators, and DACs with naturally quantized output pulses. The superconducting bandpass  $\Delta\Sigma$  modulator presented here achieves the highest center frequency (2.23GHz) and sampling rate ( $f_s=42.6\text{GHz}$ ) reported to date. The SNR (49dB over a 20.8MHz bandwidth) is limited by the frequency resolution of the measurement but still exceeds the SNRs of semiconductor modulators with comparable center frequencies.

Figure 1 presents the schematic of the bandpass  $\Delta\Sigma$  modulator[1]. The input is capacitively coupled to a superconducting microstrip resonator; for  $C_c = 0.11\text{pF}$ , loaded Q is greater than 5000. The current through  $L_r$  is quantized by a single flux quantum (SFQ) comparator comprising Josephson junctions  $J_1$  and  $J_2$ . If the current is above threshold, the sampling pulse switches  $J_2$ , generating a quantized voltage pulse on the modulator output; this quantized pulse is known as an SFQ pulse since its area equals the magnetic flux quantum ( $h/2e$ ). If the current is below threshold, the sampling pulse switches  $J_1$  instead of  $J_2$ , and no output pulse is generated. Each SFQ out-

put pulse represents a binary 1, and its absence represents a binary 0. The SFQ pulses generated across  $J_2$  also inject current back into the resonator, thereby realizing the “feedback” DAC. At quarter-wave resonance, the microstrip line shunts  $J_2$  with a low impedance, and quantization noise is suppressed. Source  $V_b$  biases the circuit to produce roughly equal numbers of 1s and 0s.

Since the modulator output data rate exceeds the capacity of the interface to room-temperature test equipment, the test chip includes an integrated acquisition memory. Only 256 bits can be captured due to integration limits of Josephson technology. A 256-point FFT lacks the frequency resolution needed for accurate measurement of ADC performance. Higher resolution measurements are made by “segmented correlation”, illustrated in Figure 2. Two 128b segments of the modulator output are captured with a pair of shift register banks.  $N$  is set by a programmable counter (from 0 to over 8000). Cross-correlation of the two segments generates an estimate of the autocorrelation function  $R[n]$ , for  $N+1 < n < N+255$ . By reprogramming  $N$ ,  $R[n]$  can be estimated for all  $n$  up to 8255. Fourier transformation of  $R[n]$  yields a spectrum with frequency resolution of an 8K-point FFT.

The block diagram of the test chip is shown in Figure 3. While the analog input is delivered to the chip over coaxial cable, external clocking at 20-45GHz cannot be done electrically due to sample holder limitations. External clocking is accomplished with an optical technique [2], in which 20.6GHz optical pulses are delivered via fiber to an on-chip photodiode, the current pulses from which drive a Josephson clock amplifier. Alternatively, the modulator can be triggered by an on-chip clock source. An increase in bias current turns the clock amplifier into an oscillator tunable between 20 and 45GHz. A 1:4 demux converts the output data to 4b words at  $f_s/4$ , allowing most of the chip to run at a reduced clock rate. The programmable counter controls loading of shift register banks A and B. After loading is done, a readout controller transfers the data to output drivers, which generate 2mV logic levels.

Figure 4 is a logic diagram of the programmable counter. The LOADA and LOADB outputs initiate loading of shift register banks A and B. The T and D flip-flops form a low-skew frequency divider described in [3], but a programmable relative delay between the LOADA and LOADB pulses is added with little extra circuitry by switching the clocking of flip-flops  $D_{0B}$ - $D_{10B}$ . In general, switching  $S_k$  from 0 to 1 increases the pipelining latency by  $2^k$  CLK cycles, so the relative delay (in CLK periods) equals the 11b code given by  $S_0$ - $S_{10}$  (from 0 to 2047). Maximum operating frequency (21GHz in simulation) is independent of counter length. Since the counter is clocked at  $f_s/4$ , N can be varied for segmented correlation from 0 to 8060, in increments of 4.

The test chip is fabricated in Nb/AlOx/Nb technology with  $1\text{kA}/\text{cm}^2$  critical current density for the Josephson junctions. While the chip has been used with the 20.6GHz optical clock, higher oversampling ratios and SNR are attained with the on-chip clock source operating near 40GHz. Output spectra at a 42.6GHz clock rate are shown in Figure 5. The width of the tone at 1.7GHz reflects the low frequency resolution of the 256-point FFTs averaged to make the plot. FS input sensitivity is -17.4dBm. Quantization noise is minimized at 2.23GHz and at higher frequencies corresponding to higher-order microstrip modes; noise suppression near dc is due to inductor  $L_b$ . Figure 6 plots SNR versus input level; peak SNR over a 20.8MHz bandwidth is 49dB. Lower in-band noise levels are attained by reducing the clock rate to 40.2GHz (where the on-chip oscillator has better stability) and by increasing the frequency resolution with segmented correlation. Idle channel spectra obtained by estimating  $R[n]$  up to various values of n are compared with (averaged) 256-point FFTs in Figure 7a); resolution enhancement by segmented correlation reduces the measured noise over a 19.6MHz bandwidth by over 3dB, to -57dBFS. Frequency variations of the on-chip oscillator (about  $\pm 0.05\%$ ) hinder longer correlation estimates. The experimental spectrum obtained by estimating  $R[n]$  up to  $n=511$  is compared with averaging 512-point FFTs of

circuit simulation data in Figure 7b); measured in-band noise is 1dB lower than in simulation. Since the limited resolution of the 512-point FFTs degrades the simulated in-band noise by 2.5dB, dynamic range of the experimental modulator over a 19.6MHz bandwidth is likely 59-60dB. The  $6.3 \times 6.3 \text{mm}^2$  test chip in Figure 8 contains 4065 Josephson junctions and dissipates 1.9mW at  $T=4.2\text{K}$ .

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*References:*

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- [2] Bulzacchelli, J.F. et al., "Optoelectronic Clocking System for Testing RSFQ Circuits up to 20GHz," IEEE Trans. Appl. Supercond., vol. 7, pp. 3301-3306, June 1997.
- [3] Lin, J.-C. and V.K. Semenov, "Timing Circuits for RSFQ Digital Systems," IEEE Trans. Appl. Supercond., vol. 5, pp. 3472-3477, Sept. 1995.

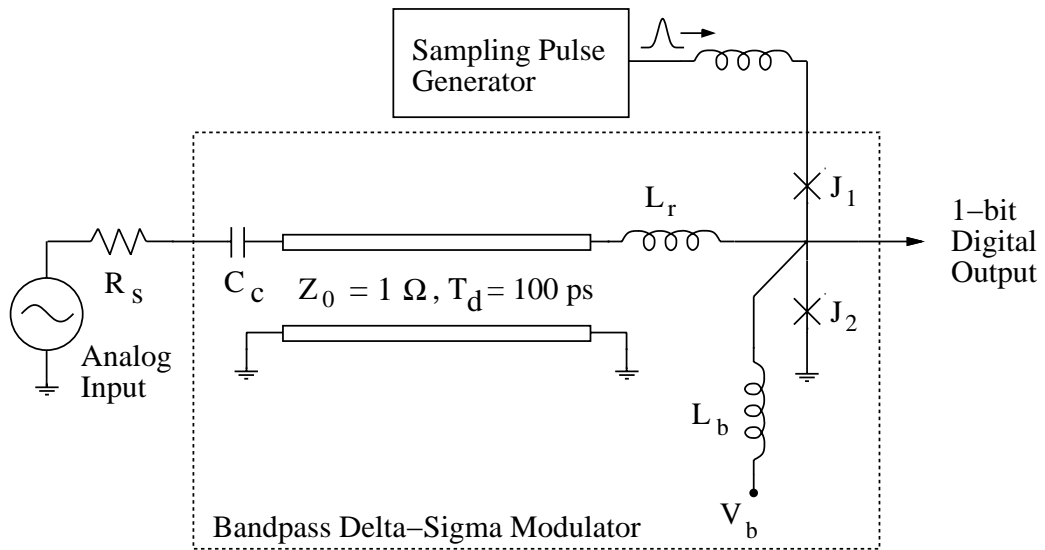


Figure 1: Superconducting bandpass  $\Delta\Sigma$  modulator.

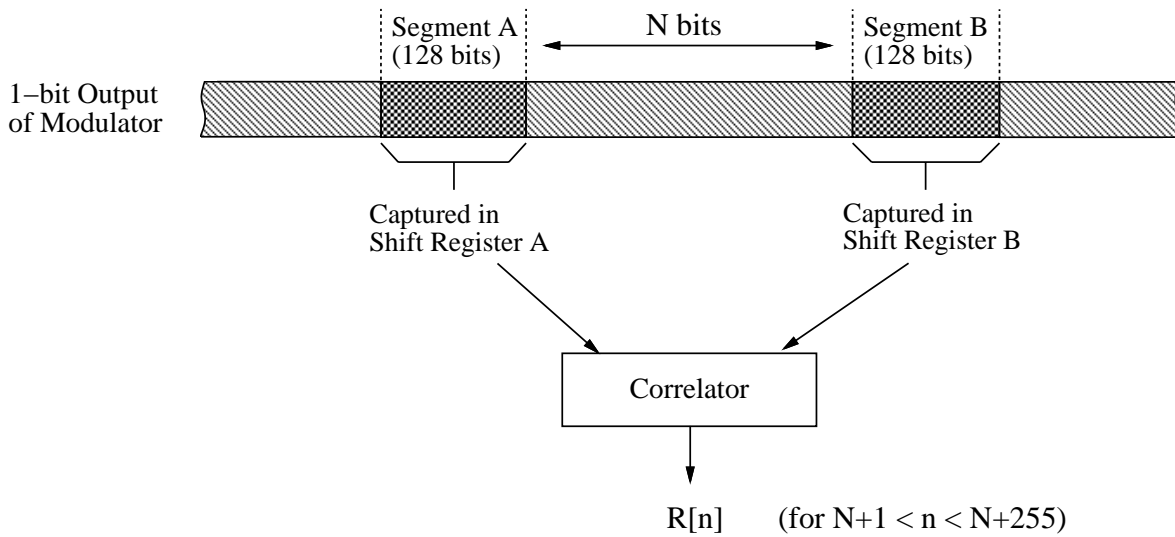


Figure 2: Segmented correlation technique.

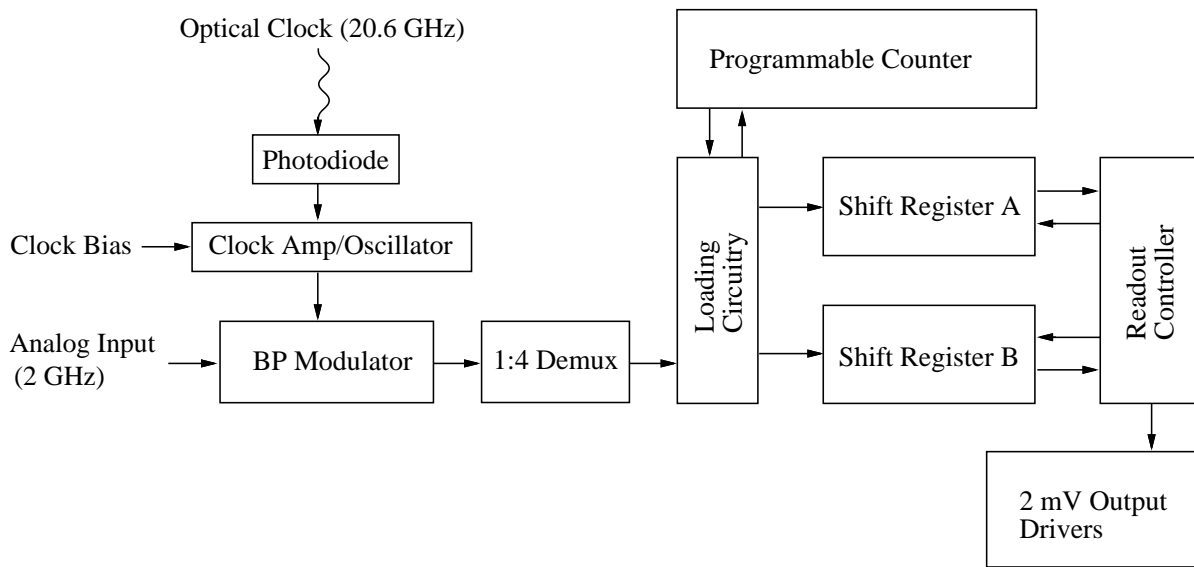


Figure 3: Test chip block diagram.

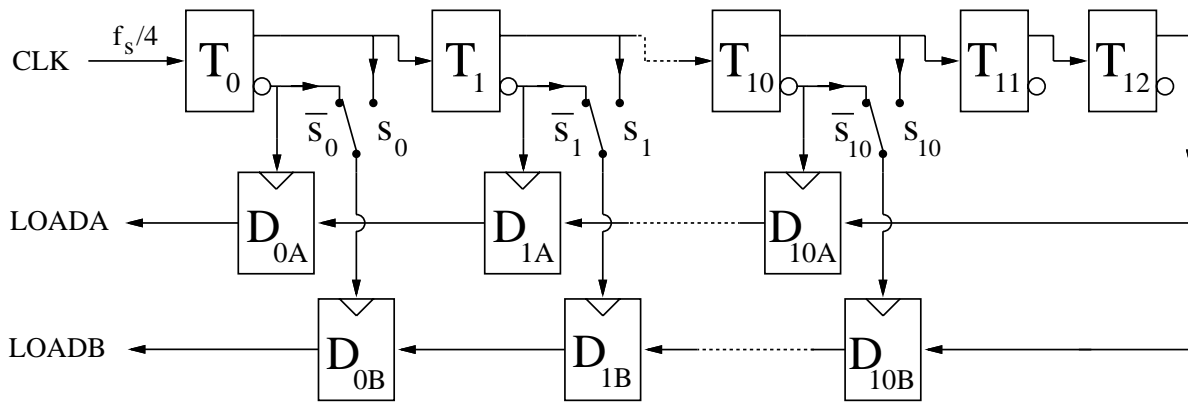


Figure 4: Counter with programmable relative delay.

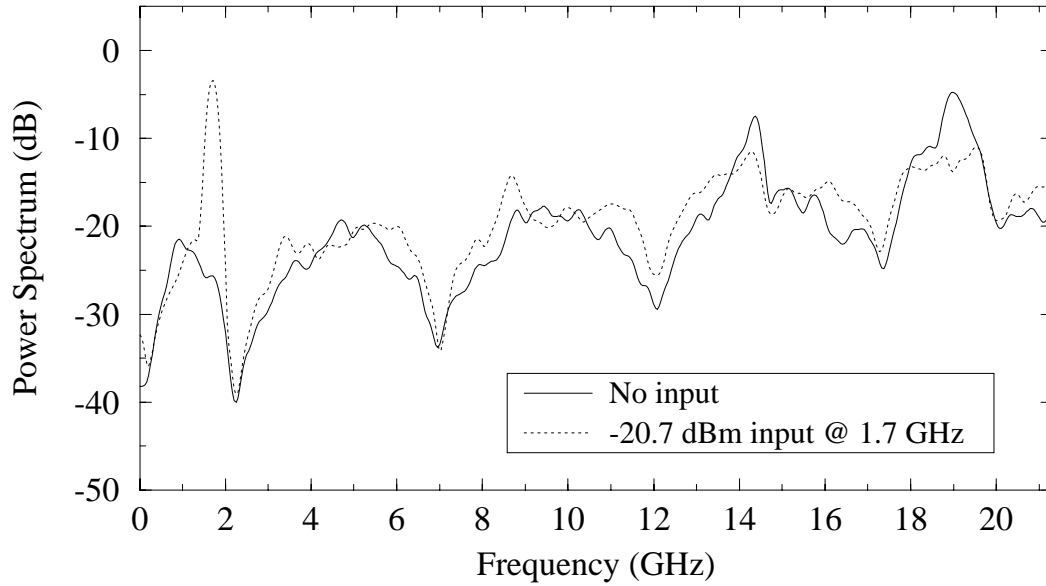


Figure 5: Measured output spectra at 42.6GHz sampling rate.

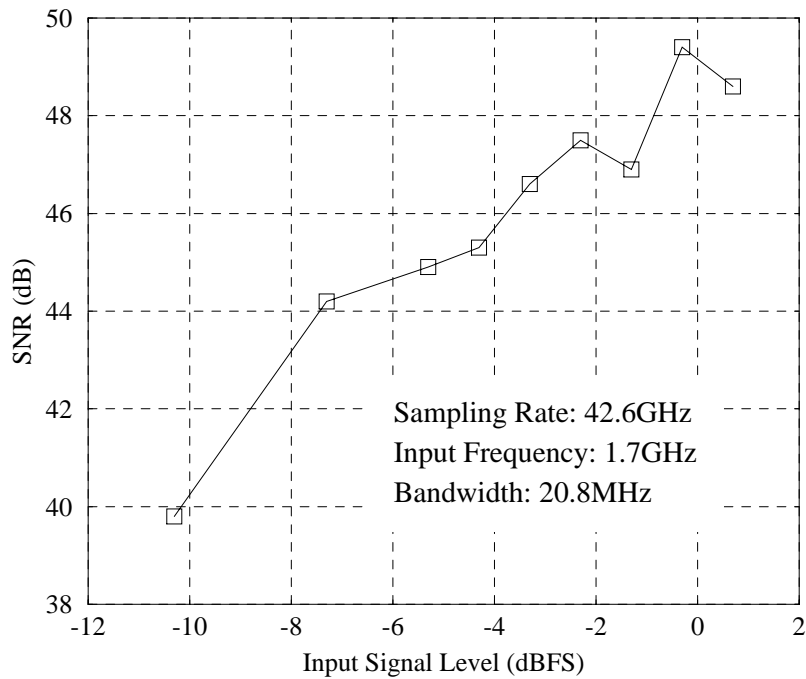


Figure 6: Measured SNR versus input signal level.



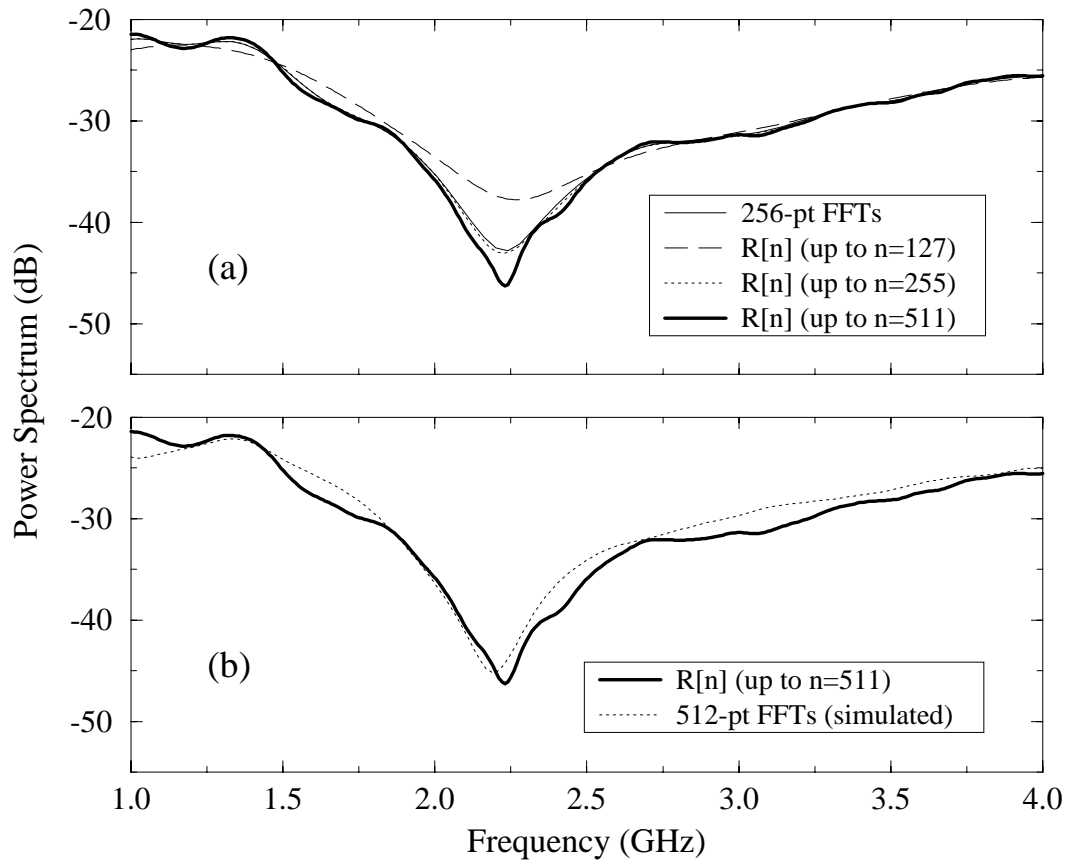


Figure 7: Idle channel spectra obtained by segmented correlation ( $f_s=40.2\text{GHz}$ ).

(a) Comparison with 256-point FFTs of experimental data.

(b) Comparison with 512-point FFTs of simulated data.

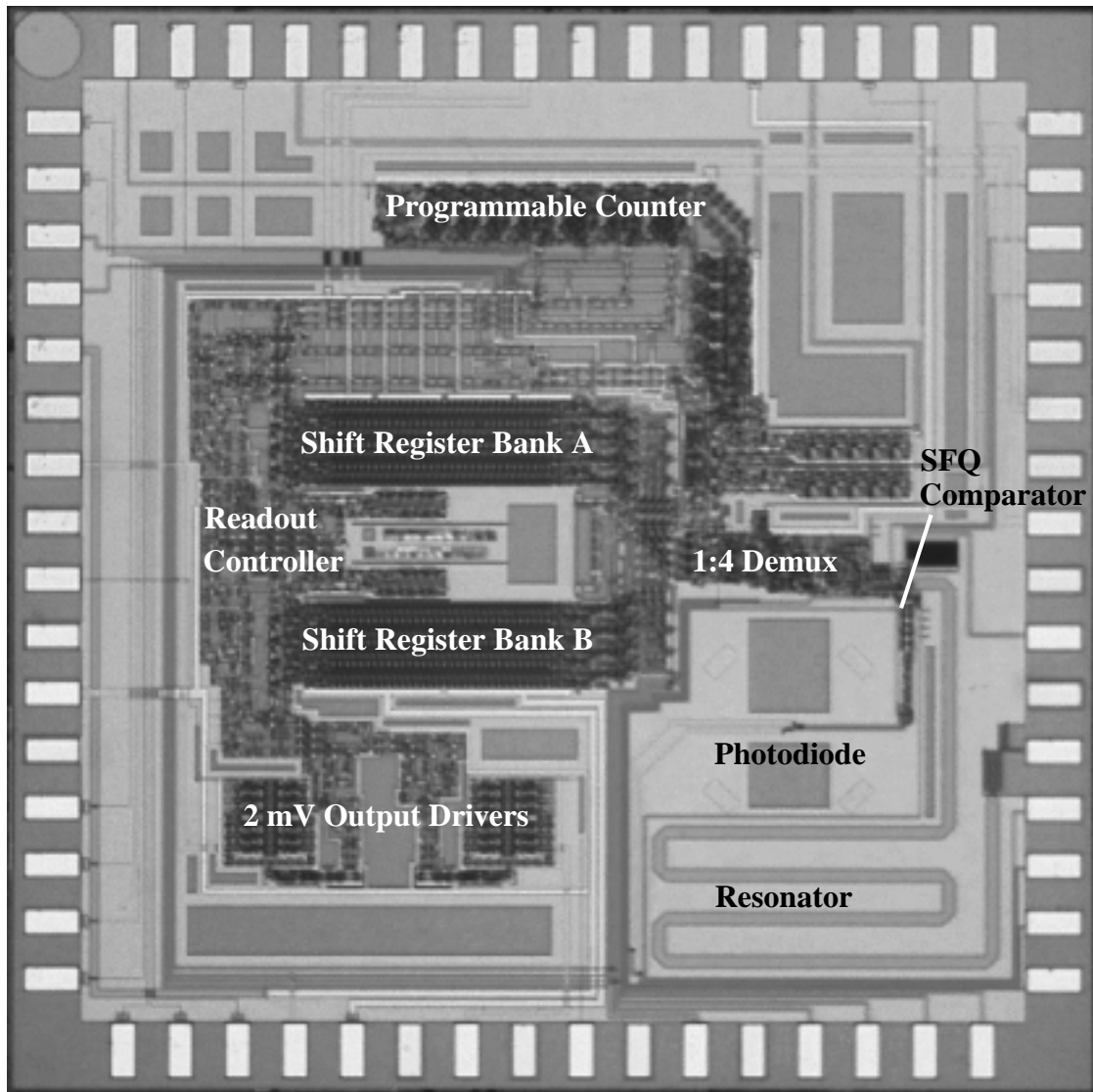


Figure 8: Micrograph of superconducting bandpass  $\Delta\Sigma$  modulator test chip.