RC22343 (W0202-051) February 20, 2002
Materials Science

IBM Research Report

Quarterly Report: November, 2001 – January, 2002

Space and Naval Warfare Systems Center, San Diego

RDT&E Division
for the 1999 Contract N66001-99-C-6000

Investigations of UHV/CVD Deposition of SiGe Alloys on Silicon-on-Sapphire Substrates for Application to Device Fabrication Technology

P. M. Mooney, J. O. Chu, D. V. Singh, S. J. Koester, A. Grill, V. Patel, J. A. Ott
IBM T.J. Watson Research Center
PO Box 218, Yorktown Heights, NY 10598

This report contains limited rights data per FAR 52.227-14.

Research Division
Almaden - Austin - Beijing - Haifa - India - T. J. Watson - Tokyo - Zurich

Fabrication of pMODFET Frequency Divider Circuit

Work continued on the processing of the divider circuit being fabricated on our standard pMODFET layer structure on bulk Si substrates. A set of 4 wafers from the GOVT61 UHVCVD growth run is being processed, with the second wafer a few steps behind the first wafer, and so forth. In November 2001 we reported DC characteristics for individual devices on the first wafer, for which all the fabrication steps through metal 1 had been completed successfully. Unfortunately, this wafer was broken during the final fabrication step to connect the devices in the divider circuit (metal 2). Therefore, further measurements on this wafer were not possible.

On the second wafer, the silicide process used to form the source and drain contacts was not successful. Part of the metal delaminated, probably due to a cleaning problem. The lithography for the following step (metal 1) does not look good; therefore processing on that wafer was stopped. The silicide process was successfully completed on the third wafer, which is now at the lithography step for metal 1.

SOS Materials Evaluation

Two new UHV-CVD growth runs of our standard pMODFET layer structure, GOVT66A and GOVT67A, were done to evaluate the bonded silicon-on-sapphire (SOS) wafers received from Prof. T.F. Kuech at the University of Wisconsin. One bonded SOS wafer was included in each run; the other wafers were bulk Si substrates. The SOS wafer and one bulk Si wafer from each run were evaluated by optical microscopy, high-resolution x-ray diffraction (HRXRD), atomic force microscopy (AFM) and Hall effect measurements. The results are very interesting and show significant improvements compared to the epitaxial SOS wafers used previously for these device structures.

The bulk wafers from the two runs look very similar. Optical microscope images from Gov67A.07, the bulk Si substrate, are shown in Figs. 1 and 2. This wafer looks very similar to previous pMODFET wafers grown in this UHVCVD reactor, except that the large faceted pits seen on the earlier wafers are not present on this one. These pits occur where there is a surface defect, such as a particle. Now that the reactor has been moved into a clean room where the particle density is reduced, we do not expect to see these pits.

Although the two bonded SOS substrates appeared to be similar prior to growth of the pMODFET structure, the two SOS wafers look very different afterwards. To the naked eye the second wafer (SOS2), received toward the end of 2001, appears to be covered with fingerprints, whereas the first wafer (SOS1), received in January of 2001, does not. Figs. 3 and 4 are optical micrographs form Govt67A.08, the SOS2 substrate. A low density of small circular defects, which could be bubbles at the bonded interface or surface pits, is seen on both SOS wafers. The density of the bubbles or surface pits is similar at all the different regions that were investigated on SOS1. In contrast, the density varies considerably at different spots on SOS2. What appears as “fingerprints” to the naked eye are regions with a very high density of bubbles/surface pits, as shown in the

optical micrograph of Fig. 5. The areas between the "fingerprints" have a much lower density of bubbles/pits, as shown in Fig. 6. In addition, beautiful star-like defects can be seen with the naked eye in some areas on this wafer. Examples of this type of defect are shown in the optical micrographs of Figs. 7 and 8. These defects appear to consist of rows of pits on the wafer surface, due to dislocation interactions, presumably due to dislocation interactions at defects in the bonded SOS layer. These star defects were not observed on SOS1.

A third bonded SOS wafer, SOS3, also received from UW toward the end of 2001 (box is labeled SOS431), was examined in the optical microscope. Some areas showed individual bubbles at a very low density as shown in Fig. 9. Other regions show rows of bubbles lying along two perpendicular axes as shown in Fig. 10. Since the oxide form the original SOI wafer is still present, these bubbles clearly result from the wafer bonding process and lie underneath the bonded Si layer. Provided the bonded interface is structurally strong enough that the Si layer does not delaminate, isolated individual bubbles might not significantly affect the UHVCVD growth process or the properties of the layer structure. Because the SiGe buffer layers relax by the glide of misfit dislocations in the bonded Si layer, dislocation pining at bubbles could give rise to bundles of threading dislocations at the wafer surface that show up as surface pits. The intersecting rows of bubbles shown in Fig. 10 may be the sites at which the "star-like" defects observed in the pMODFET structures grown on SOS2 are formed.

Fig. 11 shows an AFM image of the pMODFET on bulk Si. The usual cross hatch pattern is observed. As is seen in Fig. 12, the surface of the pMODFET structure on SOS1 is similar. The RMS roughness is slightly less on the image of the structure on the SOS substrate. The lower value for the RMS roughness on the SOS substrate is expected, since there are fewer rows of pits due to dislocation interactions when the SiGe buffer layer relaxes on this wafer.

Table I summarizes the HRXRD results from a bulk Si and SOS wafer from each growth run. For both growth runs, the structure on the SOS substrate has slightly higher alloy composition and is a little less relaxed. The buffer layers on the two structures on bulk Si substrates appear to be identical.

Table I. Summary of the HRXRD results

Wafer	Substrate	Alloy Composition, x, of Buffer Layer	% Strain Relaxation in Buffer Layer
Govt66A.07	Bulk Si	0.41	87
Govt66A.08	SOS1	0.42	77
Govt67A.07	Bulk Si	0.41	85
Govt67A.08	SOS2	0.43	81

Temperature dependent Hall effect measurements were done on the two wafers from Govt66A and the bulk Si wafer from Govt67A and the results are given in Table II. The data are similar for the pMODFET structures from Govt66A on the bulk Si and SOS substrates with a slightly (6%) higher mobility on the SOS substrate. The mobility on Govt67A.07 (bulk Si substrate) was 35% higher at room temperature and 73% higher at low temperature than that of Govt66A.07 (bulk Si substrate). The low temperature carrier density was 22% lower in Govt67A.07. The reason for this difference is not clear at this time. These room temperature mobility values are similar to those of the wafers on which the divider circuit is currently being fabricated.

In summary, good quality p-MODFET structures were grown on bonded SOS substrates received from UW. Although one wafer had regions with a very high density of bubbles at the interface, both wafers behaved similarly during UHC/CVD epitaxy at about 550 ^{o}C. No large faceted pits were observed on either the bulk Si wafers or the SOS wafers. This is due to the much lower particle density in the clean room, in the case of bulk Si substrates, and the absence of microtwin defects in the bonded SOS layer. The better surface morphology on the SOS wafers, i.e. the reduced density of rows of pits due to dislocation interactions when the SiGe buffer layer relaxes, suggests that device yields on SOS substrates may be higher than on bulk Si. These initial results on bonded SOS wafers are very encouraging.

Table II. Hole Mobility (μ_h) and Sheet Density (n_s)

Wafer	Temperature (K)	μ_h (cm^2/V-s)	n_s (10^{12} cm^{-2})
Govt66A.07 (bulk Si)	300	412	2.82
"	25	2344	1.61
Govt66A.08 (SOS1)	300	439	2.66
"	29	2440	1.88
Govt67a.07 (bulk Si)	300	556	2.95
"	25	4056	1.26

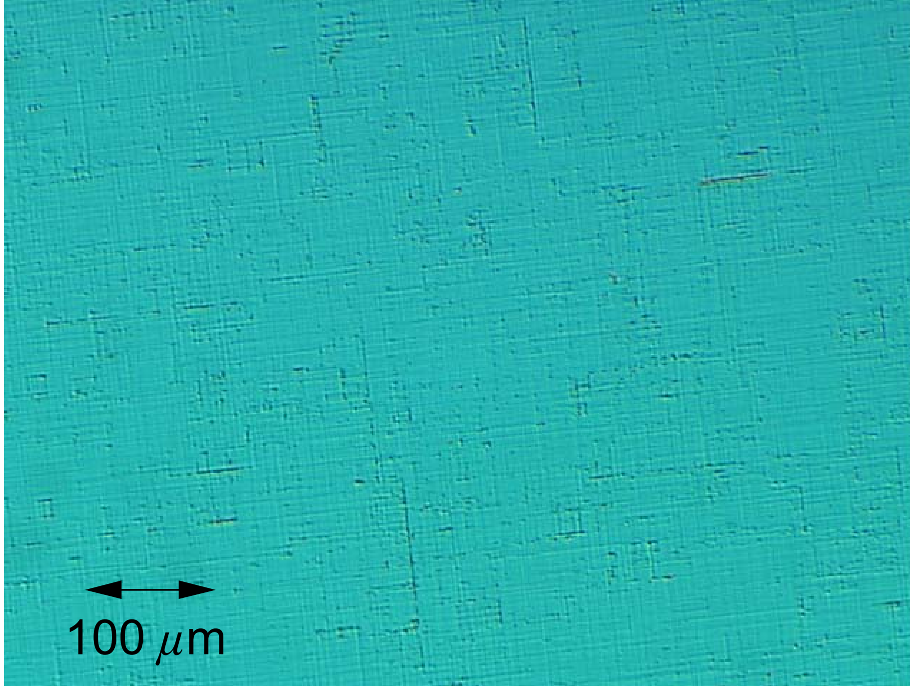

Fig. 1. Low magnification optical micrograph of a pMODFET structure on a bulk Si substrate (Gov67A.07).

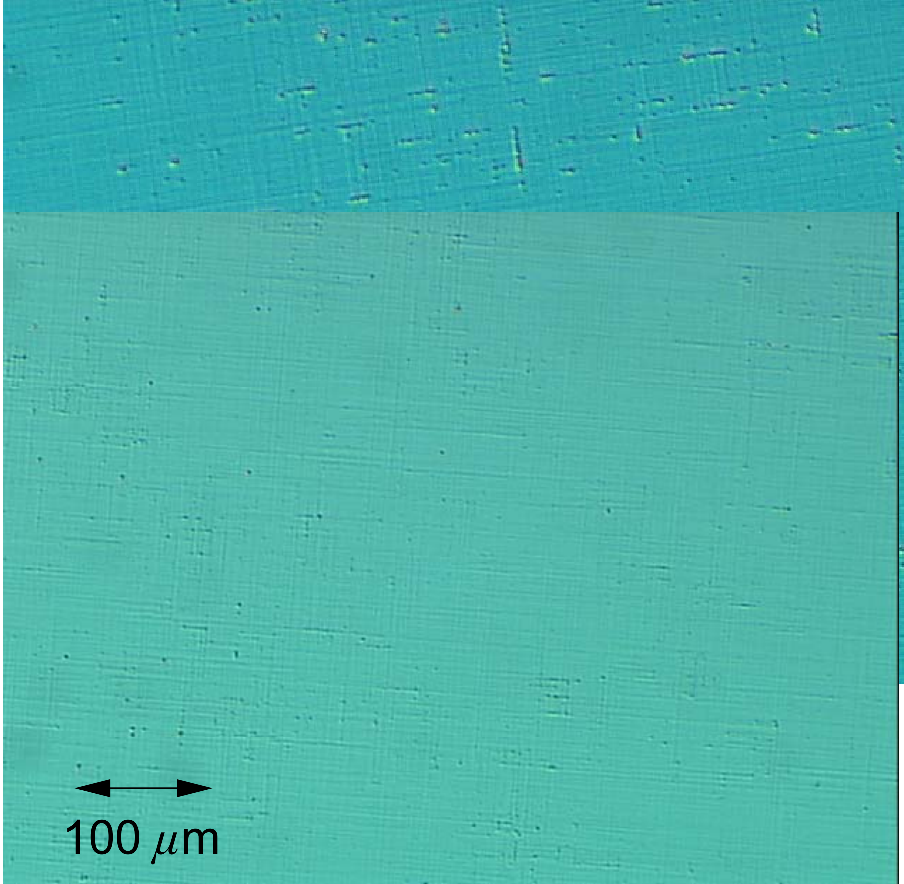

Fig. 2. Higher magnification optical micrograph of the same area as is shown in Fig. 1.

Fig. 3. Low magnification optical micrograph of the pMODFET structure on SOS2, showing an area of the wafer far away from the "fingerprints" (Gov67A.08).

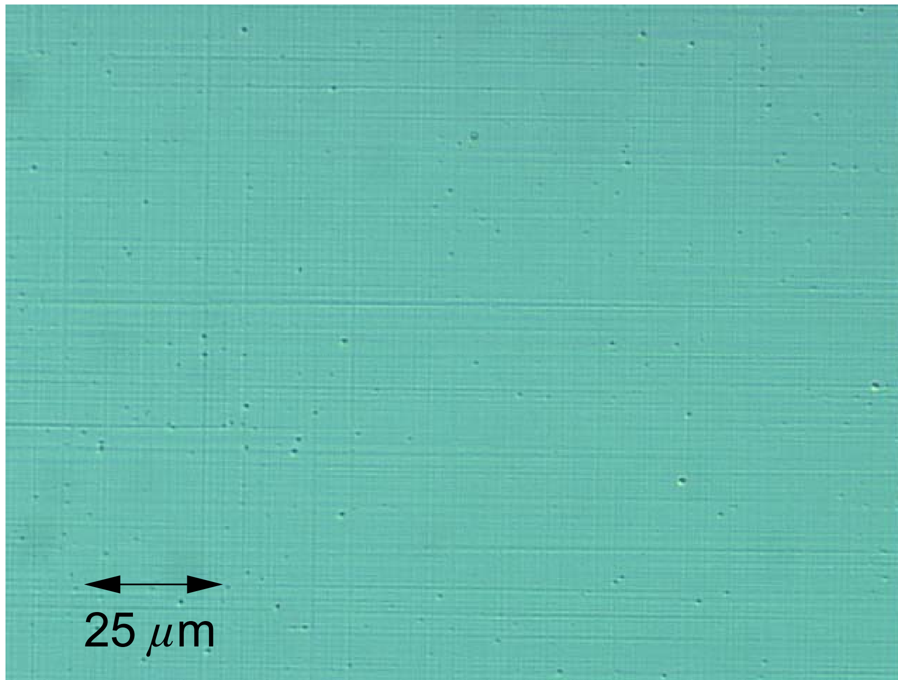

Fig. 4. Higher magnification optical micrograph of the same area as is shown in Fig. 3.

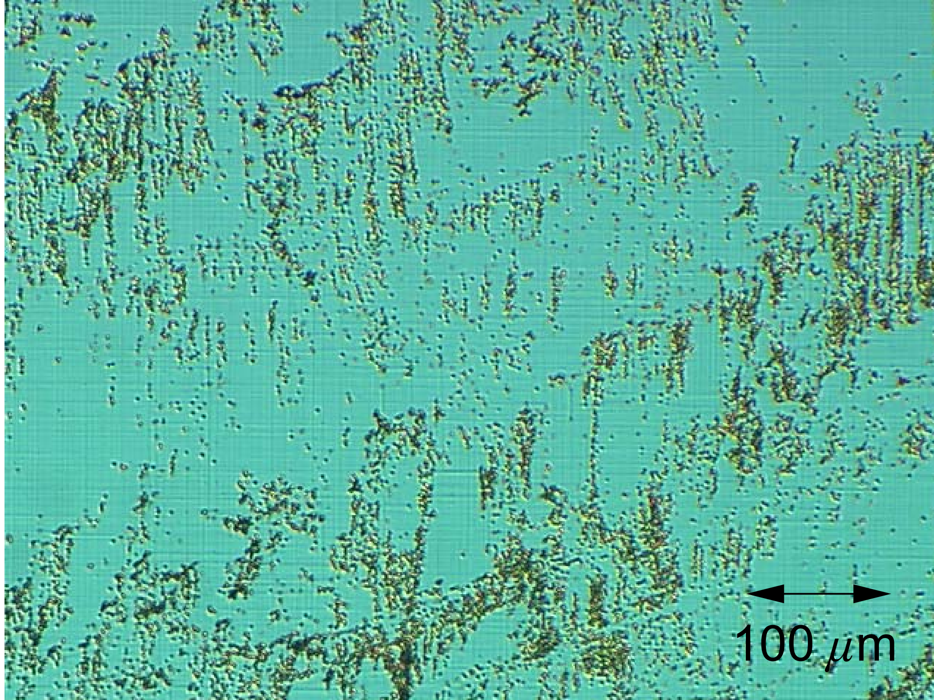

Fig. 5. Optical micrograph showing an area of SOS2 with “fingerprint” (GOV67A.08).

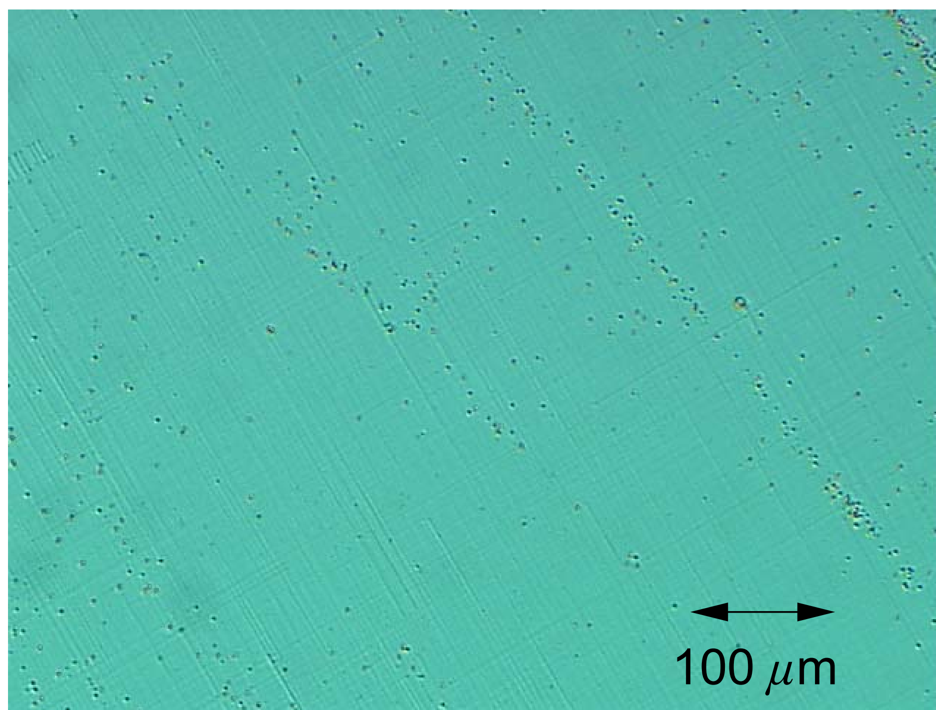

Fig. 6. Optical micrograph showing an area of SOS2 between “fingerprints” (Gov67A.08).

This report contains limited rights data per FAR 52.227-14.

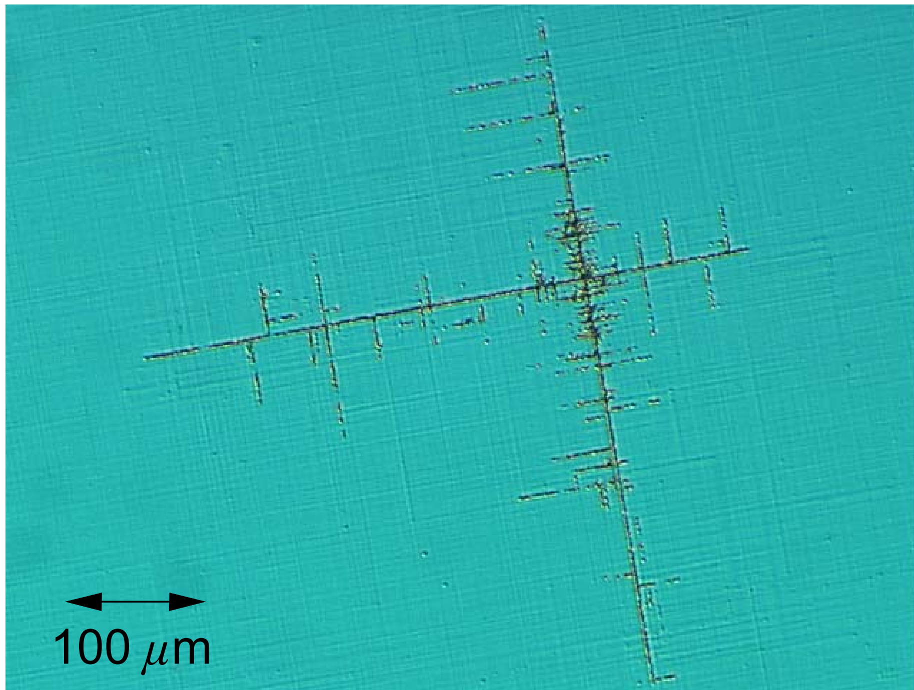

Fig. 7. Optical micrograph showing a large star-like defect on SOS2 (Gov67A.08).

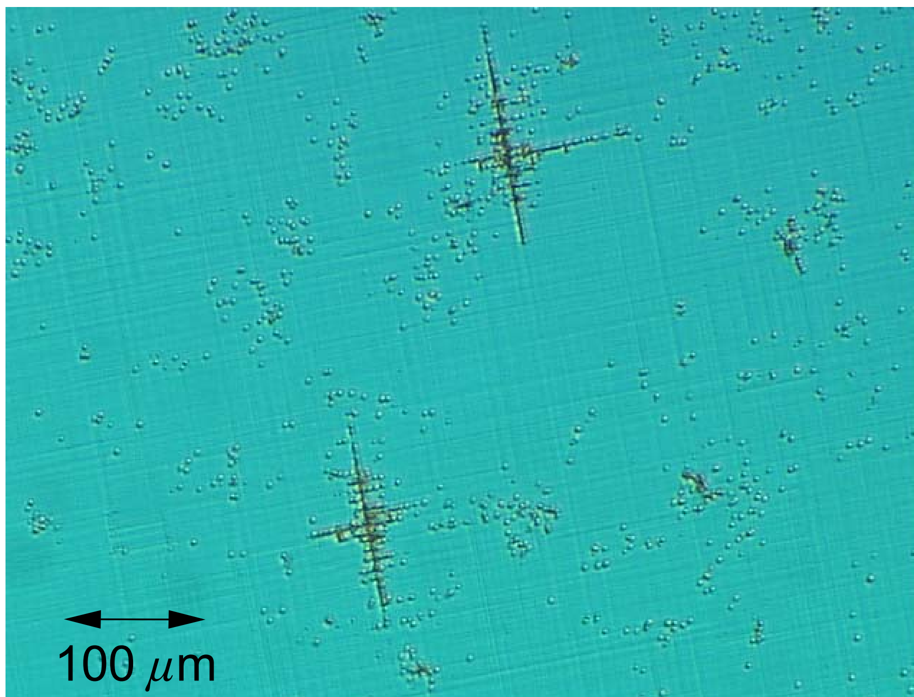

Fig. 8. Optical micrograph showing two small star-like defects on SOS. (Gov67A.08).

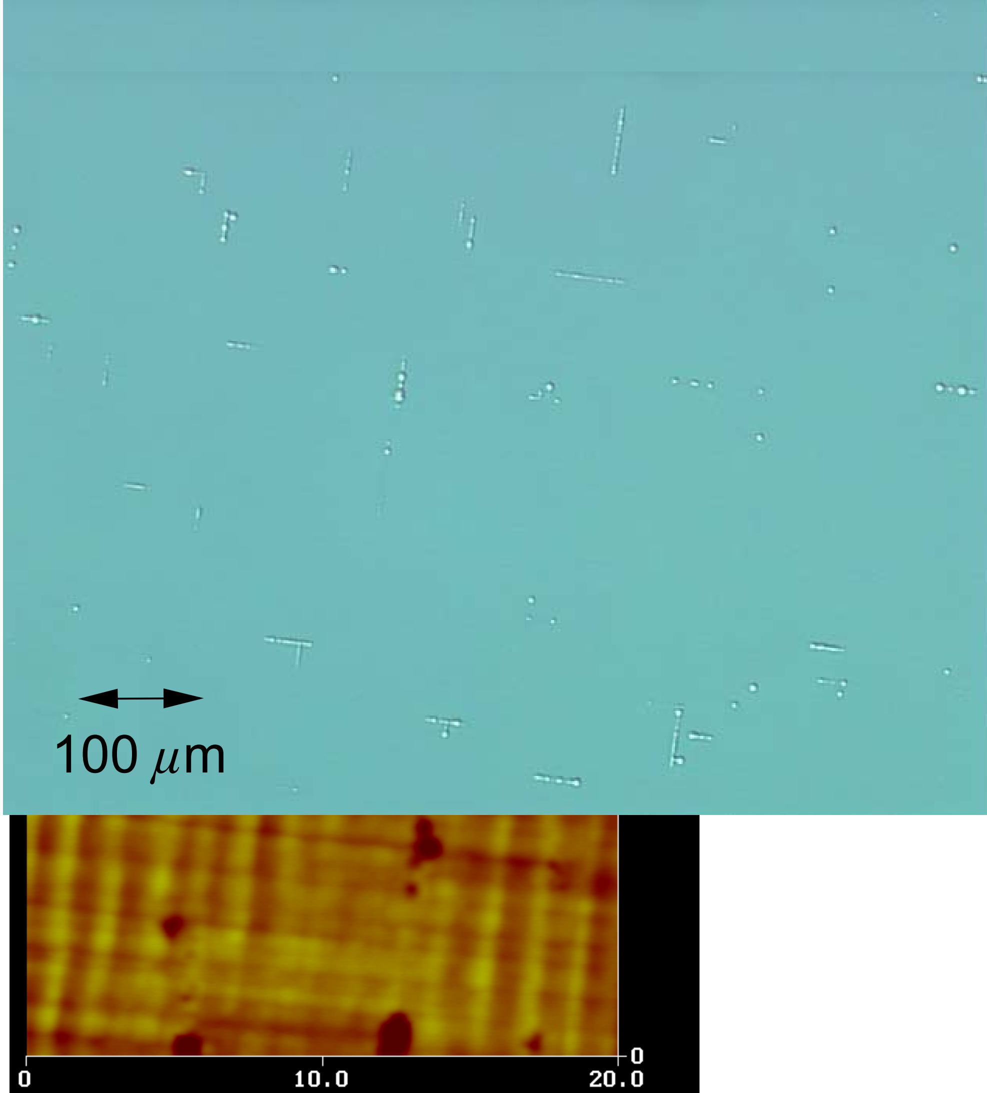

Fig. 9. Optical micrograph of SOS3 as received form UW.

Fig. 10. Optical micrograph of SOS3 as received from UW.

Fig. 11. AFM image of the surface of the p-MODFET structure on bulk Si (Gov66A.07). The Z-range of this image is 98 nm and the RMS roughness is 7.0 nm

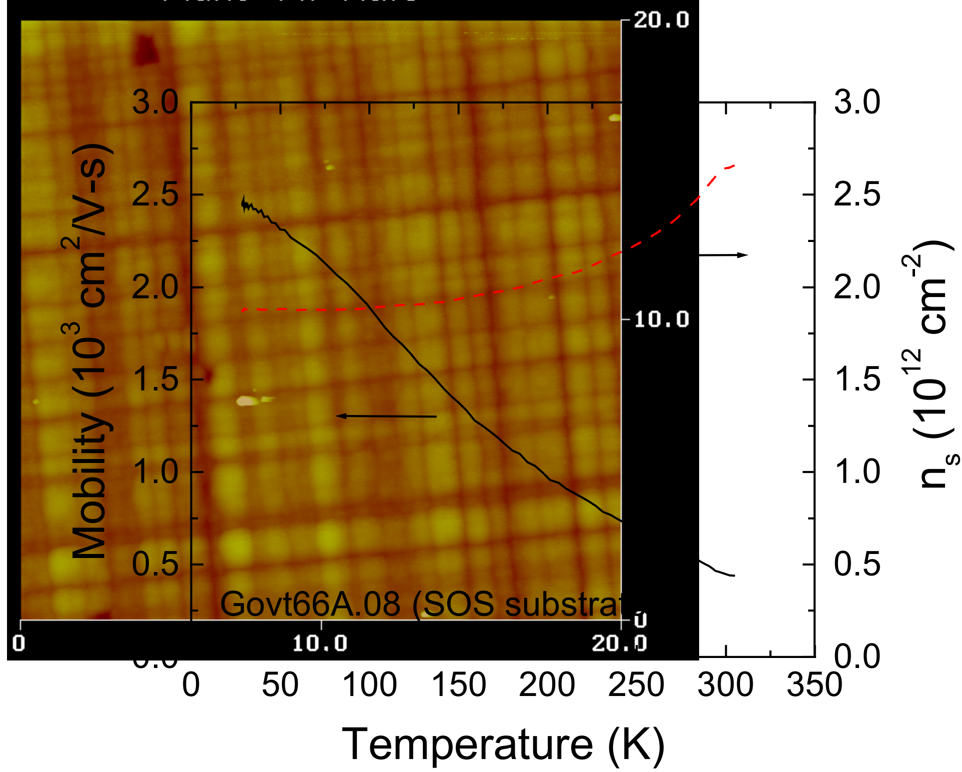

Fig. 12. AFM image of the surface of the p-MODFET structure on SOS1 (Gov66A.08). The Z-range of this image is 104 nm and the RMS roughness is 4.4 nm.

Fig. 13. Hole mobility and sheet density vs. temperature for the pMODFET structure on a bonded SOS substrate.