RC22354 (W0202-061) February 21, 2002
Materials Science

IBM Research Report

Materials for Strained Silicon Devices

Patricia M. Mooney
IBM Research Division
Thomas J. Watson Research Center
P.O. Box 218
Yorktown Heights, NY 10598

Research Division
Almaden - Austin - Beijing - Delhi - Haifa - India - T. J. Watson - Tokyo - Zurich

MATERIALS FOR STRAINED SILICON DEVICES

P.M. Mooney
IBM Research Division, T.J. Watson Research Center
PO Box 218, Yorktown Heights, NY 10549

Strained Si devices exhibit enhanced carrier mobility compared to that of standard Si CMOS devices of the same dimensions. Recent strained Si CMOS device results are reviewed. Materials issues related to the strained Si/relaxed SiGe heterostructures required for a strained Si CMOS technology are discussed.

1. Introduction

The amazing performance improvements in CMOS circuits during the last 40 years are primarily a result of reductions in the dimensions of the individual transistors by orders of magnitude enabled by advances in photolithography. The smaller device size permits a much higher device density that has, for example, resulted in logic chips with clock speeds greater than 1 GHz. As device dimensions approach <100 nm, scaling becomes increasingly difficult. Therefore, new materials that improve circuit performance cost are of interest. Examples of new materials that have been implemented recently are silicon-on-insulator (SOI) wafers, consisting of a thin Si layer separated from the bulk Si substrate by a thin layer of SiO_2 and Cu interconnections.

Improved performance due to increased carrier mobility has been reported for CMOS devices fabricated on a strained Si layer.[1-9] Theoretical calculations predict higher mobility for both electrons and holes in silicon under tensile strain.[10-14] Tensile strain removes the 6-fold degeneracy in the conduction band, lowering the energy of the two Δ valleys having electrons with a lower in-plane effective mass with respect to the four Δ valleys having electrons with a higher in-plane effective mass. This energy splitting reduces intervalley scattering and preferential occupation of the two Δ valleys with lower in-plane effective mass electrons results in higher electron mobility. Tensile strain also removes the valence band degeneracy at the Gamma-point and shifts the spin-orbit band,[1-5] thus improving the hole mobility. Typically a Si layer under tensile strain is achieved by epitaxial growth of Si on a strain-relaxed SiGe buffer layer on a Si substrate. The relaxed SiGe buffer layer serves as a "virtual substrate" for these devices. The electron mobility increases with increasing Ge mole fraction in the SiGe buffer layer, saturating at about 20% Ge.[11] The hole mobility increases more slowly and saturates at about 35% Ge.[14] Therefore structures consisting of strained Si on a relaxed SiGe buffer layer containing 15-35% Ge are interesting for CMOS applications.

Fig. 1 shows a cross section of a SSCMOS device fabricated on a 200 mm wafer using a CMOS fabrication process that was modified to accommodate the SiGe buffer layer.[7] The electron mobility measured on large area, long channel devices on SiGe buffer layers having 15 and 20 % Ge is shown in Fig. 2. The mobility of the strained Si device is about 70% higher than the universal MOSFET mobility than the mobility of control Si devices and it increases with increasing Ge content in the buffer layer as expected.[7] The mobility enhancement, which persists at high vertical field in the range

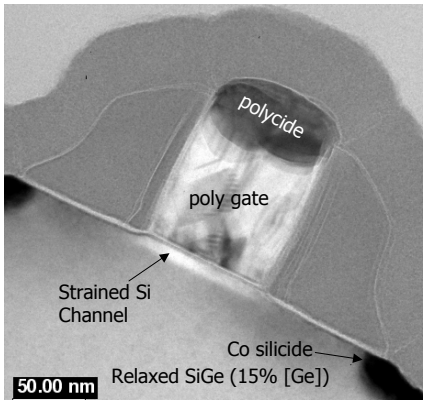

Fig. 1. Cross sectional TEM image of a fabricated strained Si MOSFET. [7] (© 2001 IEEE)

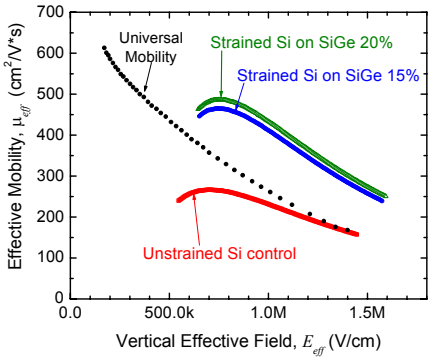

Fig. 2. Effective electron mobility of strained Si MOSFETs.[7] (© 2001 IEEE)

required for future CMOS generations, cannot be explained entirely by the band structure modifications, indicting that the tensile strain may also reduce the so-called surface roughness scattering.[7,11] This mobility enhancement is very exciting. However, there are still many questions related to process integration and materials issues to be addressed. In this paper recent work on the strained Si/relaxed SiGe structures required for strained Si devices are discussed.

2. Strain-relaxed SiGe buffer layers on Si (001)

An essential feature of strained Si CMOS device structures is the strain-relaxed SiGe buffer layer or virtual substrate. The alloy composition and degree of strain relaxation of the SiGe buffer layer determines the magnitude of the strain in the pseudomorphic Si cap layer. Moreover, the defect density in the upper part of the buffer layer must be sufficiently low to achieve the necessary yield of devices with good characteristics. When the epitaxial strained layer exceeds a critical thickness, strain relaxation occurs in $Si_{1-x}Ge_x$/Si(001) having $x<0.5$ by the introduction of 60° misfit dislocations near the SiGe/Si interface. Since Si(001) substrates are essentially dislocation free, the critical thickness in this case is that needed for dislocation nucleation; the critical thickness decreases as the Ge mole fraction of the SiGe layer is increased and also depends on the growth temperature.[16-18] A relatively thick SiGe layer may remain fully strained (pseudomorphic) when grown at low temperature; however, strain relaxation occurs when a metastable structure is subsequently heated, e.g. during device fabrication.

Since dislocations must terminate at a free surface, each 60° misfit dislocation nucleated at the initial growth interface or in the epitaxial layer ends with two threading arms that go through the SiGe layer to the wafer surface. Relatively low threading dislocation densities have been achieved by means of compositional grading. The graded buffer typically consists of a compositionally graded SiGe layer followed by a uniform composition SiGe layer. The alloy composition may be linearly graded or step-wise

graded. Threading dislocation densities in the range 10^5-10^8 cm^{-2} have been reported, with the lowest densities occurring for grading rates as slow as 10% Ge per micron of layer thickness.[19] Thus graded $Si_{1-x}Ge_x$ buffer layers for strained Si CMOS applications may be as thick as 2-4 μm. Because SiGe has a lower thermal conductivity than Si, self-heating effects are observed in strained Si CMOS devices fabricated on step-graded buffer layers.[7] Graded buffer layers also have relatively rough surfaces; a cross hatch surface pattern is created by the surface steps associated with the 60° misfit dislocations. The surface of the relaxed SiGe buffer layer can be planarized prior to the growth of the active device layers using chemical-mechanical polishing methods. However, the polishing step adds to the cost of fabrication, as does the growth of such a thick SiGe buffer layer.

For these reasons, alternative methods to achieve a much thinner relaxed SiGe buffer layer are under investigation.[20-24] One approach, using molecular beam epitaxy (MBE), employs a special low temperature (200 °C) growth step.[20] Another approach, also by MBE, uses plasma cleaning prior to growth.[21] Ion-implantation of hydrogen or helium has been used to create dislocation nucleation sources and thus enhance strain relaxation in thin SiGe/Si structures.[22-24] In this method, a pseudomorphic SiGe layer is first grown on Si(001) at low temperature. The SiGe layer must be thin enough that no strain relaxation occurs during the growth, but thick enough that it exceeds the critical thickness for relaxation at higher temperatures. Hydrogen or helium is then implanted at or below the SiGe/Si interface. After annealing, spherical defects (bubbles) were observed at or below the SiGe/Si interface as well as a dense network of misfit dislocations that relieve the strain in the SiGe layer.

We have investigated strain relaxation mechanisms in He-implanted SiGe/Si structures.[25] Depending on the He dose and implantation energy, i.e. the depth of the He atoms below the SiGe/Si interface, three different strain relaxation mechanisms were observed, as shown in Fig. 3. For some implant conditions, we observed that platelets are formed upon annealing (group 2 samples) rather than bubbles (groups 1 and 3) as reported previously. Dislocations nucleate at the platelets by a prismatic punching mechanism as seen in Fig. 4, and a dense regular misfit dislocation network is formed at the SiGe/Si interface as shown in Fig. 5. Dislocations that terminate at platelets or bubbles below the SiGe/Si interface do not have threading arms running through the SiGe layer. Therefore implanted/annealed buffer layers are expected to have low threading dislocation densities. Threading dislocation densities comparable to those found for graded buffer layers have been reported.[22-24]

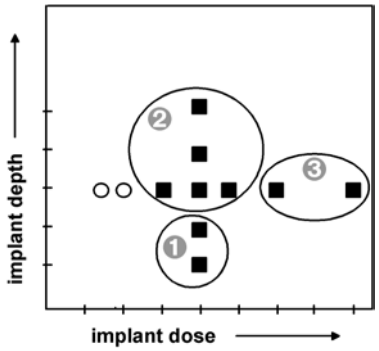

Fig. 3. Plot showing strain relaxation at various implant doses and depths below the SiGe/Si interface for both $Si_{0.85}Ge_{0.15}$ and $Si_{0.80}Ge_{0.20}$ samples: circles indicate layers that relaxed only slightly (<10%), squares indicate samples having substantial (30-80%) relaxation. The more relaxed samples are grouped according to the strain relaxation mechanism .[25]

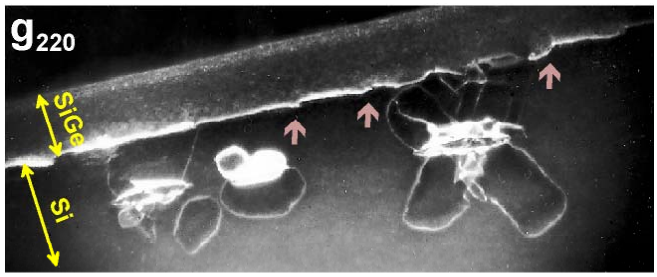

Fig. 4. Cross-sectional TEM micrograph (weak beam conditions) showing platelets below the SiGe/Si interface. Dislocation loops extend from the platelets in all eight <110> directions and glide to form misfit dislocation segments at the interface as indicated by arrows.[25]

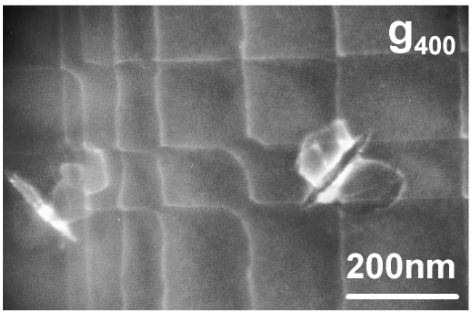

Fig. 5. Planar view TEM micrograph (weak beam conditions) showing platelets along the <100> directions below the SiGe/Si interface with a regular array of 60^0 misfit dislocations, having line directions parallel to the <110>-directions at the interface.[25]

3. SiGe-on-insulator substrates

The advantages of strained Si can be combined with the advantages of SOI substrates by fabricating SiGe-on-insulator (SGOI) substrates. Several different methods to fabricate SGOI using a relaxed SiGe buffer layer on Si(001) have been implemented. One group fabricated SGOI substrates by means of a SIMOX-like process, i.e. implantation of oxygen below the surface of the SiGe buffer layer and then annealing at high temperature (>1300 ^{o}C) to form a layer of SiO_2.[26,27] Apparently this method works only for SiGe buffer layers having low (~10%) Ge. Another approach uses dry oxidation at high temperature after deposition of a pseudomorphic SiGe layer with low Ge content.[28] During oxidation, Ge atoms are rejected from the oxide and condensed in the remaining SiGe layer, which is partially relaxed without introducing a significant number of dislocations. Raman spectroscopy shows that a strained Si cap layer grown on such a structure has about 1% tensile strain.

Wafer bonding and layer transfer is a very promising method to fabricate SGOI substrates with higher Ge content.[8,29,30] The fabrication steps are shown schematically in Fig. 6; and involve implantation of hydrogen into the relaxed SiGe buffer layer, then bonding the implanted wafer to a Si wafer with an SiO_2 layer on top, then annealing to split the SiGe layer and strengthen the bonded interface, and finally epitaxial growth of the strained Si device layers on the bonded SGOI substrate. Key process steps not shown explicitly in Fig. 6 include chemical-mechanical polishing to planarize the surface of the relaxed SiGe buffer layer and subsequent cleaning of the polished surface prior to bonding and also after layer splitting before growing the device layers. Temperature

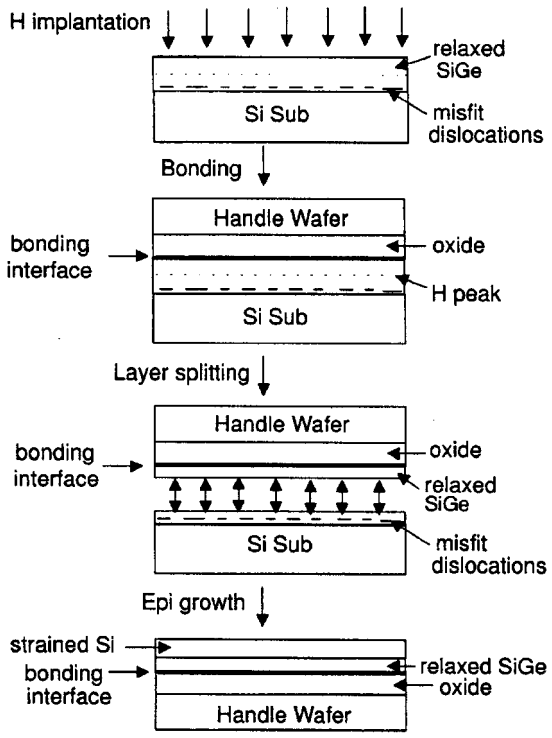

Fig. 6. Diagram showing fabrication steps for bonded SGOI substrates.[29]

dependent Hall effect measurements performed on modulation-doped structures grown simultaneously on a polished SiGe buffer layer and on a polished SGOI substrate having the same SiGe alloy composition show the presence of a two dimensional electron gas and identical electron mobility, ~2000 cm2/V-s at 300 K.[29] This indicates that the quality of the SiGe layer on the bonded SGOI wafer is the same as that of the relaxed SiGe buffer layer used to fabricate the SGOI wafer.

The effective electron mobility in strained Si MOSFETS fabricated on a bonded SGOI substrate having 15% Ge is shown in Fig. 7. An enhancement of about 50% is observed,[8] comparable to the results for strained Si MOSFETs on thick relaxed SiGe buffer layers on bulk Si substrates[7] Fig. 8 shows the effective hole mobility in MOSFETs fabricated on a bonded SGOI substrates having 25% Ge. This work extends earlier results[6] to higher effective vertical field. Hole mobility enhancements of 15-20% were found at low vertical field:[8] at high vertical field, however, there is negligible mobility enhancement, suggesting that SGOI wafers with higher Ge content are desirable.

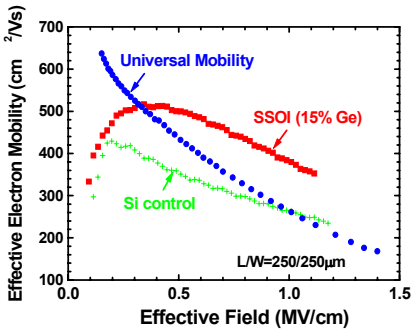

Fig. 7. Electron mobility in strained Si MOSFETs on a bonded SGOI substrate.[8] (© 2001 IEEE)

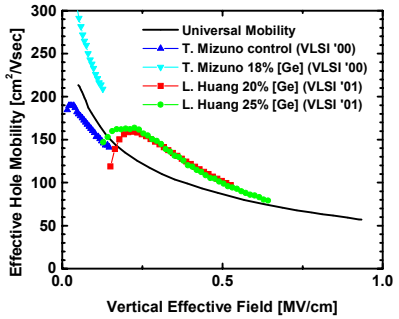

Fig. 8. Hole mobility in strained Si MOSFETs on a bonded SGOI substrate.[8] (© 2001 IEEE)

4. Thermal stability of strained Si structures

Strained Si CMOS devices, implemented by the epitaxial growth of a 10-30 nm-thick strained Si layer on a relaxed $Si_{1-x}Ge_x$ buffer layer on Si(001), are typically grown by a variety of epitaxial methods at relatively low temperatures. However, device fabrication includes standard processes, e.g. the activation of ion-implanted dopant atoms and gate oxidation, requiring temperatures as high as 1000 ^{o}C. When threading dislocations are present in the substrate, an epitaxial strained layer that exceeds the critical thickness for dislocation glide will relax by the formation of misfit dislocations at the Si/SiGe interface.[31] The rate of misfit dislocation formation increases exponentially with temperature. Interdiffusion at the Si/SiGe interface also occurs at this temperature, resulting in a graded interface and effectively reducing the thickness of the strained Si layer. We have investigated these effects by annealing $Si/Si_{1-x}Ge_x$ structures, consisting of a strained Si cap layer of varying thickness on a strain-relaxed step-graded $Si_{1-x}Ge_x$ buffer layer of varying $Si_{1-x}Ge_x$ alloy concentration, at 1000 ^{o}C for 5, 30 and 300 seconds, times which far exceed those normally used for Si CMOS fabrication.[32] The goal of this work was to measure the magnitude of the strain relaxation of the Si layer and the interdiffusion that occurs at the Si/SiGe interface during annealing.

High-resolution x-ray diffraction (HRXRD) was used to determine both the thickness and strain of the Si cap layer. X-ray diffraction measurements were performed at beamline X20 at the National Synchrotron Light Source at Brookhaven National Laboratory using a triple-axis configuration as described previously.[33] The composition and strain of the uniform $Si_{1-x}Ge_x$ layer were determined from the 004 and 224 (grazing exit) reflections. The 004 reflection measures the crystal lattice spacing in the direction of the surface normal, i.e. the out-of-plane lattice spacing. The 224 reflection measures the spacing of lattice planes at an angle to the surface normal, i.e. a set of planes whose lattice spacing has both an out-of-plane and an in-plane component. The composition and the strain are calculated from the angular separation between the SiGe layer and the Si substrate peaks in the two measurements.[33]

Fig. 9 shows the 004 data for a 21 nm-thick Si cap layer on a $Si_{0.72}Ge_{0.28}$ buffer layer taken at two different regions, one with and one without the strained Si cap layer. Comparing the two scans, the features to the right of the Si substrate peak are from the

strained Si cap layer. Although the Si layer thickness can be determined from the solid curve in Fig. 9, comparison with the simulation is more precise when the two scans are subtracted. The difference of the two scans in Fig. 9 is shown in Fig. 10, along with a simulated diffraction scan from RADS.[34] The thickness of the Si cap layer determines the spacing of the oscillations and the strain determines their position with respect to the Si substrate peak. The shift of the experimental data from the Si cap layer with respect to the Si substrate peak is clearly visible. With this method of analysis the strain in the Si cap layer can be determined to within 1 or 2%, depending on the sample.

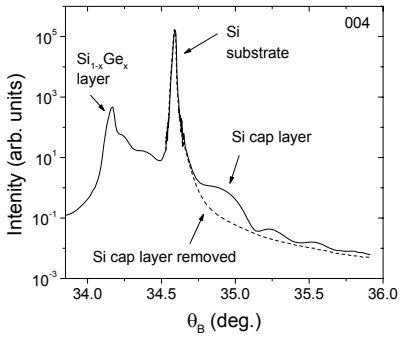

Fig. 9. 004 x-ray scan taken at regions with and without the 21nm-thick strained Si cap layer on $Si_{0.72}Ge_{0.28}$.[32]

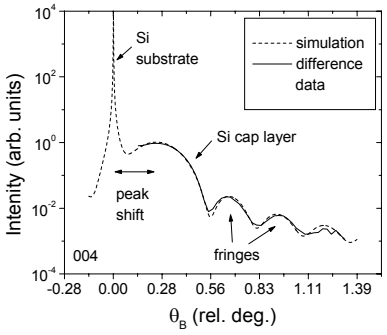

Fig. 10. The difference of the two x-ray scans shown in Fig. 8 with the simulated x-ray data.[32]

As was expected from previous Raman spectroscopy measurements on the same samples,[35] x-ray diffraction results show that the thickness of the Si cap layer decreases with the annealing time (see Fig. 11). The change in the Si cap layer thickness showed no dependence on the initial thickness of the Si cap layer or the alloy composition of the SiGe layer over the ranges investigated.[32] Since these samples were annealed in an inert atmosphere, the most likely explanation is that interdiffusion occurs at the $Si/Si_{1-x}Ge_x$ interface, effectively reducing the thickness of the pure Si layer. These changes in thickness are consistent with experimental values for the diffusion coefficients reported for Ge in Si.[36-37] Interdiffusion results in a graded interface rather than the abrupt one achieved during epitaxial growth at low temperature. This is an advantage for the pMOSFETs, since a graded interface reduces the probability of parallel hole conduction in the top of the relaxed $Si_{1-x}Ge_x$ buffer layer.[3]

Fig. 12 shows the time dependence of the strain relaxation for two samples. The Si cap layer is 0% relaxed when the in-plane lattice parameter matches that of the underlying $Si_{1-x}Ge_x$ layer and it is fully relaxed when the in-plane lattice parameter has the value of bulk Si. Even in the worst case, very little strain relaxation occurs (~10%), consistent with previous Raman scattering measurements on the same samples.[35] The trends observed are exactly as expected; greater relaxation occurs for higher Ge mole fraction and for thicker Si layers. The x-ray results agree well with the strain relaxation calculated from the misfit dislocation density determined from planar view TEM images.[32] TEM images also clearly show that the misfit segments terminate at threading dislocations in the upper part of the $Si_{1-x}Ge_x$ buffer layer, indicating that strain relaxation occurs by the glide of threading dislocations in the relaxed $Si_{1-x}Ge_x$ layer.

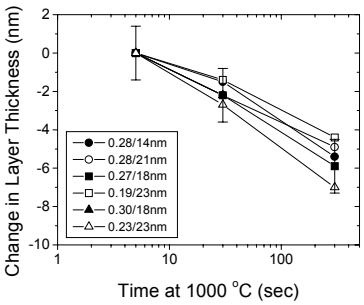

Fig. 11. Change in strained Si layer thickness with annealing time in samples having initial Si layer thickness and $Si_{1-x}Ge_x$ alloy Composition indicated.[32]

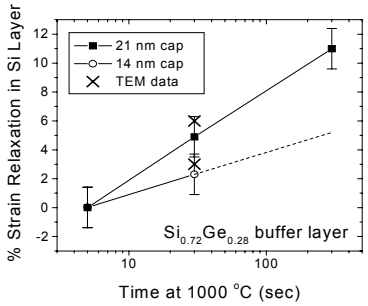

Fig. 12. % strain relaxation as a function of annealing time. Strain relaxation calculated from the misfit dislocation density from planar view TEM images is also plotted.[32]

5. Conclusions

Strained Si CMOS devices fabricated on 200 mm wafers using standard CMOS fabrication processes exhibit increased carrier mobility due primarily to the modified band structure in Si under tensile strain. These devices were fabricated in a strained Si layer grown epitaxially on a strain-relaxed SiGe layer that acts as a virtual substrate. The relaxed SiGe layer may also be the thin SiGe layer of an SGOI substrate. No matter how the virtual substrate is fabricated, the defect density in the relaxed SiGe buffer layer must be sufficiently low to achieve device yields required for the desired applications of strained Si CMOS technology, e.g., ULSI logic circuits. To avoid the formation of misfit dislocations at the strained Si/SiGe interface during device fabrication, the strained Si/SiGe heterostructures must be thermodynamically stable, i.e., the strained Si layer thickness must be less than the critical thickness for dislocation glide. If metastable heterostructures are used, device fabrication process conditions must be restricted to temperatures and times for which dislocation glide is negligible.

Acknowledgements

The contributions of many IBM colleagues to the work discussed in this paper are gratefully acknowledged. The work at NSLS is partially supported by the Dept. of Energy, Materials Science and Chemical Science Divisions.

References

1. J. Welser, J.L. Hoyt, S. Takagi and J.F. Gibbons, “Strain Dependence of the Performance Enhancement in Strained-Si n-MOSFETs”, IEDM Tech Dig. (1994) 373-6.
2. D.K. Nayak, K. Goto, A. Yutani, J. Murota and Y. Shiraki, “High Mobility Strained Si pMOSFETs”, IEEE Trans. Elect. Dev. **43** (1996) 1709-16.

3. K. Rim, J. Welser, J.L. Hoyt and J.F. Gibbons, “Enhanced Hole Mobilities in Surface Channel Strained Si p-MOSFETs”, IEDM Tech Dig. (1995) 517-20.
4. K. Rim, J.L. Hoyt and J.F. Gibbons, “Transconductance Enhancement in Deep Submicron Strained-Si n-MOSFETs”, IEDM Tech. Dig. (1998) 707-10.
5. T. Mizuno, S. Takagi, N. Sugiyama, J. Koga, T. Tezuka, K. Usuda, T. Hatakeyama, A. Kurobe and A. Toriumi, “High Performance Strained Si pMOSFETs on SiGe on Insulator Substrates Fabricated by SIMOX Technology”, IEDM Tech. Dig. (1999) 934-6.
6. T. Mizuno, N. Sugiyama, H. Satake, S. Takagi, “Advanced SOI MOSFETs with Strained Si Channel for High Speed CMOS Electron/Hole Mobility Enhancement”, Symposium on VLSI Technology Dig. (2000) 210-11.
7. K. Rim, S. Koester, M. Hargrove, J. Chu, P.M. Mooney, J. Ott, T. Kanarsky, P. Ronsheim, M. Ieong, A. Grill, H.-S.P. Wong, “Strained Si NMOSFETs for High Performance CMOS Technology” Symposium on VLSI Technology Dig. (2001) 59-60.
8. L.J. Huang, J.O. Chu, S.A. Goma, C.P. D’Emic, S.J. Koester, D.F. Canaperi, P.M. Mooney, S.A. Cordes, J.L. Speidell, R.M. Anderson, H.-S.P. Wong, “Carrier Mobility Enhancement in Strained Si-on-Insulator Fabricated by Wafer Bonding”, Symposium on VLSI Technology Dig. (2001) 57-58.
9. N. Sugii, D. Hisamoto, K. Washio, N. Yokoyama and S. Kimura, “Enhanced Performance of Strained-Si MOSFETs on CMP SiGe Virtual Substrate”, IEDM Tech. Dig. (2001) 737-40.
10. M.V. Fischetti and S.E. Laux, “Band Structure, Deformation Potentials, and Carrier Mobility in Strained Si, Ge, and SiGe Alloys”, J. Appl. Phys. **80** (1996) 2234-52.
11. S. Takagi, J.L. Hoyt, J.J. Welser, and J.F. Gibbons, “Comparative Study of Phonon-Limited Mobility of Two-Dimensional Electrons in Strained and Unstrained Si Metal–Oxide–Semiconductor Field-Effect Transistors”, J. Appl. Phys. **80** (1996) 1567-77.
12. J.B. Roldán, F. Gámiz, J.A. López-Villanueva, and J.E. Carceller, “A Monte Carlo Study on the Electron-Transport Properties of High-Performance Strained-Si on Relaxed $Si_{1-x}Ge_x$ Channel MOSFETs”, J. Appl. Phys. **80** (1996) 5121-28.
13. G. Formicone, D. Vasileska and D.K. Ferry, “Transport in the Surface Channel of Strained Si on a Relaxed $Si_{1-x}Ge_x$ Substrate”, Solid State Elec. **41** (1997) 879-85.
14. R. Oberhuber, G. Zandler and P. Vogel, “Subband Structure and Mobility of Two-Dimensional Holes in Strained Si/SiGe MOSFETs”, Phys. Rev. B **58** (1998) 9941-8.
15. D.K. Nayak, J.C.S. Woo, J.S. Park, K.L. Wang and K.P. MacWilliams, “High-mobility p-channel metal-oxide-semiconductor field-effect transistor on strained Si”, Appl. Phys. Lett. **62** (1993) 2853-5.
16. J.W. Matthews, S. Mader, and T.B. Light, “Accomodation of Misfit Across the Interface Bewteen Crystals of Semiconduction Elements or Compounds” J. Appl. Phys. 70 (1970) 3800-04; J.W. Matthews, A.E. Blakeslee and S. Mader, “Use of Misfit Strain to Remove Dislocations From Epitaxial Thin Films”, Thin Solid Films **33** (1976) 253-66.
17. J.C. Bean, L.C. Feldman, A.T. Fiory, S. Nakahara and I.K. Robinson, “Ge_xSi_{1-x}/Si Strained-Layer Superlattice Grown by Molecular Beam Epitaxy”, J. Vac. Sci. Technol. A **2** (1984) 436-440; R. Hull, “Metastable Strained Layer Configurations in the SiGe/Si System” in *Silicon Germanium and SiGe:Carbon,* EMS Datareviews Series No. 24, INSPEC, London (2002) 21-41.
18. S.R. Stiffler, J.H. Comfort, C.L. Stanis, D.L. Harame and E. de Fresart, “The Thermal Stability of SiGe Films Deposited by Ultra-High Chemical Vacuum Vapor Deposition”, J. Appl. Phys. **70** (1991) 1416-20.
19. P.M. Mooney, “Strain Relaxation and Dislocations in SiGe/Si Structures”, Materials Science and Engineering Reports, **R17** (1996) 105-146, and references therein.
20. M. Bauer, K. Lytovich, M. Oehme, E. Kasper, H.J. Herzog, F. Ernst, “Relaxed SiGe Buffers with Thickness below 0.1 Micometers”, Thin Solid Films **369** (2000) 152-156.
21. J. Kuchenbecker, H. Kibbel, P. Muthsam, U Konig, “Thin SiGe Buffer Layer Growth by In Situ Low Energy Hydrogen Plasma Preparation”, Thin Solid Films **389** (2001) 146-152.

22. D.M. Follstaedt, S.M. Meyers, S.R. Lee, "Cavity–Dislocation Interactions in Si–Ge and Implications for Heterostructure Relaxation", Appl. Phys. Lett. **69** (1996) 2059-61.
23. S. Mantl, B. Hollaender, R. Leidtke, S. Mesters, H.J. Herzog, H. Kibble, T. Hackbarth, "Strain Relaxation of Epitaxial Layers on Si(001) Improved by Hydrogen Implantation", Nucl. Instr. and Meth. Phys. Res. B **147** (1999) 29-34.
24. M. Luysberg, D. Kirch, H, Trinkhaus, B. Hollaender, S. Lenk, S. Mantl, H.J. Herzog, T. Hackbarth, P.F. Fichtner, "Relaxation of SiGe Buffer Layers on Si(100) Through Helium Ion Implantation", *Microscopy in Semiconducting Materials*, Institute of Physics Publishing, Oxford (in press).
25. S.H. Christiansen, P.M. Mooney, J.O. Chu and A. Grill, "Strain Relaxation Mechanisms in He^+-Implanted and Annealed SiGe Layers on Si(001) Substrates", in *Materials Issues in Novel Si-Based Technology,* Mat. Res. Soc. Symp. Proc. **686** (in press).
26. N. Sugiyama, T. Mizuno, S. Takagi, M. Koike, A. Kurobe, "Formation of Strained-Silicon Layer on Thin Relaxed-SiGe/SiO_2/Si Structure Using SIMOX Technology", Thin Solid Films **369** (2002) 199-202.
27. T. Mizuno, S. Takagi, N. Sugiyama, H. Satake, A. Kurobe, A. Toriumi, "Electron and Hole Mobility Enhancement in Strained Si MOSFETs on SiGe on Insulator Substrates Fabricated by SIMOX Technology", IEEE Elect. Device Lett. **21** (2000) 230-2.
28. T. Tezuka, N. Sugiyama, and S. Takagi, "Fabrication of Strained Si on an Ultrathin SiGe-on-Insulator Virtual Substrate with a High-Ge Fraction", Appl. Phys. Lett. **79** (2001) 1798-1800.
29. L.J. Huang, J.O. Chu, D.F. Canaperi, C.P.D'Emic, R.M. Anderson, S.J. Koester and H.-S. P. Wong, "SiGe-on-Insulator Prepared by Wafer Bonding and Layer Transfer for High-Performance Field-Effect Transistors", Appl. Phys. Lett. **78** (2001) 1267-9.
30. Zhi-Yuan Cheng, M.T Currie, C.W. Leitz, G. Taraschi, E.A. Fitzgerald, J.L. Hoyt and D.A. Antoniadas, "Electron Mobility Enhancement in Strained-Si n-MOSFETs Fabricated on SiGe-on-Insulator (SGOI) Substrates", IEEE Electron. Device Lett. **22** (2001) 321-3.
31. J.W. Matthews, "Defects Associated with the Accommodation of Misfit Between Crystals", J. Vac. Sci. Technol. **12** (1975) 126-33.
32. P.M. Mooney, S.J. Koester, J.A. Ott, J.L. Jordan-Sweet, J.O. Chu and K.K. Chan, "Thermal Stability of Strained Si on Relaxed $Si_{1-x}Ge_x$ Buffer Layers", in *Materials Issues in Novel Si-Based Technology,* Mat. Res. Soc. Symp. Proc. **686** (in press).
33. P.M. Mooney, J.L. Jordan-Sweet, G.B. Stephenson, F.K. LeGoues, and J.O. Chu, "High Resolution X-Ray Diffraction Measurements of Strain Relaxed SiGe/Si Structures", Advances in X-Ray Analysis **38** (1995) 181-93.
34. Rocking Curve Analysis by Dynamical Simulation, Bede Scientific, Inc.
35. S.J. Koester, K. Rim, J.O. Chu, P.M. Mooney, and J.A. Chu, "Effect of Thermal Processing on Strain Relaxation and Interdiffusion in Si/SiGe Heterostructures Studied Using Raman Spectroscopy", Appl. Phys. Lett**. 79** (2001) 2148-50.
36. P. Baucaud, L. Wu, C. Guedji, H.F. Julien, I. Sahnes, Y. Campidelli and L. Garchery, "Photoluminescence and Intersubband Absorption Spectroscopy of Interdiffused Si/SiGe Quantum Wells", J. Appl. Phys. **80** (1996) 1414-21.
37. M. Griglione, T.J. Anderson, Y.M. Haddara, M.E. Law, K.S. Jones and A. van den Bogaard, "Diffusion of Ge in $Si_{1-x}Ge_x$/Si Single Quantum Wells in Inert and Oxidizing Ambients", J. Appl. Phys. **88** (2000) 1366-72.