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A SELF-ALIGNED SILICIDE PROCESS UTILIZING ION IMPLANTS FOR REDUCED SILICON CONSUMPTION AND CONTROL OF THE SILICIDE FORMATION TEMPERATURE

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Abstract:

We propose a modified self-aligned silicide (salicide) process that uses Ge implantation and a silicon cap to reduce the silicon substrate consumption by 75% as compared with a conventional salicide process. We have used Ge implants to increase the cobalt disilicide formation temperature. This forces the cobalt to react primarily with a deposited silicon cap, thus minimizing consumption from the silicon substrate. We expect this process to be useful for making silicide on shallow junctions and thin SOI films, where silicon consumption is constrained.

Introduction:

Self-aligned silicide (salicide) is an integral process in the fabrication of high-performance CMOS devices. The salicide process converts the surface portions of the source, drain, and gate silicon regions into a silicide. Due to the low sheet resistance of the silicide film, the series resistance to the intrinsic device is minimized. In bulk devices the silicide film must be contained within the source and drain junction or otherwise it would form a leakage path to the substrate. Moreover, to obtain a good ohmic contact it is desirable to target the silicide/silicon junction to coincide with the peak concentration of the source/drain doping. Scaling the gate length of a MOSFET requires shallow junctions to suppress short channel effects (SCE) [1,2]. The junction depth is expected to become comparable or even thinner than the required silicide film thickness. Meeting the shallow junction requirement and maintaining a thick enough silicide film requires a revision of the conventional salicide process.

Scaling of the silicon-on-insulator (SOI) MOSFET leads to similar constraints on the salicide process. In the case of SOI, reducing the channel thickness (t_{si}) has been found to suppress SCE for both single-gate and double-gate MOSFETs [1]. The use of the conventional salicide process with devices having a very thin SOI channel leads to the following problem: There may not be enough silicon in the source/drain regions to complete the silicide formation. However, even consumption of more than 80% of the silicon film would actually *increase* the series resistance due to a reduction in the contact area [3]. Constraints on the silicon consumption by silicide imposed by future bulk and SOI technologies require altering the conventional salicide process to be compatible with ultra shallow junction technology and ultra thin SOI films.

In a recent publication [4] we discussed a self-aligned silicide (salicide) process that uses a silicon cap to reduce the substrate silicon consumption by 50% as compared with a conventional salicide process. In this paper we propose a modification to the referenced salicide process which uses Ge implants, a cobalt-silicon mixture and a silicon cap to reduce the silicon consumption from the substrate by 75%.

Experiment:

To experimentally determine the effect of Ge implantation on silicide formation, we monitored silicide phase evolution using in-situ synchrotron x-ray diffraction. Figure 1 shows the formation temperature of the $CoSi_2$ phase in $Si_{1-x}Ge_x$ epitaxial layers as a function of the Ge content (x) in the film. The formation temperature increases with the Ge concentration in the film. The higher formation temperature for $Si_{0.8}Ge_{0.2}$ epitaxial layers was also reported in Ref. 5. It is interesting to note that even a film with as low as 3% Ge shows a pronounced increase of over 100 °C in the formation temperature as compared with a pure silicon film (zero percent Ge). Since a low Ge concentration can also be obtained by implanting Ge into silicon, we further tested if the higher formation temperature is obtainable when Ge is incorporated into the silicon film by implantation.

We tested different Ge implant energies having projected ranges of 5.4, 10, 15 and 20 nm. The implant dose was 3E15 cm^{-2}, which roughly corresponds to a Ge content of 6%. The obtained Ge profile and dose were verified by SIMS. Since the implant amorphizes the top portion of the silicon film, we also investigated the role of the amorphization on the silicide formation by testing the silicide process with and without a 900°C RTA re-crystallization anneal. Following the implant and in some samples a re-crystallization anneal, a Co layer capped by a TiN film was deposited on all samples. While annealing the samples at a heating ramp rate of 3°C/s from 100°C to 1000°C, we monitored the silicide formation using x-ray diffraction. The results were compared with a control sample, which was not implanted.

Figure 2 summarizes our results for the different experimental conditions. Each bar shows the range of temperatures for which the CoSi phase exists. The top of the bar indicates the $CoSi_2$ formation temperature. Below the bar Co or Co_2Si exist. The x-axis indicates the Ge implant energy. The samples listed in Fig. 2(a) were *not annealed* by RTA prior to the silicide formation. The non-implanted silicon control sample has a $CoSi_2$ formation temperature of 618°C. The sample that was implanted with Ge at energy of 2 keV (5.4 nm projected range) exhibits a $CoSi_2$ formation temperature of 747 °C, which is 129°C higher than that of the control sample. The higher formation temperature in the Ge-implanted film is similar to that observed in the epitaxial SiGe film. As the Ge implant energy is increased, the formation temperature decreases and even drops below that of the non-implanted sample.

In contrast, all of the samples that were *annealed* prior to silicide formation exhibit a pronounced increase in the formation temperature compared with the non-implanted control, as shown in Fig. 2(b). The sample that was implanted with Ge at energy of 2keV and then annealed exhibits a $CoSi_2$ formation temperature of 739°C. This formation temperature is comparable with the non-annealed sample implanted with energy of 2keV. However, samples implanted with energy of 14keV show a $CoSi_2$ formation temperature of 712°C if annealed, and only 577°C when no anneal is carried out following the Ge implant. This large temperature difference is due to the amorphization of the top portion of the silicon substrate, which is induced by the Ge implant. When the substrate is annealed the superficial amorphous layer re-crystallizes by solid phase epitaxy. The subsequent silicide formation is then carried out in a crystalline SiGe film. These samples show a high formation temperature for all implant conditions. In the case of non-annealed samples, the silicide reaction takes place with an amorphous layer. If the implant energy is low (such as 2keV) the amorphous layer that forms is very thin and is totally consumed when the Co_2Si and CoSi phases form. The $CoSi_2$ reaction occurs within a crystalline SiGe layer. In this case the observed formation temperature is high and is comparable to that of the annealed

sample. If the implant energy is high, the amorphous layer is thicker, and the $CoSi_2$ reaction takes place with amorphous material. The formation temperature in this case is actually lower than that of the non-implanted crystalline silicon control sample.

Some decrease in the formation temperature is seen for annealed samples implanted with higher energy as compared to the sample with the lowest energy implant. Since all samples were implanted with the same dose of the Ge, the lowering of the formation temperature is explained by: (1) Broadening of the implanted Ge profile, which leads to a lower effective concentration of Ge in the sample. (2) Distancing the Ge peak from the surface where the silicide reaction takes place. SIMS analysis (not shown) of the samples confirmed the effective lower concentration and the deeper Ge peak position.

Discussion:

Our main observation is that in Ge-implanted wafers the formation temperature of the $CoSi_2$ phase is over 120°C higher than that of the non-implanted control sample. There is no significant change in the formation temperature of the CoSi phase. We also found that in amorphous silicon the formation of the $CoSi_2$ phase is not retarded. Yet, if the amorphous portion of the film is thin enough so it is consumed by the CoSi phase, then the resulting formation temperature of the $CoSi_2$ phase is similar to those of fully re-crystallized wafers, and is retarded by 129 °C.

Based on our study we propose a new salicide process having reduced silicon consumption. The process is illustrated in Fig. 3, and consists of the following steps: (a) After device gate and spacer formation, implant the junction dopants to form a source and drain. (b) Implant Ge and anneal to re-crystallize amorphized silicon and activate dopants by RTA. (c) Deposit a mixture of Co and Si. (d) Anneal to form Co_2Si and etch the excess metal. (e) Deposit a blanket Si film. (f) Anneal to form the $CoSi_2$ phase. (g) Etch the unreacted portion of the Si cap. The second anneal temperature should be lower than the formation temperature of $CoSi_2$ in the Ge-implanted Si. This limits the silicide reaction to the top silicon cap. When a shallow Ge implant is used (such as the 2 keV implant) there is no need to carry out the re-crystallization anneal. Moreover, the shallow Ge implant can be made after the dopant activation step since it exhibits the same higher $CoSi_2$ formation temperature.

The outlined salicide process enables a 75 % reduction in the silicon consumption as compared with the conventional process. The reduction is achieved due to the following reasons: (1) A silicon cap is applied following the Co_2Si phase formation, thus consumption during the formation of the CoSi phase is reduced by a factor of two due to the supply of silicon from the cap. (2) During the formation of the $CoSi_2$ phase all the silicon is supplied from the cap.

The Co_2Si phase forms within a narrow window of 20°C when pure Co is used. The temperature window opens up to about 100 °C when a mixture of Co and silicon is reacted to form the Co_2Si phase [4]. The wider temperature window makes it easier to form Co_2Si and allows the introduction of the silicon cap earlier in the process. The inclusion of silicon in the Co film also reduces the silicon consumption during the formation of the Co_2Si phase. We note that the amount of silicon incorporated cannot be too high or otherwise bridging from the source and drain to the gate will occur. We found that the addition of 20% Si to Co did not result in bridging and the unreacted portion of the Co-Si mixture was etchable [6].

Conclusions:

The Co silicide formation on Ge-implanted samples and epi-grown SiGe layers was investigated. We found that the $CoSi_2$ formation is retarded to higher temperatures as compared with non-implanted silicon. The retardation is not observed if the silicide reaction takes place with an amorphous film, and the formation temperature in these films is lower than that of pure crystalline silicon. Based on our findings we propose a modified salicide process that uses Ge implants, a cobalt-silicon mixture, and a silicon cap to reduce the silicon consumption from the substrate by 75% as compared with a conventional salicide process

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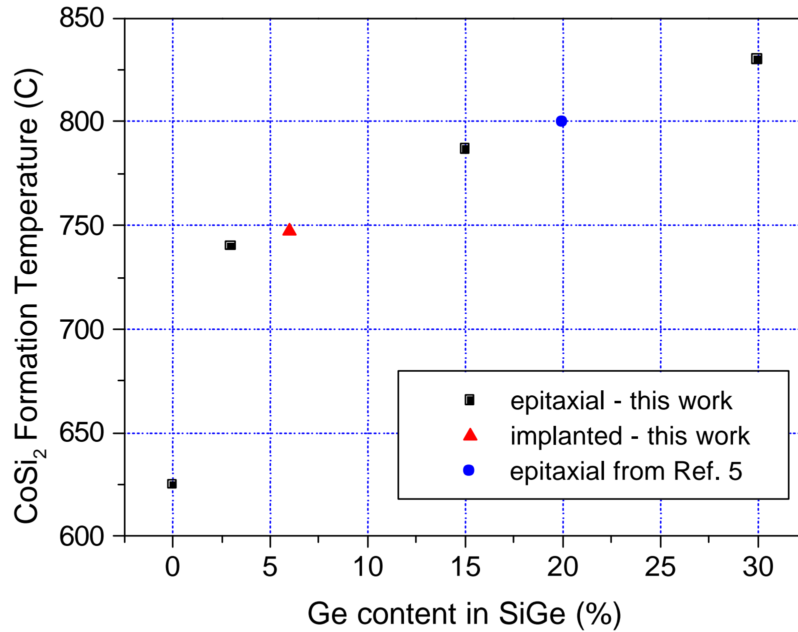

Figure 1: $CoSi_2$ formation temperature in epi-grown $Si_{1-x}Ge_x$ films as a function of the Ge concentration. A silicon wafer implanted with a Ge dose of 3E15 cm^{-2} is also shown.

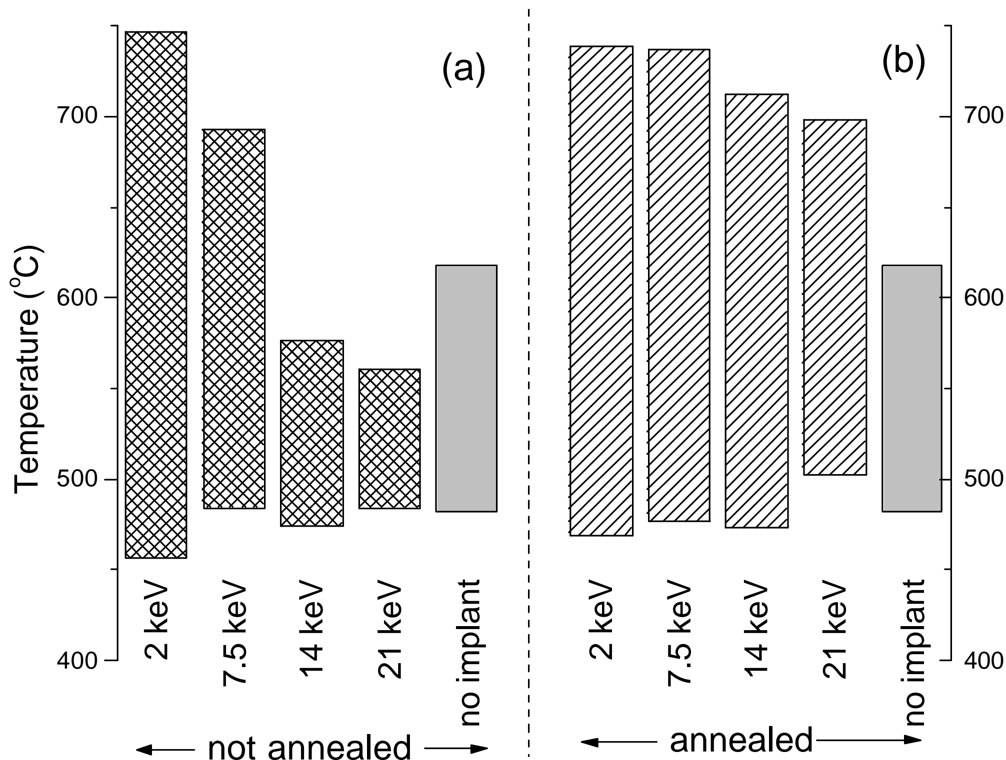

Figure 2: Cobalt silicide formation temperature in silicon implanted with Ge. The bars show the range of temperatures for which the CoSi phase exists. The top of the bar indicates the $CoSi_2$ formation temperature. The implant dose is 3E15 cm^{-2}, and the energies correspond to projected ranges of 5.4, 10, 15 and 20 nm. The samples labeled "annealed" were annealed by RTA at 900°C for 1 second prior to the cobalt deposition.

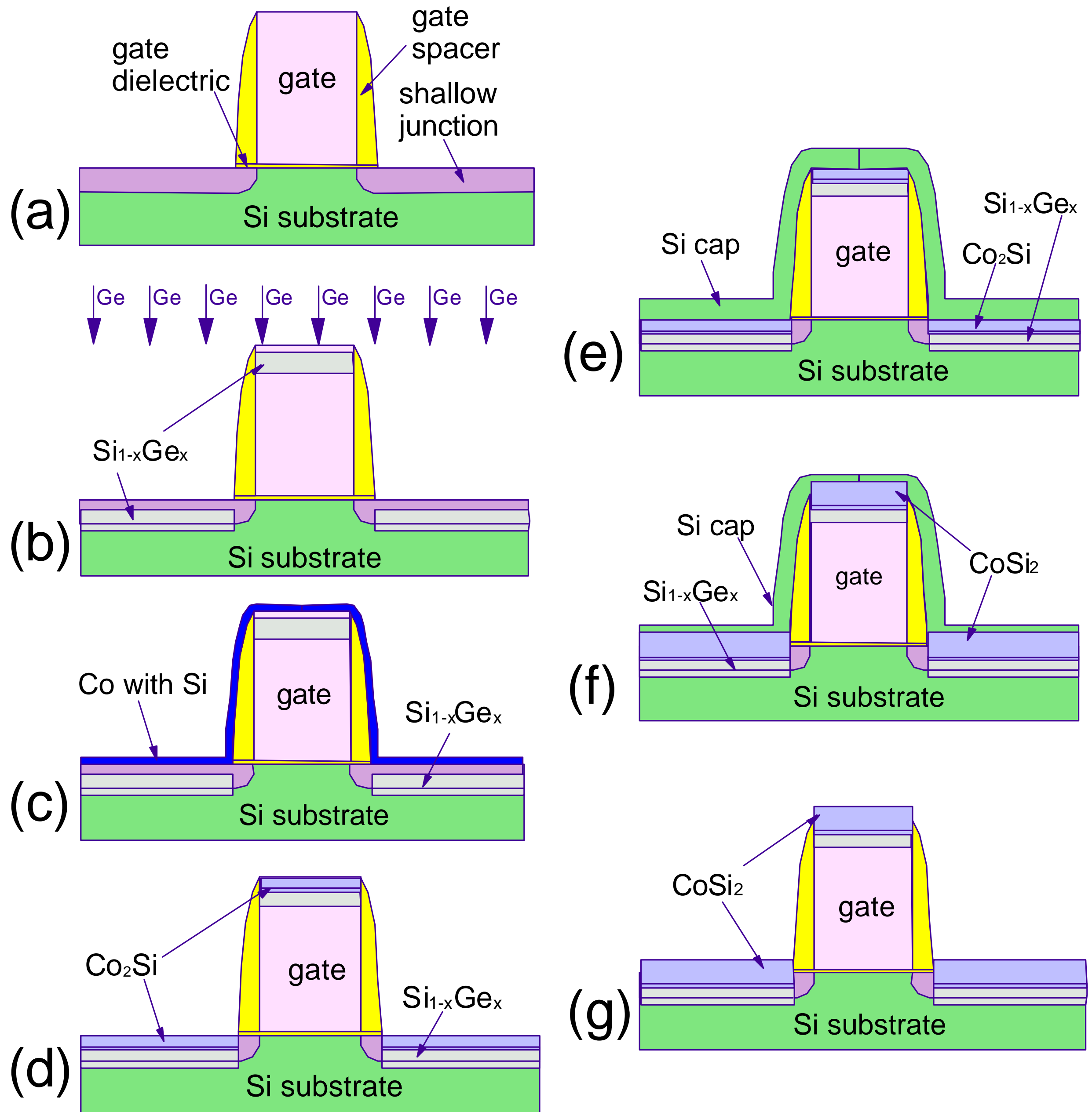

Figure 3: A modified salicide process: (a) After gate and spacer formation implant the junction dopants to form a source and drain. (b) Implant Ge and RTA anneal to re-crystallize amorphized silicon and activate dopants. (c) Deposit a mixture of Co and Si. (d) Anneal to form Co_2Si and etch the excess metal. (e) Deposit a blanket Si film. (f) Anneal to form the $CoSi_2$ phase, and (g) Etch the unreacted portion of the Si cap.