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## Formation of Nanometer-Scale Dot Arrays from Diblock Copolymer Templates

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## Formation of Nanometer-Scale Dot Arrays from Diblock Copolymer Templates

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### ABSTRACT

We have developed four different fabrication processes based on self-organizing diblock copolymers that all produce densely-spaced, uniformly-sized nanometer-scale dot arrays over large wafer areas. We demonstrate the versatility of these techniques through examples of dot arrays formed of metallic, insulating, and polymeric materials. These fabrication processes vary in complexity, utility, and degree of optimization, and we discuss the relative merits of each. The ability to create uniform nanoscale features below lithographic resolution limits may enable key applications in fields such as magnetic recording and microelectronics.

### INTRODUCTION

We have been exploring self-organizing diblock copolymer thin films as general templates for patterning surfaces on length scales below lithographic resolution limits, and specifically for applications in microelectronics. For example, we have previously described our use of these polymer films as masks for reactive ion etching (RIE) in order to produce electrodes with increased surface area [1]. In addition, several other groups have been investigating various versions of surface patterning using diblock copolymers [2,3,4,5,6,7]. Here we describe processes for forming nanometer-scale dot arrays from polymer templates. Such structures may find use in applications such as magnetic media [5] or as quantum dots [2] and will also prove useful as masks for etching pillar structures with sub-lithographic dimensions [8].

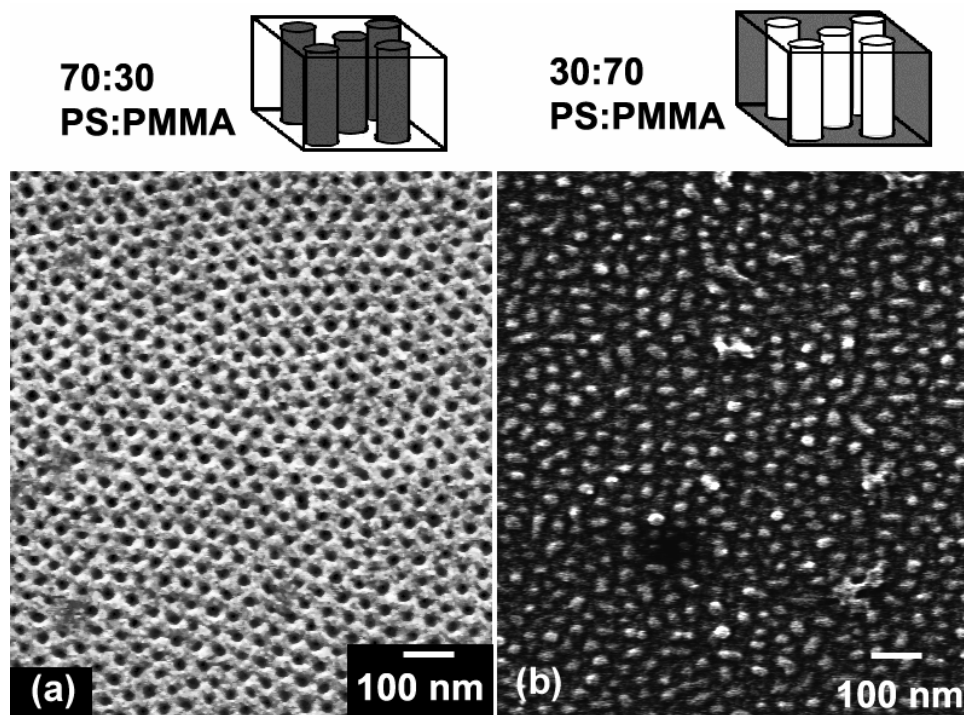
We present four different methods for producing nanometer-scale dot arrays, all of which use diblock copolymer templates as a starting point for fabrication. First we demonstrate a method of producing self-assembled polymeric dots by adjusting the composition of the block copolymer itself. We also describe a process for forming arrays of silicon nitride dots that integrates the polymer template with conventional semiconductor fabrication techniques such as reactive ion etching and chemical vapor deposition. Both of these methods are attractive because they are entirely materials-compatible with silicon processing, and can therefore be used as steps in the fabrication of silicon devices. We have also developed an extremely versatile method for producing nanodot arrays using a liftoff technique. Finally, we describe a curious example of how a nanostructured surface affects the self-assembly of chemically-synthesized nanocrystals.

### POLYMER DOT ARRAYS

Our previous experiments used diblock copolymers composed of polystyrene (PS) and poly(methyl methacrylate) (PMMA), both because the behavior of these two polymers is well understood and because of their materials compatibility with standard semiconductor processing [1,9,10]. We have previously described details of the polymer template formation, and so here we will merely highlight the important features of the self-assembly process. Following a

surface pretreatment with a random copolymer underlayer [11], we spin-cast thin films of asymmetric 70:30 PS:PMMA diblock copolymers onto a substrate [12]. The two polymer blocks spontaneously assemble into hexagonal arrays of cylindrical PMMA domains in a matrix of PS upon heating the substrate to temperatures above 165 °C. After heat treatment, the PMMA is selectively removed from the polymer film using a wet develop in acetic acid. A top-down scanning electron microscope (SEM) image of a completed PS template is shown in Fig. 1a. Formation of cylindrical PMMA domains is ensured by the intrinsic molecular weight ratio of the diblock copolymer (70:30 PS:PMMA), while template dimensions are determined by both the weight ratio and the total molecular weight. For the template shown in Fig. 1a ( $M_n=67$  kg/mol), we measure 20 nm diameter pores ( $\sigma=10\%$ ) with 42 nm interpore separations ( $\sigma < 20\%$ ). The quality of this template is typical of the pore size uniformity we achieve with this diblock copolymer system.

As we have indicated, diblock copolymer film morphology is determined in large part by the molecular weight ratio of the two constituent polymer blocks [13], and this provides an experimental handle with which to alter the properties of the polymer template. Because the diblock copolymer phase diagram is largely symmetric with respect to the two polymer blocks, we can reverse the tone of the polymer template shown in Fig. 1a (and thus produce cylindrical domains of PS in a matrix of PMMA) by selecting the complementary block molecular weight ratio.



**Figure 1.** (a) Top-down SEM image of a 70:30 PS:PMMA diblock copolymer template on silicon. Dark circular regions are areas where the PMMA has been removed. Template pore diameters are 20 nm with center-to-center spacings of 42 nm. (b) Top-down SEM image of 30:70 PS:PMMA diblock copolymer template. Light circular regions are areas of remaining PS. Average PS dot size is 22 nm.

Figure 1b shows the result of spin-casting a thin film of 30:70 PS:PMMA diblock copolymer ( $M_n=71$  kg/mol) [12] onto a silicon substrate and processing the film under similar conditions as used to form the nanoporous template shown in Fig. 1a. After removal of the PMMA block in acetic acid, the template consists of loosely-arranged 22 nm diameter PS dots (Fig. 1b). This template is much less uniform than its complement (Fig. 1a), and the diameter distribution varies widely ( $\sigma\sim 40\%$ ). We have not optimized the processing conditions for formation of a well-ordered PS dot array, however these initial results hint at an effective means of patterning large areas with nanometer-scale polymer dots. The polymer dots may serve as etch masks for transfer of the dot pattern into a more thermally-stable or mechanically-robust underlying material. PS has proved a resistant mask for reactive ion etching (RIE) [9], therefore this system is suitable for forming high-aspect-ratio structures such as nanoscale pillar arrays.

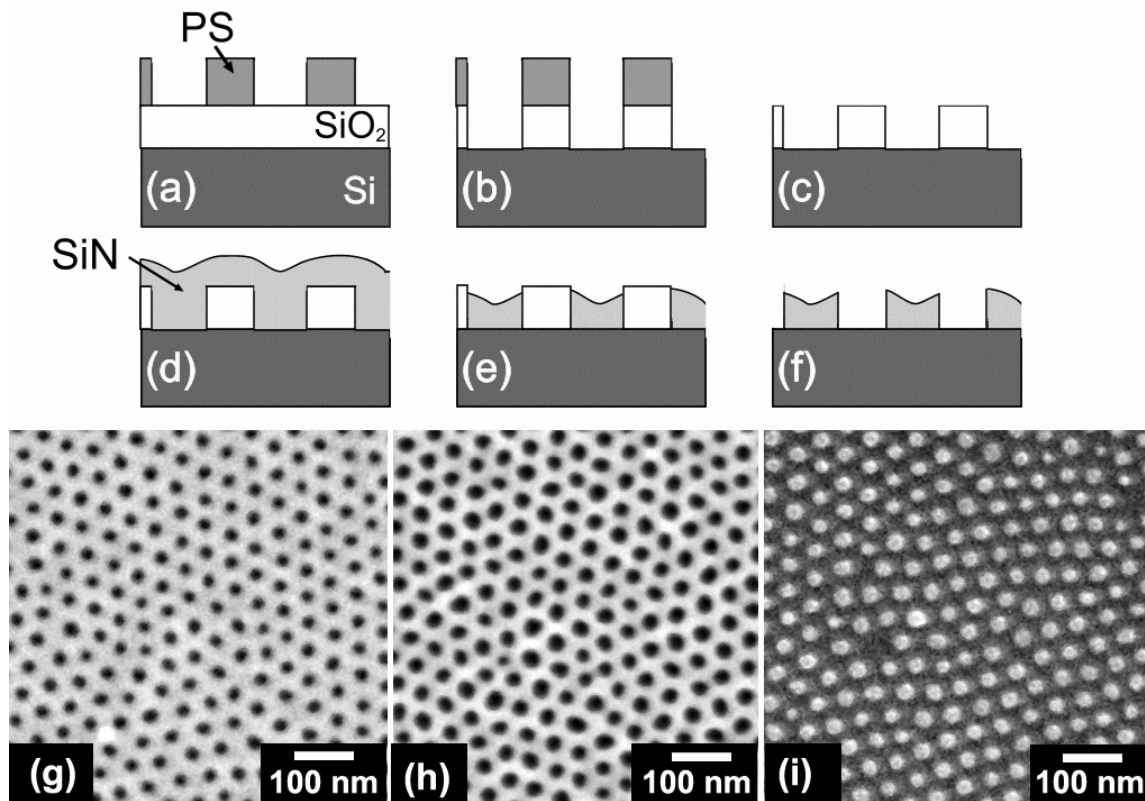
### SILICON NITRIDE DOT ARRAYS USING CHEMICAL VAPOR DEPOSITION

One of our main research interests has been developing methods for integrating diblock copolymer templates into semiconductor processing [1]. Because the polymer materials themselves are inherently compatible with silicon technology, we believe this technique can be used quite generally as a high-resolution patterning step in the fabrication of complicated silicon devices. With this idea in mind, we present here a process for forming dot arrays that integrates the polymer template with several other standard techniques from semiconductor processing. We have developed this process using 8-inch diameter silicon wafers, and all processing steps were performed in a Class 100 semiconductor cleanroom facility.

We begin by forming the diblock copolymer template (70:30 PS:PMMA) on a silicon wafer onto which 20 nm of silicon dioxide has been grown (Fig. 2a). Top-down SEM images (Fig. 2g) show average pore diameters of 20 nm with 10% diameter variations across the full 8-inch wafer. The polymer template pattern is next transferred into the underlying  $\text{SiO}_2$  using RIE (Fig. 2b). After polymer removal by oxygen plasma ashing, the nanostructured template pattern is reproduced in the  $\text{SiO}_2$  layer (Fig. 2c). SEM images of the wafer at this stage show slightly widened pore diameters (23 nm,  $\sigma=9\%$ ) due to the oxide RIE (Fig. 2h).

We next deposit 20 nm of silicon nitride on the wafer surface using rapid thermal chemical vapor deposition. Because of the conformality of this deposition process, the vertical thickness of the silicon nitride in the template holes is larger than that on top of the oxide (shown schematically in Fig. 2d). An anisotropic RIE process can remove the silicon nitride from the wafer surface until the oxide template is exposed, leaving silicon nitride in the pore bottoms (Fig. 2e). Finally, the  $\text{SiO}_2$  template is stripped with dilute hydrofluoric acid (Fig. 2f). The remaining silicon nitride dot array has dimensions and uniformity similar to those of the starting polymer template (22 nm diameters with  $\sigma=9\%$  and interpore spacing 42 nm) (Fig. 2i). These dimensions correspond to a dot density of approximately  $6.5 \times 10^{10}$  dots/cm<sup>2</sup>.

This process is fully compatible with standard semiconductor processing, opening up opportunities for integration of the self-assembly process into silicon device fabrication. The nitride dots can serve as robust etch masks for forming nanoscale silicon pillar arrays, where the pillar dimensions are below photolithographic resolution. Because of the continued shrinking of conventional silicon device dimensions, there is a strong need to improve our understanding of the physics of electron devices at these nanometer length scales. This technique provides an important tool for nanofabrication of devices at these dimensions.

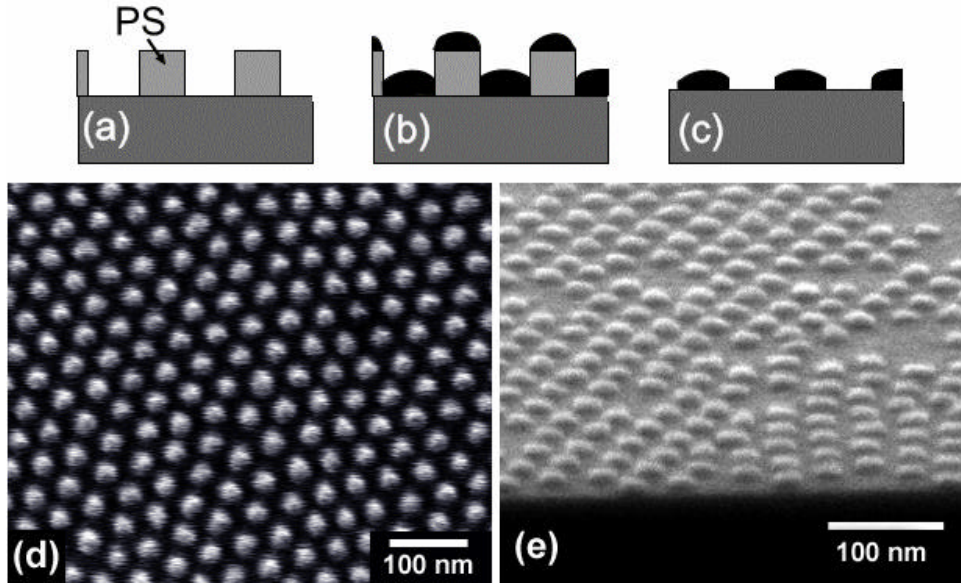


**Figure 2.** (a-f) Schematic of dot array formation process. (a) PS template formed on thermally-oxidized silicon substrate. (b) Pattern transfer to the oxide layer by RIE. (c) Removal of PS. (d) Conformal deposition of silicon nitride. (e) Anisotropic silicon nitride etch exposes SiO<sub>2</sub> layer. (f) SiO<sub>2</sub> removal with hydrofluoric acid. (g) Top-down SEM image of polymer template. (h) Top-down SEM image of etched SiO<sub>2</sub> surface (after PS removal). (i) Top-down SEM image of resulting silicon nitride dot array.

## DOT ARRAYS USING PHYSICAL VAPOR DEPOSITION

We have also developed a general method for producing uniform dot arrays by transferring the pattern of the optimized PS template shown in Fig. 1a into a variety of non-polymeric materials using a liftoff technique. This technique is extremely versatile, and we have successfully demonstrated dots formed of Au, Ti, Co, AuPd, and quartz. In principle we can form nanometer-scale dot arrays of any material that can be directionally deposited on virtually any substrate material. Other groups have been exploring similar methods of producing arrays of close-packed nanoparticles using block copolymer templates of both spherical [14,5] and cylindrical [3] phase morphologies, but this liftoff technique is perhaps the simplest and most general.

We begin by forming a nanoporous polymer template by assembling a thin film of the 70:30 PS:PMMA and then removing the PMMA from the cylindrical pores (Fig. 3a). (A typical template of this type is shown in Fig. 1a). A brief oxygen RIE is used to clean out the pore bottoms and promote metal adhesion to the substrate. We then electron-beam evaporate a thin



**Figure 3.** (a-c) Schematic of liftoff process that results in uniform dot arrays. (a) Beginning PS template. (b) Metal deposition by electron-beam evaporation. (c) PS removal. (d) Top-down SEM image of a 2 nm Ti/6 nm Co dot array. (e) 70 degree angle SEM image of 2 nm Ti/6 nm Au dot array.

film of the desired dot material over the wafer surface (Fig. 3b). Next we “lift off” the evaporated material that deposited on top of the polymer template by dissolving the PS in 1-methyl-2-pyrrolidone (NMP) heated to 120 °C under ultrasonic agitation. The final structure (Fig. 3c) consists of a hexagonal close-packed dot array with dimensions similar to the beginning PS template.

Top-view SEM images of a completed dot array confirm that the template pattern has been faithfully reproduced (Fig. 3d). We measure mean metal dot diameters of 21 nm ( $\sigma = 15\%$ ) and interdot spacings of 42 nm, which closely match the dimensions of the original template. Because of the limitations imposed by the height of the polymer template, [15] we are limited to dot thicknesses on the order of 10 nm using this technique. Angled SEM images of metal dot arrays show their pancake-like shape (Fig. 3e).

We envision several useful technological applications of this versatile fabrication technique. For example, dense arrays of physically patterned nanometer-scale magnetic domains are one possibility for future magnetic recording media [16]. If each metal dot in Fig. 3d corresponded to a single magnetic bit, the recording density of such a media would be  $\sim 400$  Gbit/in<sup>2</sup>. As a second example, the size uniformity of the dots produced by our technique may provide an avenue for improving the performance of quantum-dot memory devices [17], whose voltage threshold variations are determined in large part by dot size distributions.

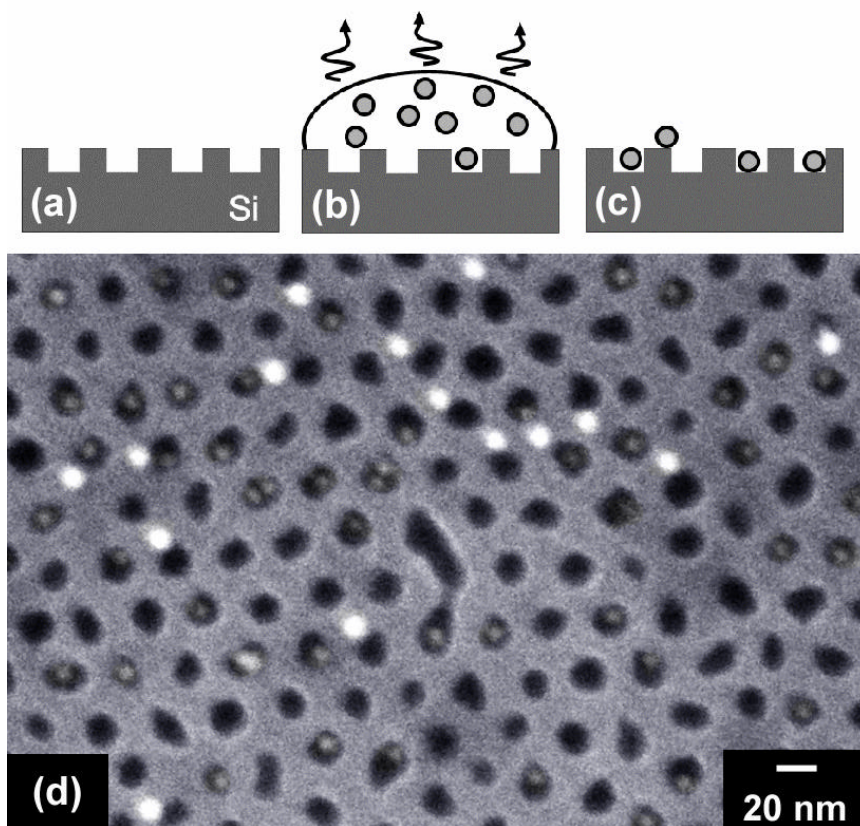
## SEPARATION OF CHEMICALLY-SYNTHESIZED NANOCRYSTALS

Surfaces that are structured on a nanometer length scale can influence the assembly of solution-deposited chemically-synthesized nanocrystals. Here we demonstrate the effect of

nanometer-scale silicon topography on the assembly of metallic nanocrystals, where the surface features are defined by block copolymer self assembly. Other interesting experiments have shown that chemical differences from the diblock copolymer template can also influence metal coatings of surfaces [6,18].

We use a diblock copolymer template as a RIE etch mask to roughen a silicon surface (Fig. 4a). The etch conditions for this experiment are similar to those which we have previously described [1]. After template removal, the silicon surface is covered with shallow pits (10-12 nm depths) of similar lateral dimensions as the polymer mask (20 nm diameter, 42 nm pitch). Next we place a drop of hexane containing a dilute solution of chemically-synthesized cobalt nanocrystals onto the nanostructured surface (nanocrystal diameters were 10 nm) [19], and allow the solvent to evaporate (Fig. 4b) before cleaning residue with methanol (Fig. 4c). We then image the surface with an SEM to observe the nanocrystal positions. Although we have not performed a systematic study of the uniformity of the nanocrystal deposition, Fig. 4d illustrates a reasonably typical sample region.

Figure 4d demonstrates that the nanocrystals move to regions of high surface interaction, as they tend to settle into the pits of the silicon surface. Of the 66 nanocrystals in this image, 51 are settled into a pit (78%). Furthermore, because the size of the etched pits is roughly matched to



**Figure 4.** (a-c) Schematic of nanocrystal separation process. (a) Beginning etched silicon substrate. (b) Nanocrystals deposited on substrate by evaporation of carrier solvent. (c) Resulting substrate with deposited nanocrystals. (d) Top-down SEM image of nanocrystals residing in etched pits on silicon substrate.

the size of a single nanocrystal, the nanocrystals tend to fill pits one at a time, similar to eggs in an egg carton. In this figure, there are only 3 instances of 2 nanocrystals per pit, and 45 cases of a single nanocrystal occupying a hole. While mostly a curiosity, this technique may have some application in depositing uniformly-dilute nanocrystal films on a surface.

## CONCLUSIONS

We have described four different techniques for producing wafer-scale areas of high-density dot arrays with dimensions below lithographic resolution limits. Each of these methods relies on the nanometer size scale and uniformity inherent in self-assembled diblock copolymer thin films. By tailoring the composition of the diblock copolymer material, it is possible to form arrays of polymeric dots. Fabrication of inorganic dot arrays is accomplished by combining diblock copolymer templates with either silicon nitride chemical vapor deposition and anisotropic RIE or electron-beam evaporation and liftoff. The former process has been fully integrated with semiconductor processing in order to facilitate fabrication of more complicated silicon structures, while the latter technique may prove useful in the construction of patterned magnetic recording media or quantum-dot electronic devices. We have also illustrated the effect of a nanostructured surface on the assembly of solution-deposited metallic nanocrystals. We are presently working toward integrating these high-resolution self-assembly processes with more conventional fabrication techniques in order to produce more complicated nanometer-scale devices.

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