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Batch-Fabricated Spin-Injection Magnetic Switches

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Abstract

A method is developed for the fabrication of sub-100nm current-perpendicular spin-valve junctions with low contact resistance. The approach is to use a batch-fabricated trilayer template with the junction features defined by a metal stencil layer and an undercut in the insulator. The spin-valve thin film stack is deposited afterwards into the stencil, with the insulator undercut providing the necessary magnetic isolation. Using this approach, reproducible spin-current-induced magnetic switching is demonstrated for junctions down to 50nm $\times$ 100nm in size.

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Recent development in spin angular momentum transfer devices [1–8] has opened an active new area for the exploration of magnetic nanostructures. Since the phenomenon is only quantifiable for devices with dimensions around 100nm or less, methods are sought for to produce such structures reliably and with fast turn-around time so as to facilitate materials optimization. The common approaches to fabricating such devices involve mostly a subtractive process (e.g., see ref. [7]), where the thin film stack is deposited first, and e-beam lithography is then used to define a mask on top of the film for subsequent etching of the necessary device structure. This approach produces the most ideal device structure in principle, yet it is often too slow for quick materials screening and physics exploration.

An alternative is the additive method, where the critical dimension is first formed on a substrate using e-beam lithography. Subsequent thin film deposition is made onto the substrate with the mask structure already defined. This is common for lift-off lithography. A slightly different version has recently also been used with an embedded polymer insulator layer for the fabrication of current-perpendicular (CPP) magnetic junctions in spin-injection experiments [8]. The problem of their approach is the lack of control over the edges of the device due to complex edge growth dynamics and the lack of deep undercuts of the stencil. The use of a polymer stencil also limits the process parameters such as thin film growth temperature.

Here we introduce a modified approach to the additive patterning of CPP magnetic structures. A metal hard-mask is used as stencil. An inorganic insulator, such as SiO_2, is used with a controllable amount of undercut to provide the necessary isolation and edge definition for the deposited junction stack.

The process begins with a metal-insulator-metal trilayer (the template film, or the template in short). Fig.1 describes the fabrication process. First a Pt-SiO_2-Pt trilayer was deposited as shown in Fig.1(a). The top Pt layer, about 20nm thick, is then patterned using e-beam lithography, and etched using ion milling to open the hole of critical dimension (around 50 to 100nm). The SiO_2 is further opened up with wet etching, allowing the formation of an undercut, whose amount one can control by controlling the etch condition.

The template structure has an inert bottom electrode surface, with critical device dimension defined and ready for additive deposition. Next the metal multilayers needed for CPP transport are deposited. The critical stack sequence, usually very thin, on the order of tens of nanometers, is deposited first. The hole is then filled with a thick layer of contact metal, such as copper. As the very last step, the surface of the whole film is coated with an inert metal, such as platinum or gold, for subsequent lithographic processing.

The sample then goes through a regular optical lithography process to further define an insulator for isolating the top and bottom electrodes, and for the deposition and patterning of the electrodes. This process has the advantage that all critical dimensions are defined on a template substrate before the active film stack is deposited, separating the critical lithography step from the rest of deposition and fabrication, allowing for large quantities of wafer templates to be prepared first using e-beam (which is often the limiting step in turn-around), thus achieving much shorter processing time from thin film layer deposition to final device testing.

Fig.2(a) shows a cross section scanning electron micrograph of a template structure with an undercut. Fig.2(b) and (c) show a cross section view of a film stack deposited into the template with e-beam evaporation (b) and sputtering (c). This particular stack is not thick enough to make good electrical contact. It illustrates the formation of a thin film junction pillar inside the hole with good shape definition. As expected, e-beam evaporated films show better edge definition than sputtered films. However, sputtered films are apparently good enough to yield interesting junction results, as used in this study. For transport study a sample stack of 15Cu-3Co-10Cu-12Co-200Cu-10Pt was sputter deposited onto a patterned stencil with the layered structure of Si-500SiO_2-100Cu-30Pt-50SiO_2-20Pt-Surface. Numbers are film thicknesses in nm.

Current-induced magnetic switching is observed in these junctions. Fig.3 gives an example for a junction with a nominal dimension of 0.05×0.10 μm^2 with easy-axis field. Here unless otherwise specified, junction resistance always refers to the dynamic resistance dV/dI measured using an ac lock-in technique.

The current switching threshold depends on applied field, as shown in the inset of Fig.3(b). Similar switching behavior is obtained at reduced temperatures. For the same junction, a $dI_c^-/dH \approx 9.7 \times 10^{-7}$ A/Oe and a $dI_c^+/dH \approx 6.3 \times 10^{-6}$ A/Oe were observed at 13.4K.

In addition to the current induced switching, Resonance-like features were observed in the junction's resistance *vs.* bias current data for certain values of applied field. Fig.4(a) is one such "resonance peak" for the same 0.05×0.10 μm^2 junction, whose dependence on applied magnetic field is shown in Fig.4(b). The presence of extended magnetic films above the nanostructured pillar may contribute to these resonance structures which is related to magnon excitation [1,6,9,10].

The junction resistance vs. junction area for samples thus prepared show proper scaling. An example is shown in Fig.5(a), where the junction resistance-area product (or RA in short) shows little dependence on junction size, except at the very small junction area end, showing perhaps a reduction of junction yields. Fig.5(b) shows junction magnetoresistance (MR) as a function of RA. The data are seen to cluster around a 2.5% MR and about 0.018 $\Omega\mu m^2$, as expected from a clean CPP structure without parasitic shunting from the circumference of the junction. These data confirm the quality of junction produced in terms of their electrical integrity.

In summary, an alternative approach is demonstrated for batch-processable fabrication of sub-100nm CPP spin-valve structures. The resulting junctions have low contact resistance, well below the junction resistance which is on the order of $1.6 \times 10^{-10} \Omega \mathrm{cm}^2$. They show adequate amount of magnetoresistance (about 2 to 3% typical for the Co-Cu-Co system demonstrated), and current-induced magnetic switching.

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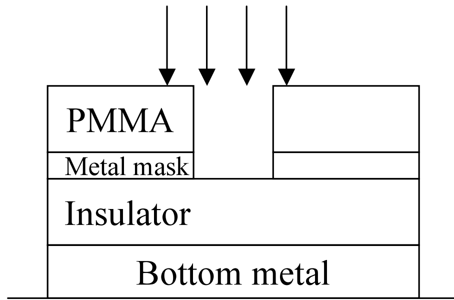
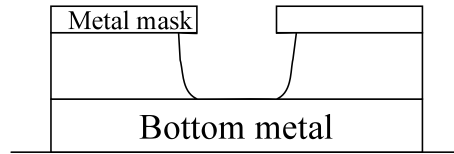
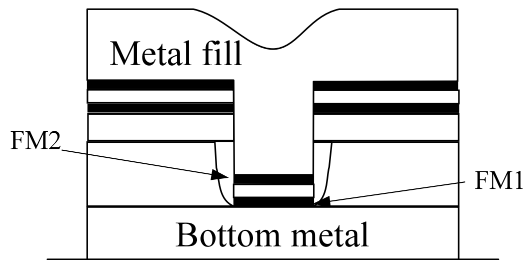
(a) Ion mill to open metal mask



(b) Wet etch to open insulator with undercut



(c) Deposit multilayer films



(d) Form top level contact

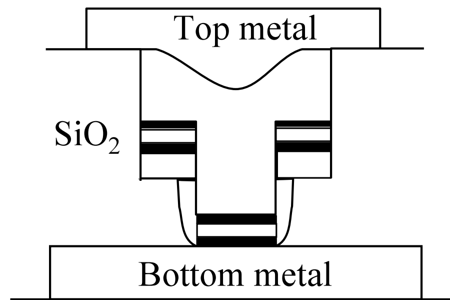


FIG. 1. An illustration of the junction fabrication process-flow. (a)A Pt mask made by a typical PMMA e-beam lithography and ion milling process. (b) Wet-etch is used to open the insulator and to create an undercut in the insulator beneath the metal mask. (c)Deposition of magnetic layers into the batch-fabricated stencil, followed by a thick metal fill to create *in situ* top contact. The undercut decouples the magnetic stack in the pillar. (d)Optical lithography for wiring.

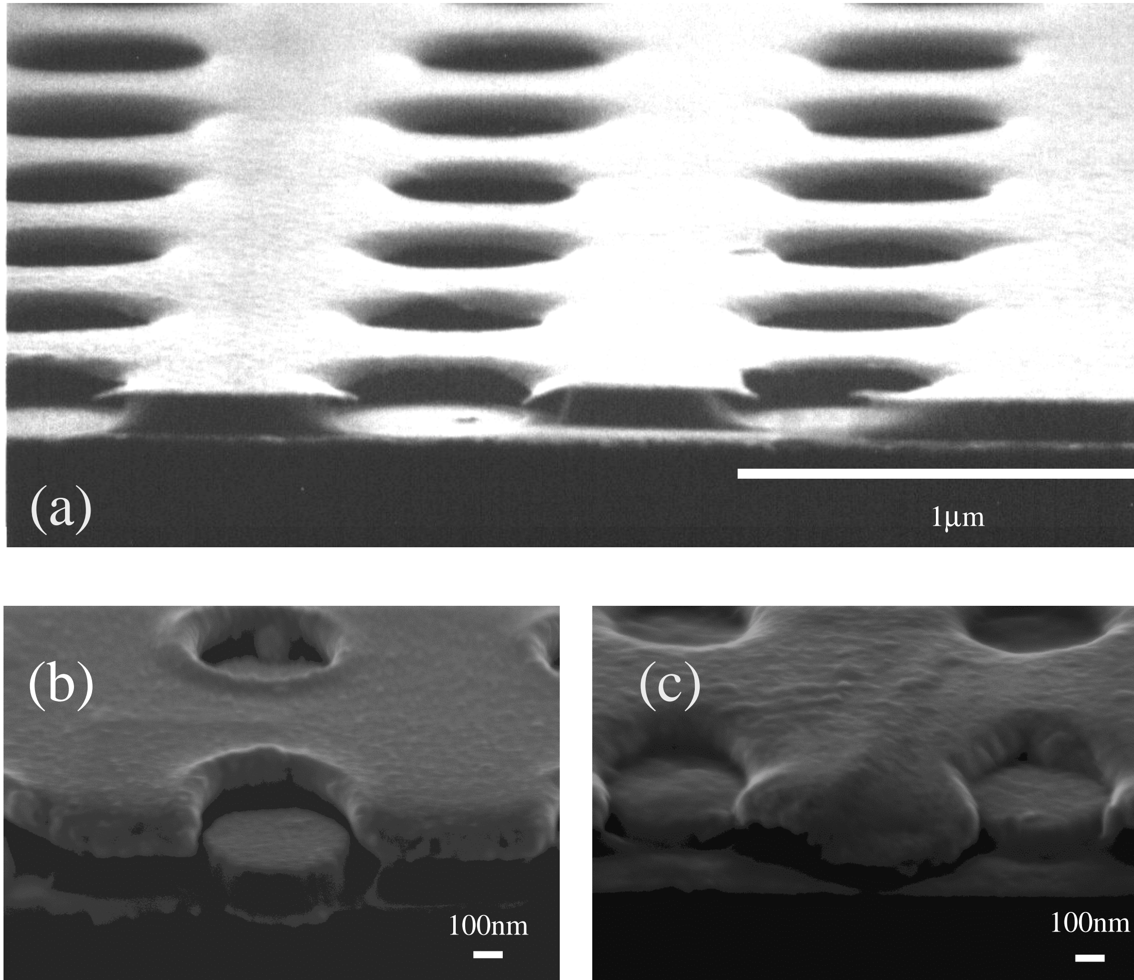


FIG. 2. Cross-section scanning electron micrograph (SEM) views of the batch fabricated magnetic junctions. (a) The batch fabricated template. The Pt stencil definition, and the SiO_2 undercut is shown. (b)The same stencil after electron beam evaporation deposition of a film stack 100Co-10Cu-3Co. Numbers are layer thicknesses in nm. This particular stack is not thick enough to bridge the stencil's top and bottom layers. (c)The same layer sequence, deposited using magnetron sputtering. As expected, the edge profile of evaporation-grown pillars is better than those sputter-grown.

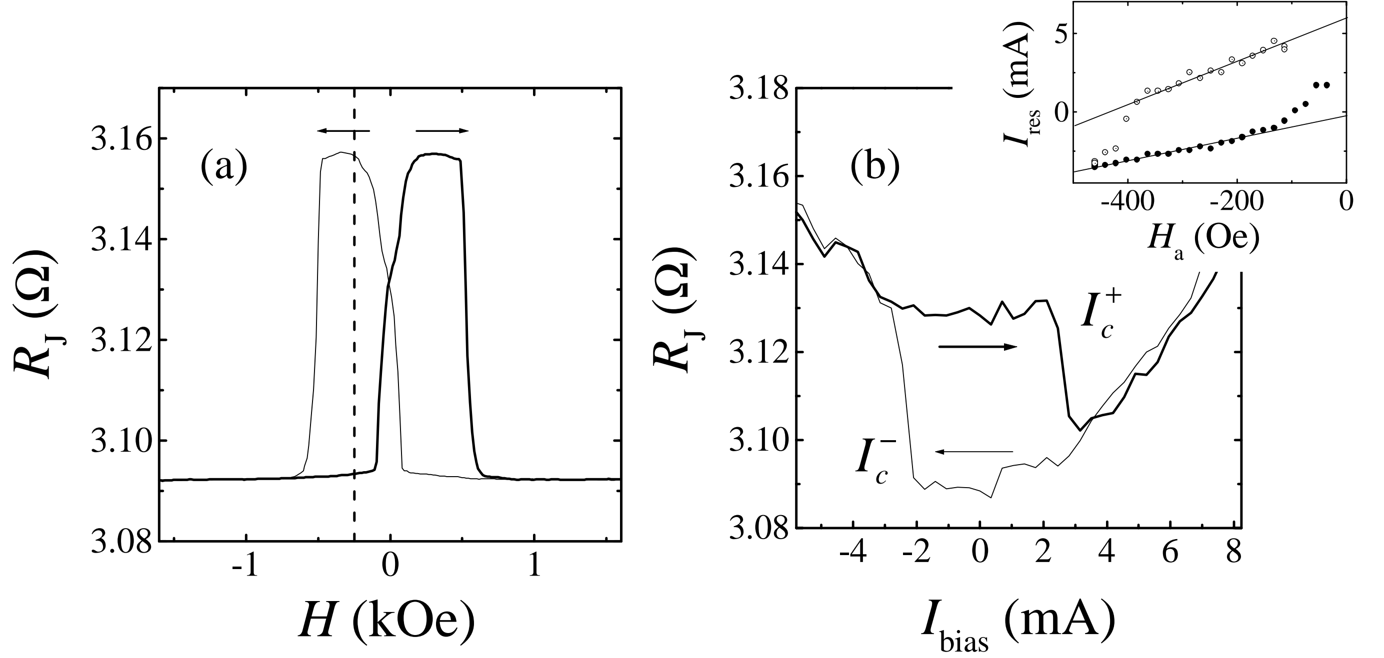


FIG. 3. MR and spin-induced switching of a junction 0.05 × 0.10 μm^2 in size. (a) Junction resistance vs. easy-axis field sweep. (b) Junction resistance *vs.* dc bias current at a bias field of -248 Oe (field position indicated by the vertical dashed line in (a)). A clear current-driven switch between the resistive-high and -low state is observed. Inset: the two switching current observed in (b) as a function of bias field. The slope and intercept for I^{+}_{c}(H) are 1.38×10^{-5}A/Oe and 5.98mA; while those for I^{-}_{c}(H) are 7.11 × 10^{-6}A/Oe and -0.25mA, respectively. Here I^{+}_{c} represents the up-sweep switching current, corresponding to an anti-parallel to parallel (AP to P) transition. I^{-}_{c} represents the down-sweep switching current, corresponding to P to AP transition. Data taken at room temperature.

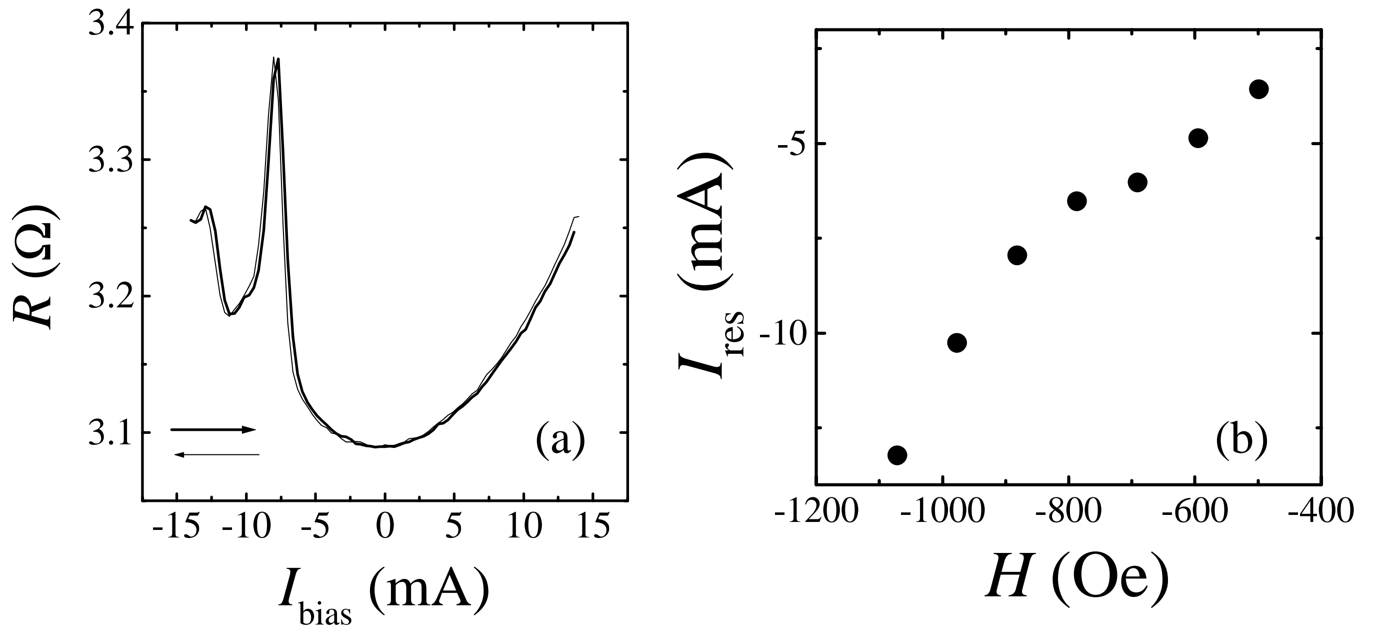
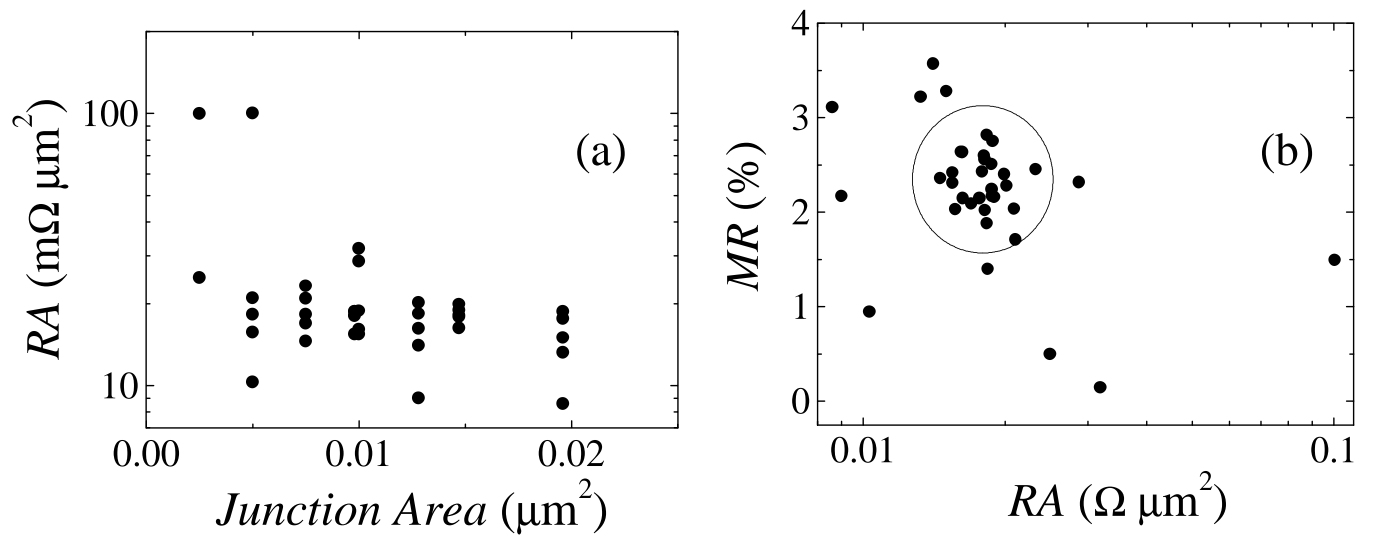


FIG. 4. The resonance behavior of a 0.05×0.10 μm^2 junction. (a) the *R vs.* bias current plot at a bias field of -880 Oe showing the resonant peak in *R* around a current of I_{res} l -10mA. (b) I_{res} dependence on the value of applied field *H.*



J. Z. Sun *et al.*, Fig.5

FIG. 5. Scaling of junction resistance *vs.* area. (a): Junction resistance-area product *RA* shows area-independence except for the smallest devices ($50\times50nm^2$). (b): Junction magnetoresistance *MR vs. RA* plot, showing the clustering of data around $RA \approx 0.02\Omega\mu m^2$. Both indicate the junctions are free from parasitic electrical shorting around the circumference.