RC22459 (W0205-180) May 23, 2002
Electrical Engineering

IBM Research Report

Investigations of UHV/CVD Deposition of SiGe Alloys on Silicon-on-Sapphire Substrates for Application to Device Fabrication Technology Quarterly Report: February-April, 2002

P. M. Mooney, D. V. Singh, J. O. Chu, J. A. Ott, V. Patel, S. J. Koester, A. Grill
IBM Research Division
Thomas J. Watson Research Center
P.O. Box 218
Yorktown Heights, NY 10598

Research Division
Almaden - Austin - Beijing - Haifa - India - T. J. Watson - Tokyo - Zurich

Quarterly Report: February – April, 2002

Space and Naval Warfare Systems Center, San Diego

RDT&E Division
for the 1999 Contract N66001-99-C-6000

Investigations of UHV/CVD Deposition of SiGe Alloys on Silicon-on-Sapphire Substrates for Application to Device Fabrication Technology

P.M. Mooney, D.V. Singh, J.O. Chu, J.A. Ott, V. Patel, S.J. Koester, and A. Grill
IBM T.J. Watson Research Center
PO Box 218, Yorktown Heights, NY 10598

May 13, 2002

Program Review Meeting

A program review meeting with Isaac Lagnado of the Space and Warfare Systems Center, San Diego, was held at IBM on May 8, 2002. Presentations included a materials update (Pat Mooney) and a progress report on divider circuit fabrication run (Dinkar Singh).

Materials Update

Five bonded silicon-on-sapphire wafers were received from the University of Wisconsin (UW) in April 2002. Optical inspection showed that these wafers look very good, with a low density of tiny round defects and with none of the line or corner defects seen in the previous two wafers (see quarterly report of February 2002). The first bonded SiGe-on-sapphire wafer was received in March 2002. There are a number of large voids at the bonded interface, but the bond was strong enough to survive lapping to remove most of the silicon substrate from the original SiGe wafer. UW will send additional SiGe-on-sapphire wafers soon.

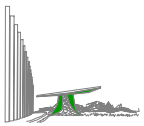
Divider Circuit Fabrication Run

A second pMODFET on bulk Si circuit fabrication run has been completed through the first metal deposition (metal 1). The fabrication process developed to increase the yield of the T-gates is working well, as is the new metal lift-off process. Individual devices were tested and were found to have f_t = 27 GHz, consistent with the lower hole mobility in these wafers compared to the wafers used in previous work (S.J. Koester, et al., IEEE Electron Device Letters 22, 92 (2001)). The device yield was 100% of those tested (45 devices) with a mean threshold voltage of 0.182 V and standard deviation of 25 mV. Although the divider circuit was designed for devices having a threshold voltage of 0.4 V, we are optimistic that these new devices are sufficiently on at zero bias and there is sufficient yield for the divider circuit to work. We expect that the circuit fabrication run will be completed by the end of June. The presentation slides from the program review meeting are attached to this report.

Strained SiGe *p*-MODFET circuits

D. V. Singh, P. M. Mooney, S. J. Koester, J. O. Chu, J. Ott,
V. V Patel, and A. Grill

IBM T. J. Watson Research Center



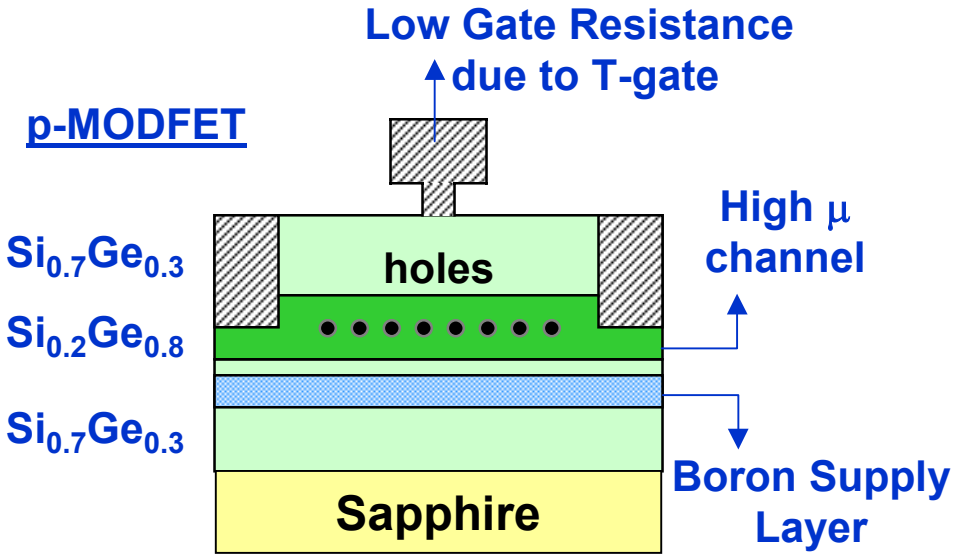
May 8, 2002

IBM

Overview

- Motivation
- Program challenges
- Epitaxial layer structure issues
- Process yield issues & innovations
- Run GOV61: DC measurements
- Run GOV66,67: DC, AC measurements
- SPICE model extraction
- SPICE simulations of the divider circuit
- Summary

Motivation

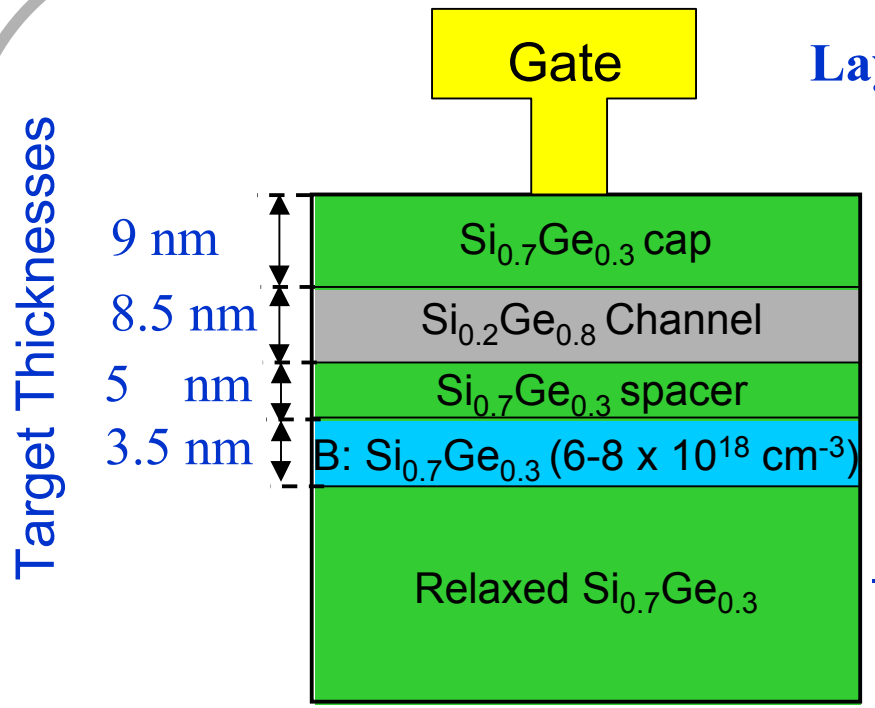


- **High channel mobility ⇒ high transconductance, g_m**
  - Low bias voltages possible, low operating power
  - High frequency, low noise
  - Improved low T performance
- **Sapphire is an excellent substrate for microwave applications**
  - low dielectric loss tangent, good thermal conductor
  - reduced device parasitics and improved passive performance
  - Commercially available substrates
  - Integration issues have posed a significant challenge

Program Challenges

- **Epitaxial growth of p-MODFET layer structure**
- **Device yield during processing:**
  - Divider circuits have approximately 50 transistors
  - 98.6 % device yield required for 50 % yield on circuits
- **Statistical variation of device parameters**
  - e.g. Threshold voltage variation
- **Relaxed SiGe on Sapphire substrates**
  - thin relaxed SiGe on Sapphire required to maximize the benefits of sapphire

Epitaxial layer structure



Layer structure key to high performance

- Maximize carriers in the high mobility channel

- Minimize parallel conduction in the low mobility doped layer

- High Ge content in the strained channel for improved confinement and mobility enhancement

- Minimize the contribution of parasitic capacitances by bringing the channel close to the gate

Above layer structure has in the past yielded excellent devices

μ = 910 cm^2/Vs, n_s ~ 3.5x10^{12} cm^{-2}, f_t ~ 50 Ghz*

* S. J. Koester et al., *IEEE Electron Device Letters*, **22** (2), 92, 2001

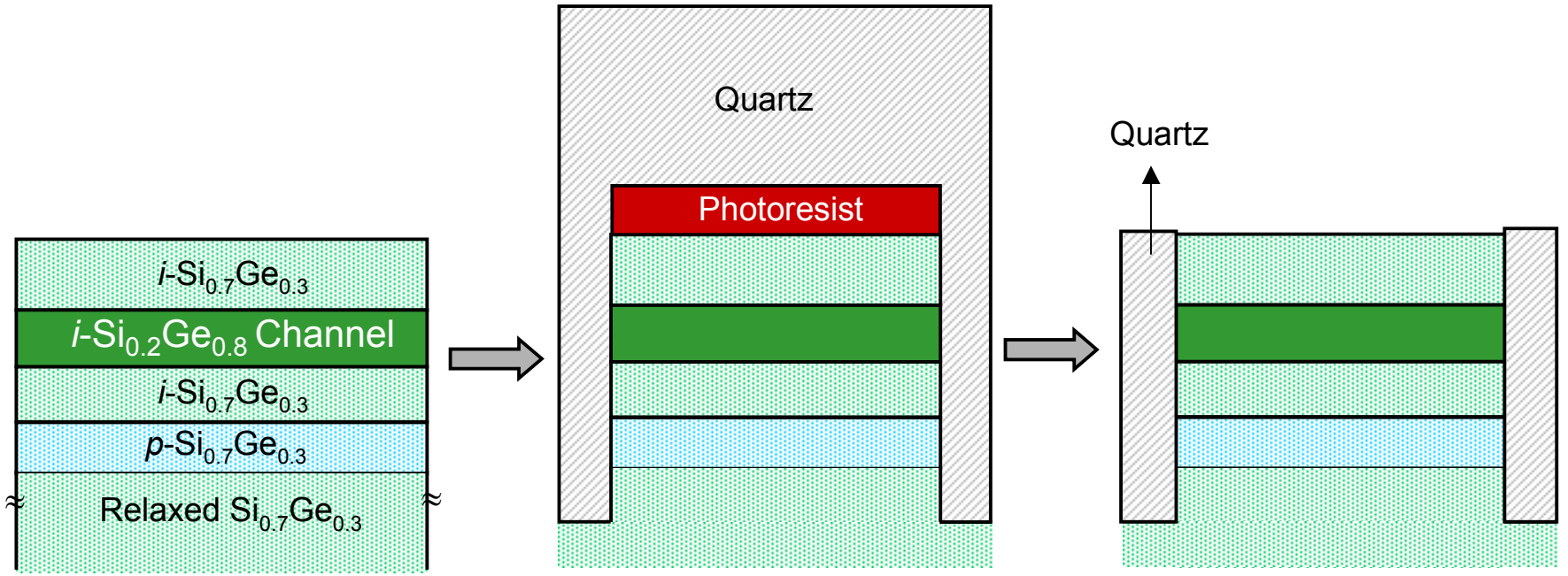
Overview of *p*-MODFET process

MESA FORMATION AND PLANARIZATION

1. Epitaxial Layer Structure grown by UHV-CVD

2. Mesa Isolation:

3. Planarization

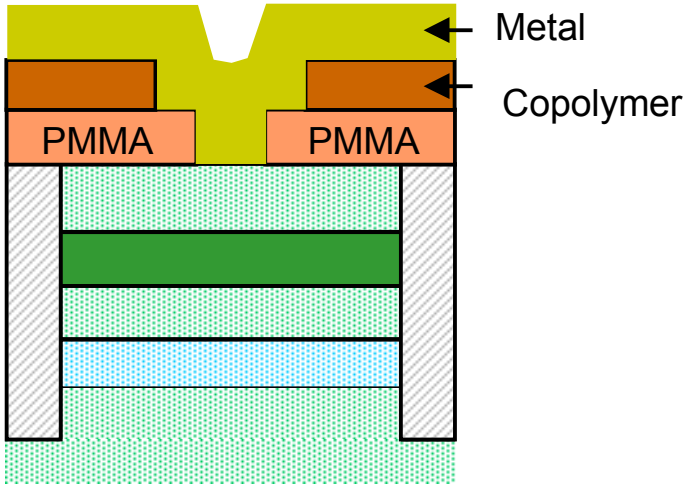


Photolithography
↓
Mesa etch:CF_4 RIE (90nm)
↓
Sputter Quartz (140nm)

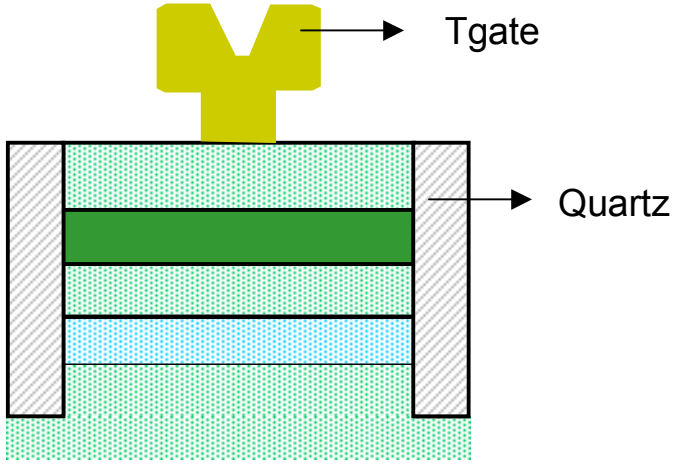
Lift-off process
(clears quartz over the mesas)

T-gate formation

4. T-Gate: Ebeam lithography/ Metal deposition

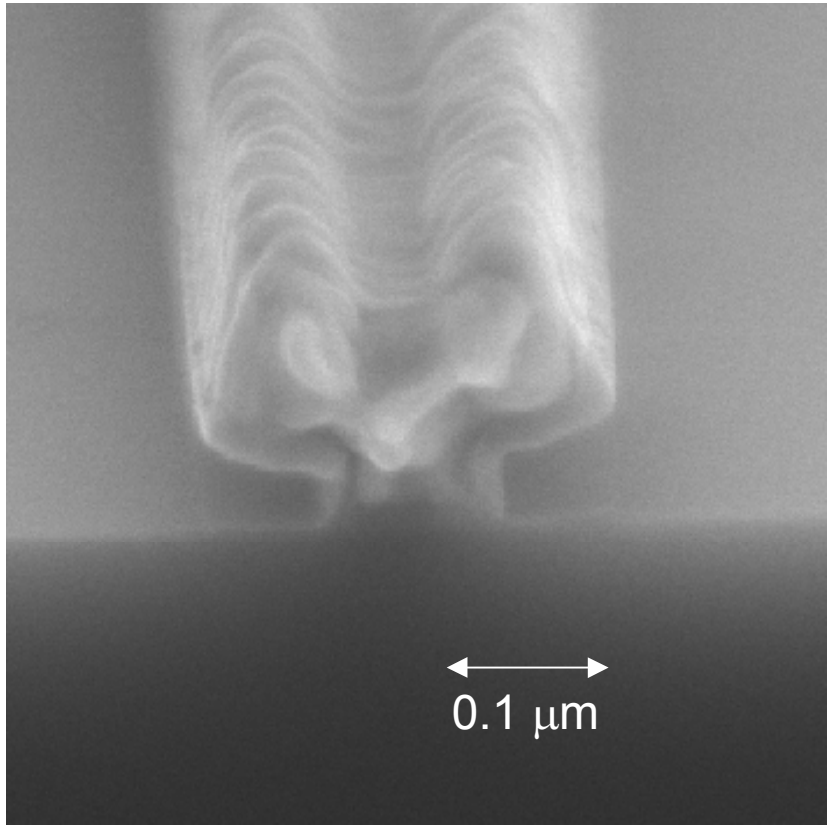


5. T-Gate: Lift off



Lift off to form T-gate

T-Gate formation



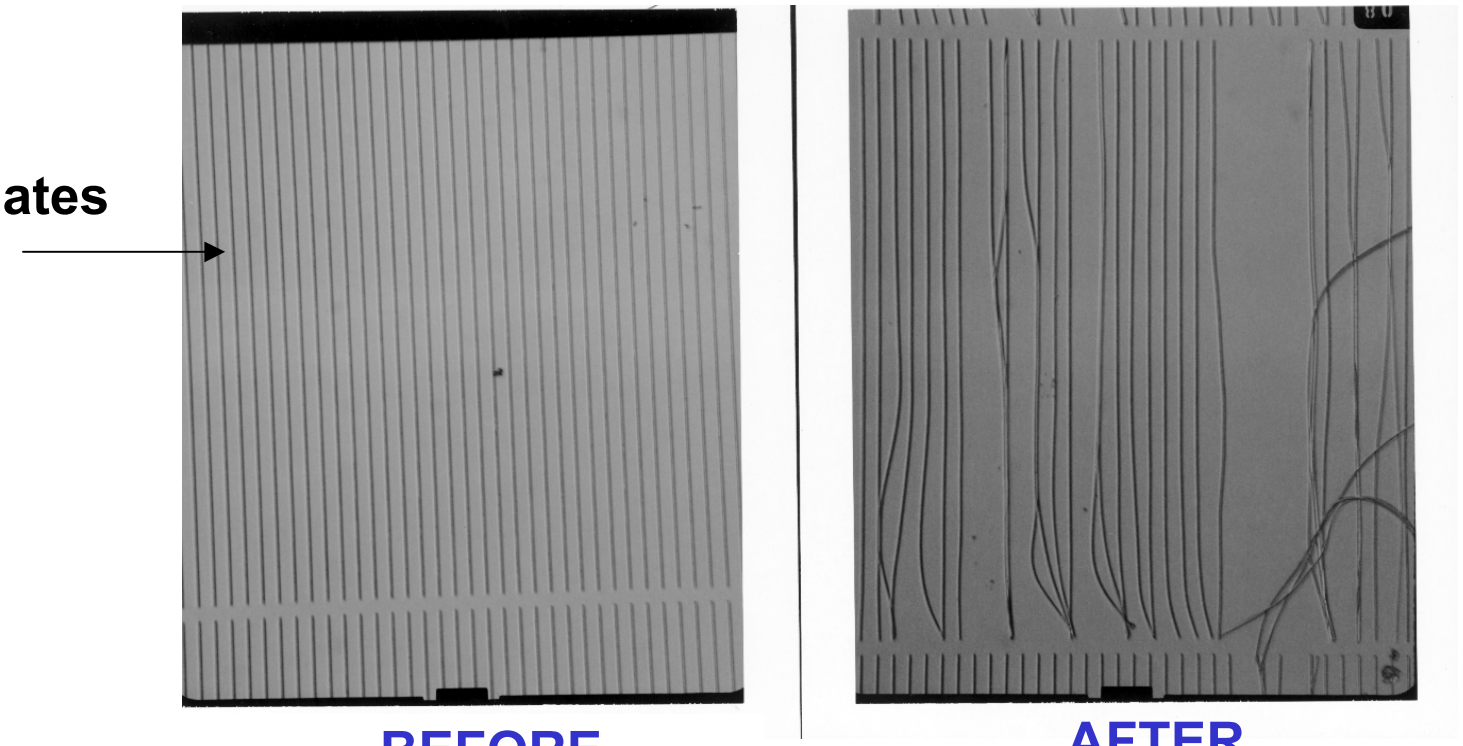
SEM of a T-gate

Problem: T-gates yield

- **Subsequent processing degrades T-gates resulting in low yield**

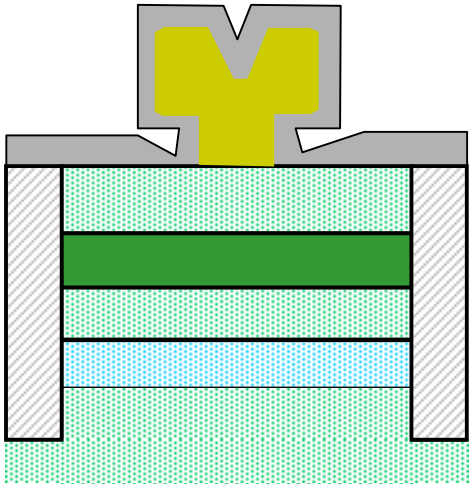
- **Serious yield limiting step involves exposure of the T-gates to BOE**
  - HF on the BOE etches Ti undercutting the T-gates

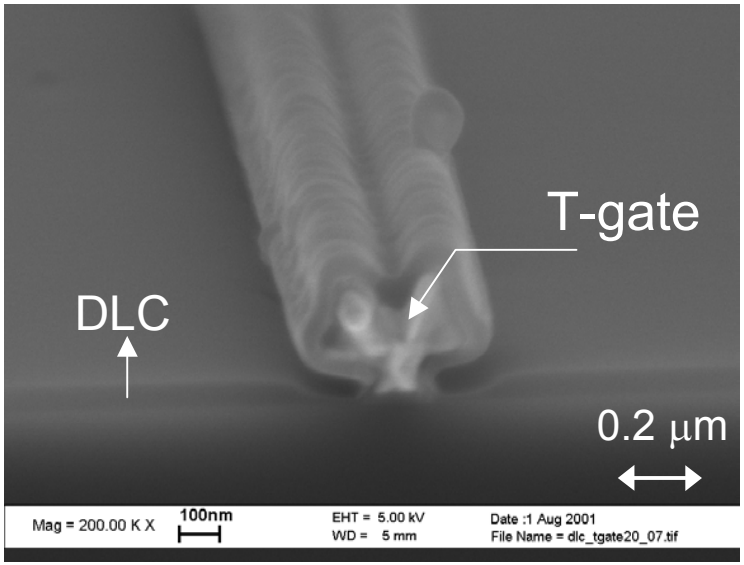
Plan view optical micrographs of T-Gates before and after a 20s 9:1HF:NH_4F (BOE) dip



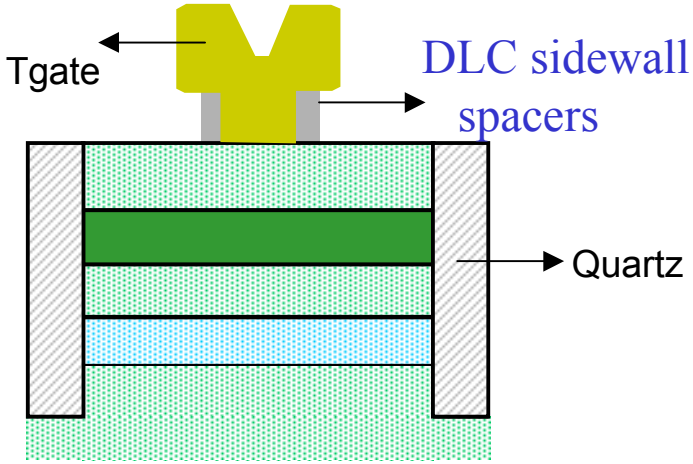
Solution: DLC sidewall spacers

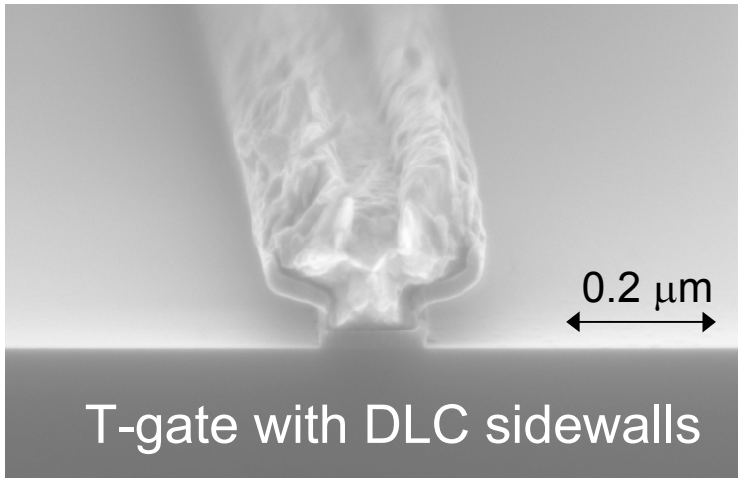
6. Conformal DLC deposition





7. Anisotropic etch of DLC

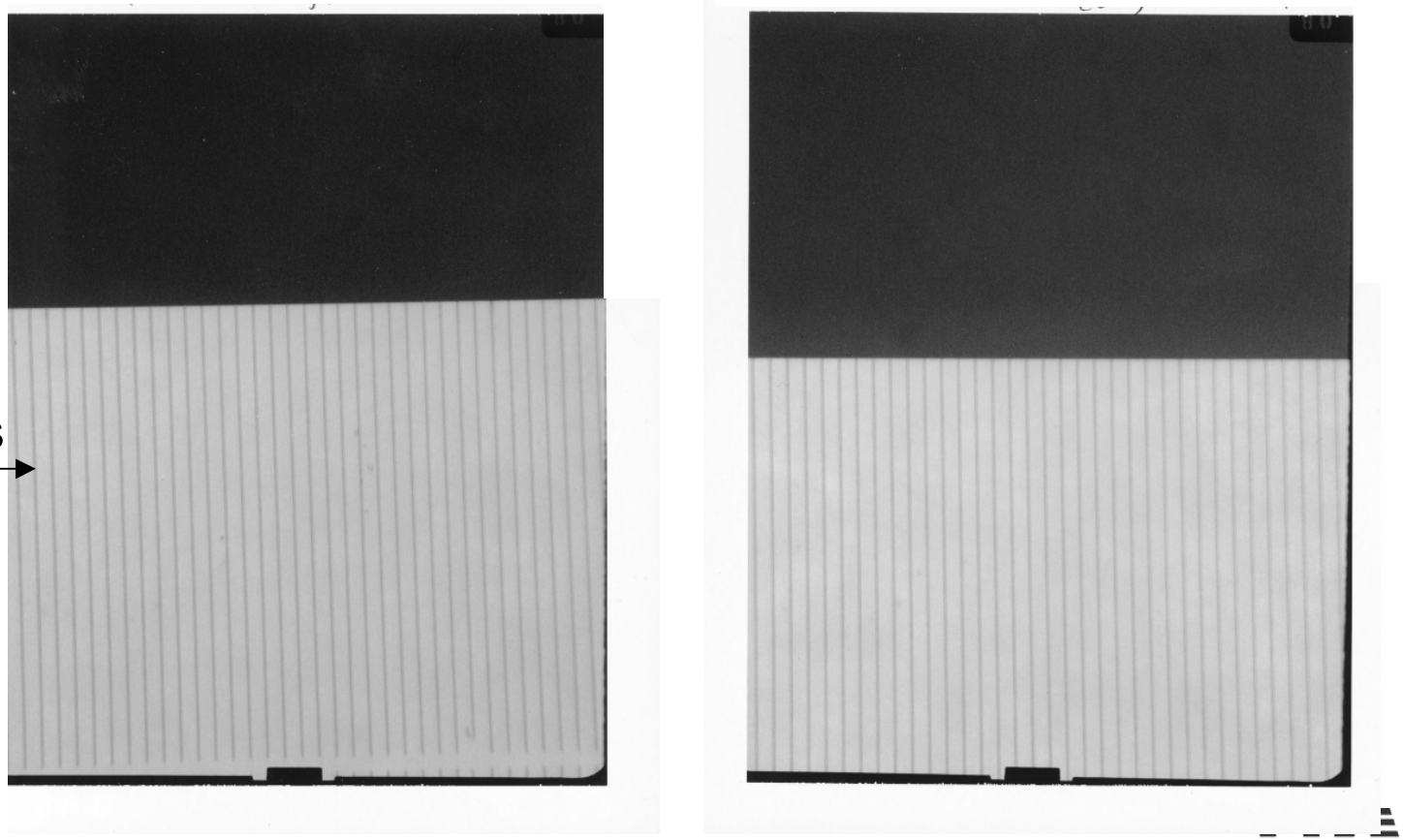




DLC is inert to most acids and has a low dielectric constant

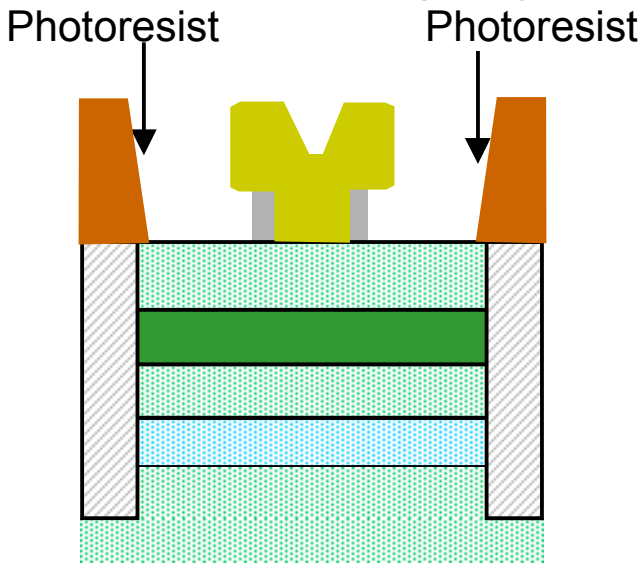
DLC sidewall spacer process

Optical Micrographs of T-Gates *with* DLC spacers before and after a 30s 9:1 HF:NH_4F (BOE) dip

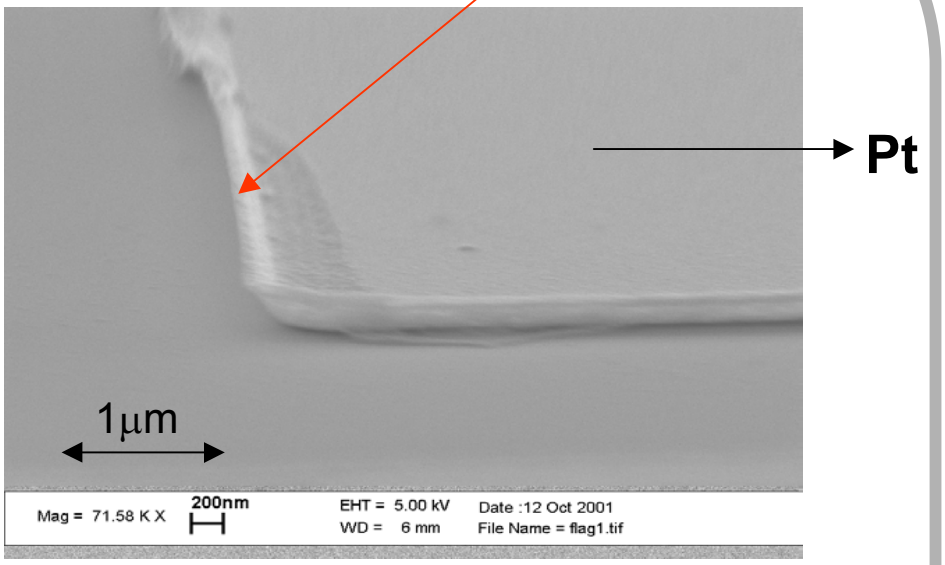


Problem: source/drain silicide formation

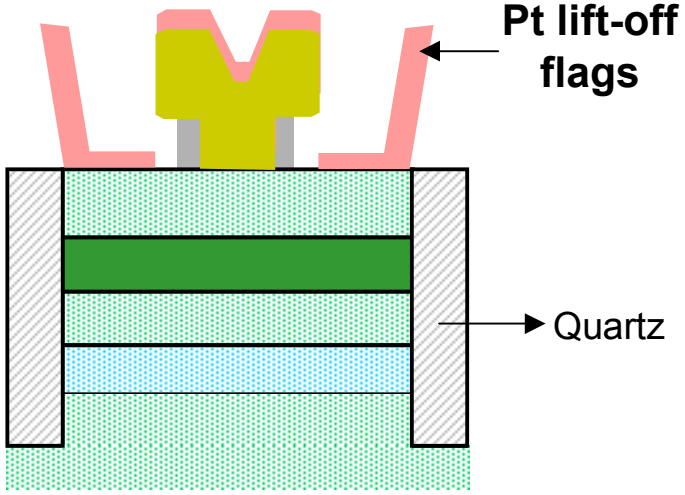
7. S/D Photolithography

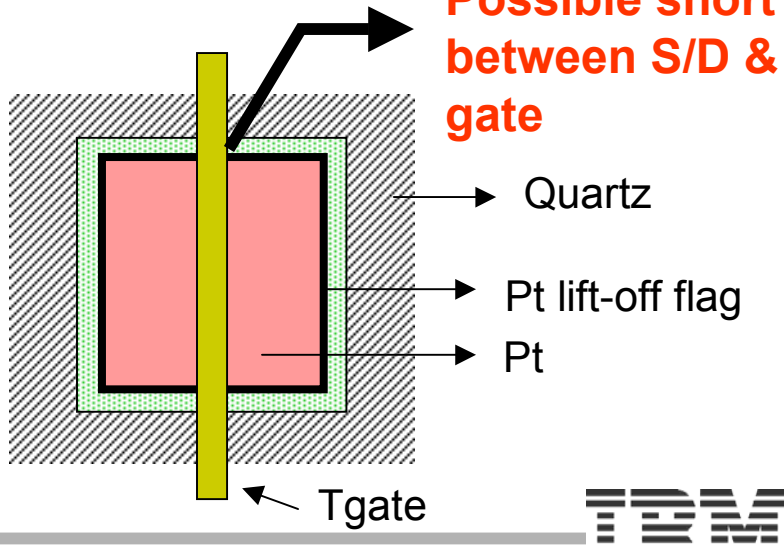


Sloped Resist sidewalls give lift-off flags



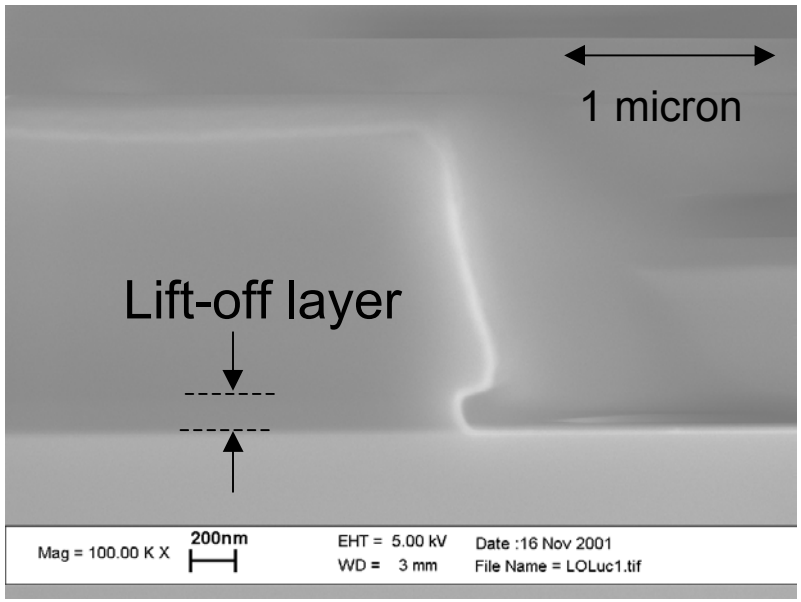
8. Pt evaporation/lift-off

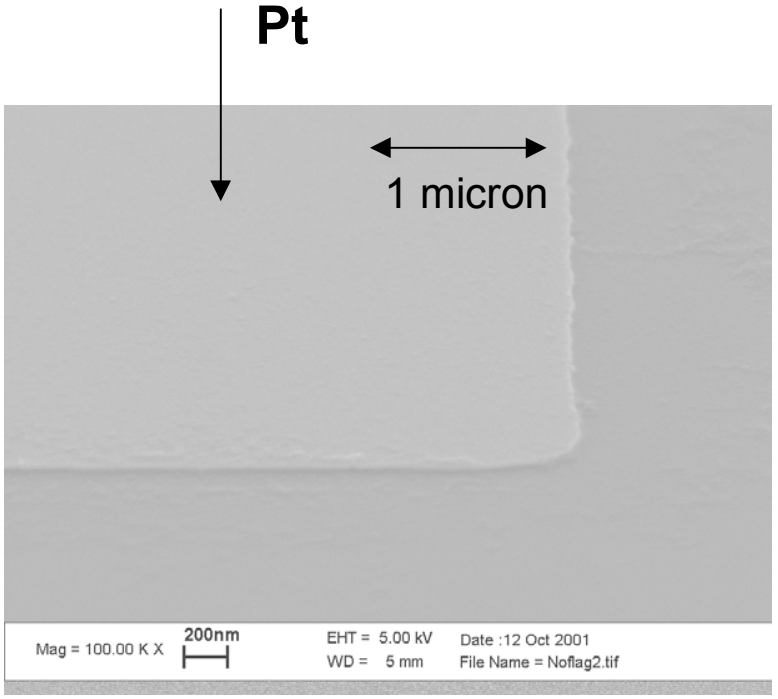




Solution: Improved lift-off process for S/D silicides

Dual layer resist used to create an undercut profile





Excellent lift-off profiles obtained using dual layer resist

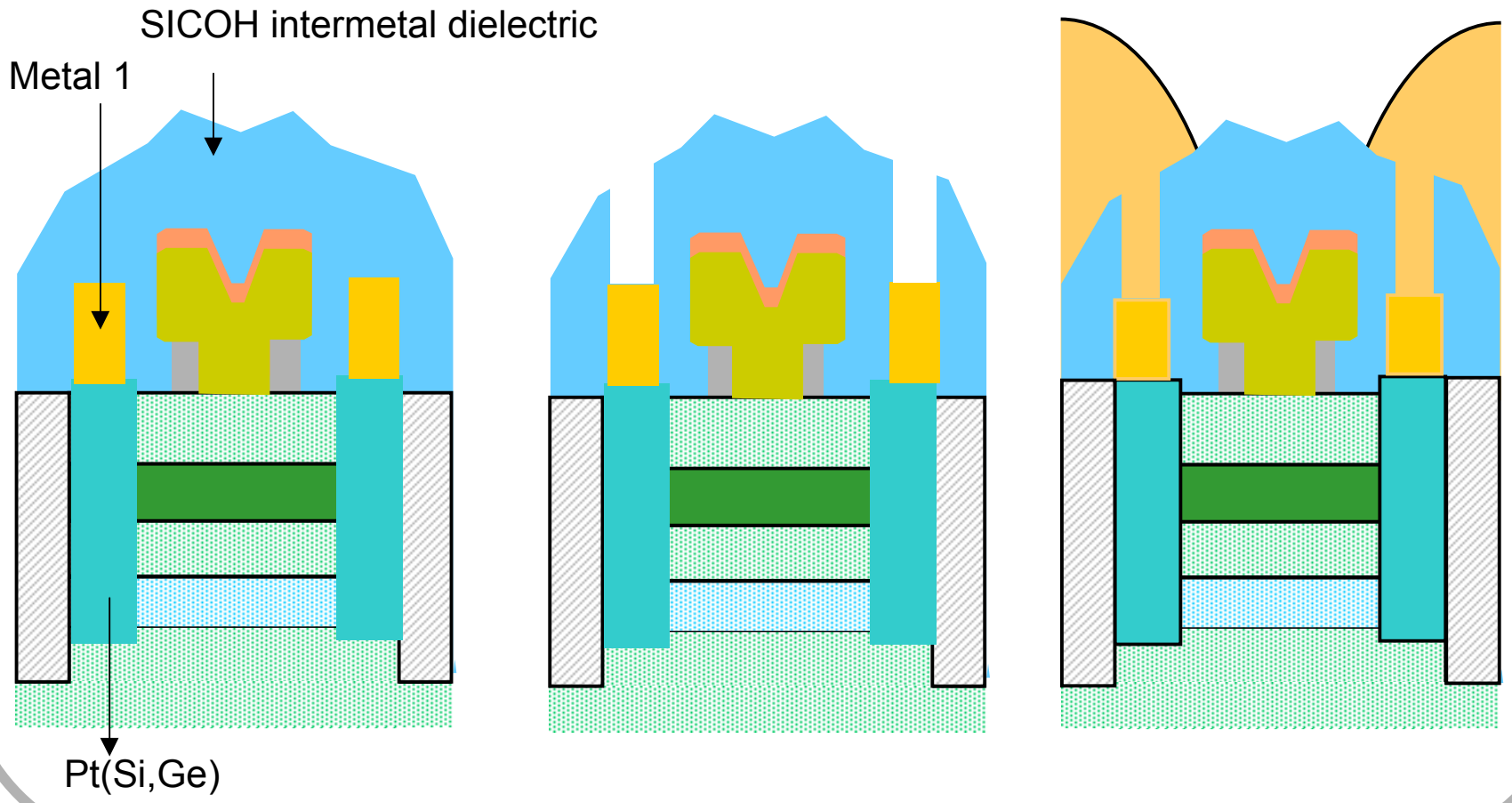
S/D to gate shorts not a yield limiting factor

New metallization process

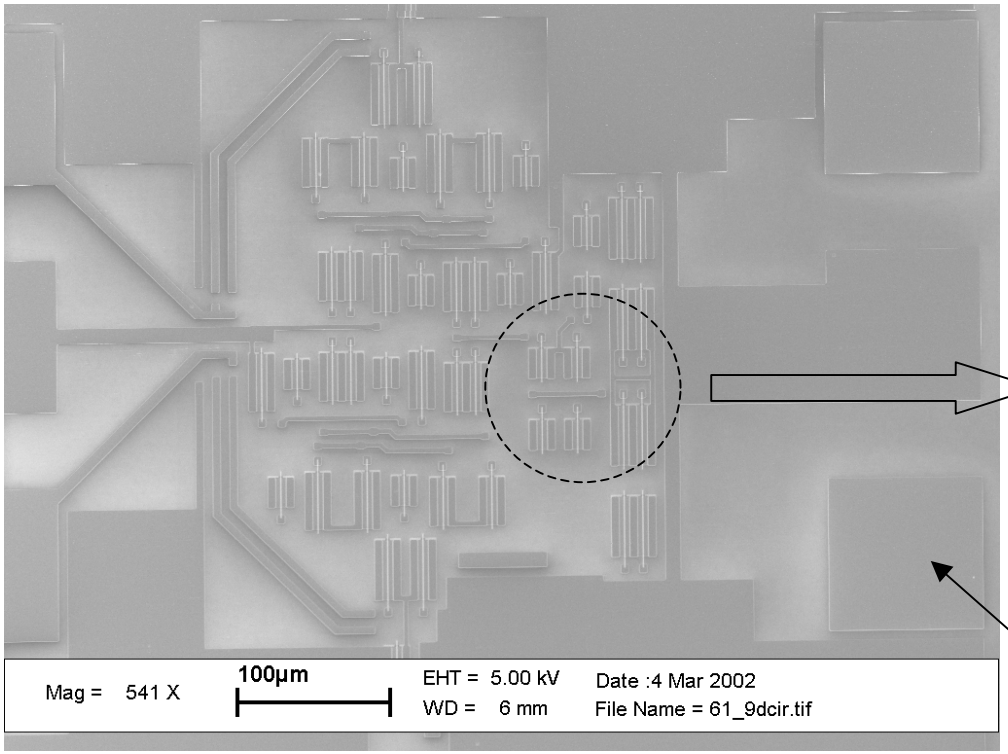
9. M1 Lithography
M1 evaporation/liftoff
Deposit intermetal dielectric

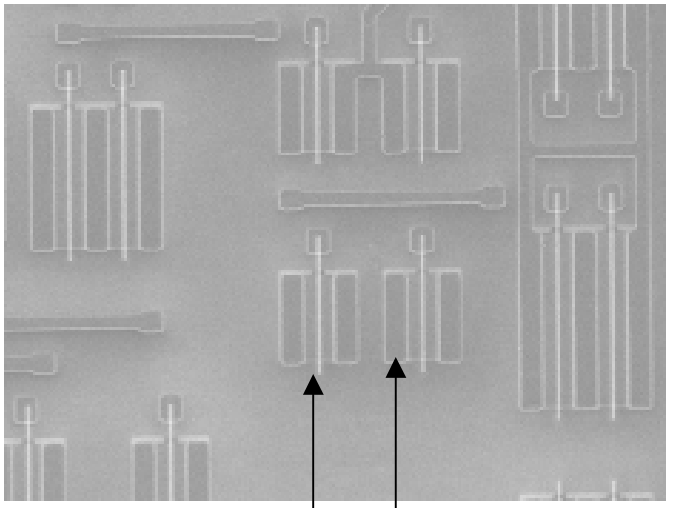
10. Via Lithography
Via etch

11. M2 evaporation
M2 lithography
M2 etch



SEM image of divider circuit after metal1





T-gate

Metal 1

Mesa + Silicide + M1

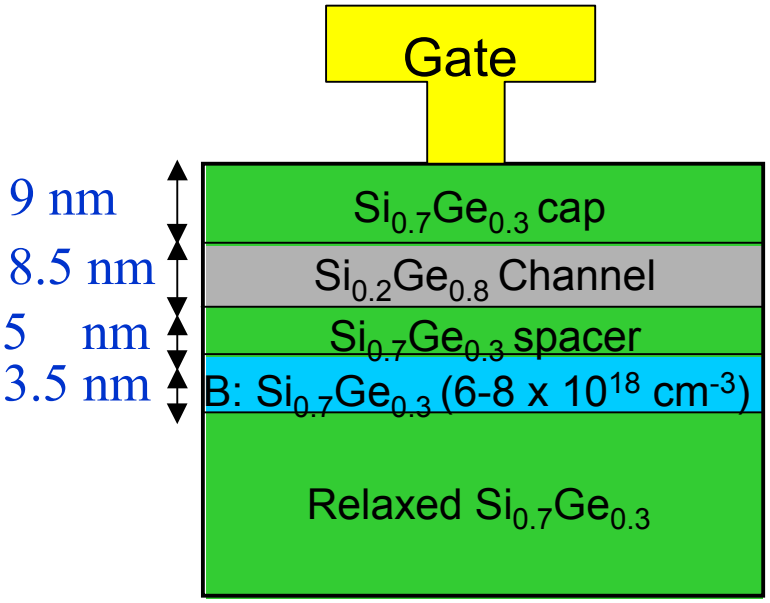
- Excellent T-Gate yield.
- No evidence of flags in Silicide or Metal 1 levels

Overview of process runs

Run	Wafers	Split	Final Level	Comments
1	Gov61-7 Gov61-9 Gov61-11 Gov61-12	1: 61-7 61-12	Metal 1	Good devices on 61-12. Poor device characteristics on 61-7 due to poor Pt lift-off during silicide formation
		2: 61-12	Metal 2	Wafer broke during metal2 litho
		3. 61-9	Metal 1	High gate leakage current Due to overetch of field oxide prior to gate deposition
		4. 61-9	Metal 1	Reprocessed. Unintentional gate oxide caused large V_t shift
2	66-6, 66-10, 66-11 67-6, 67-10, 67-11	1. 66-10 67-11	Metal 1	Excellent yield on both wafers

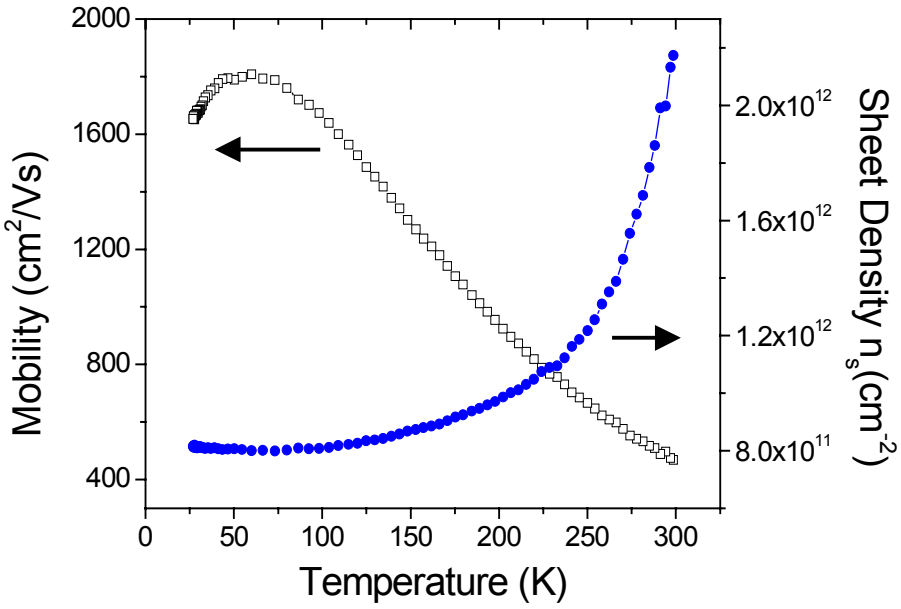
Run 1: Gov 61 wafers

Started with 4 wafers: Gov61-7, Gov61-9, Gov61-11, Gov61-12



Target Layer Structure

Low T Hall measurements
Gov 61-10



At RT μ ~ 470 cm^2/Vs and
n_s ~ $2x10^{12}$ cm^{-2}

- RT mobility and sheet density lower than targeted

Gov61-12, Gov61-7 processing

	61-12	61-7
Align mark litho/etch		
Mesa Litho/etch		
Mesa planarization(Quartz deposition & lift-off)		
T-Gate Litho (ebeam), metal evaporation + liftoff		
T-Gate sidewall formation		
Silicide Litho	T-gate sidewalls ensure high yield during HF prior to Pt evaporation	
Pt evap/lift-off/ RTA for silicide formation	Pt lift-off flags observed	Ultrasonic to remove flags resulted in Pt ripping off
Metal 1 Litho		
Metal 1 evap/Lift-off	Flags observed during M1 lift-off	

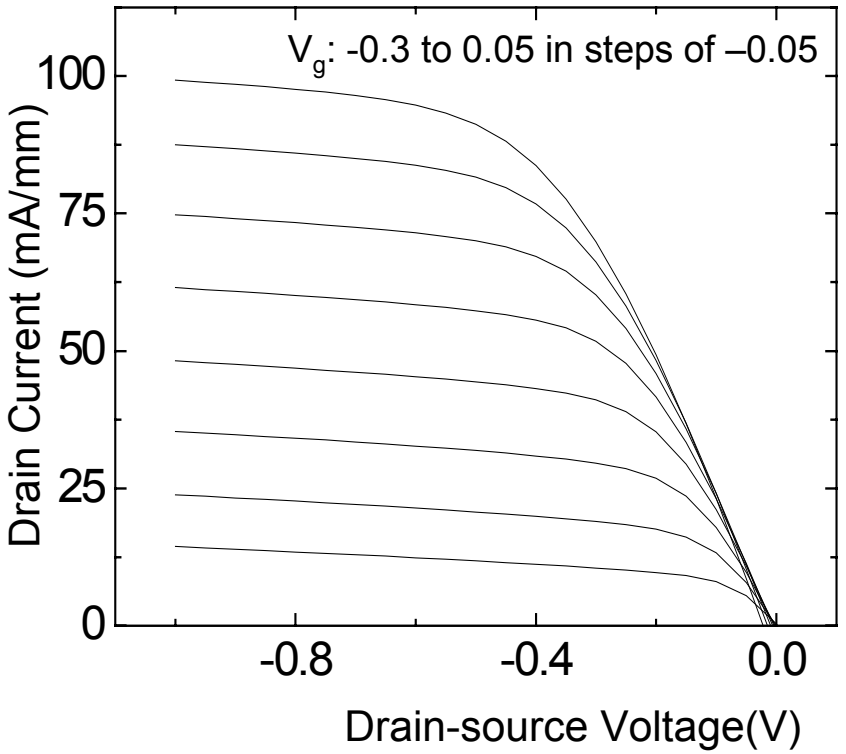
DC device testing

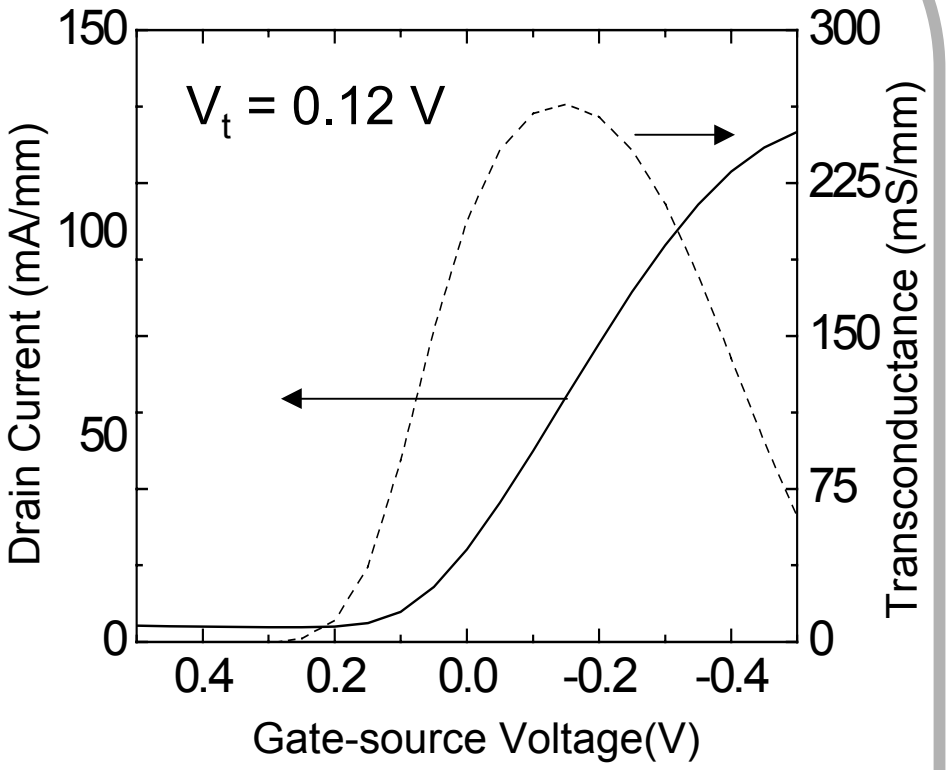
Gov 61-7, Gov 61-12 processing

	61-12	61-7
Interlevel Dielectric (DLC deposition)	Plasma damage observed in M1 during dep. DLC adhesion problem	
Strip the DLC		
Interlevel dielectric (SICOH deposition)		
Via Hole litho/ SICOH RIE etch		
Metal 2 deposition		
Metal 2 litho + etch	**Wafer broke**	

DC characteristics: GOV61-12

Width = 20 μm, Length = 0.15 μm



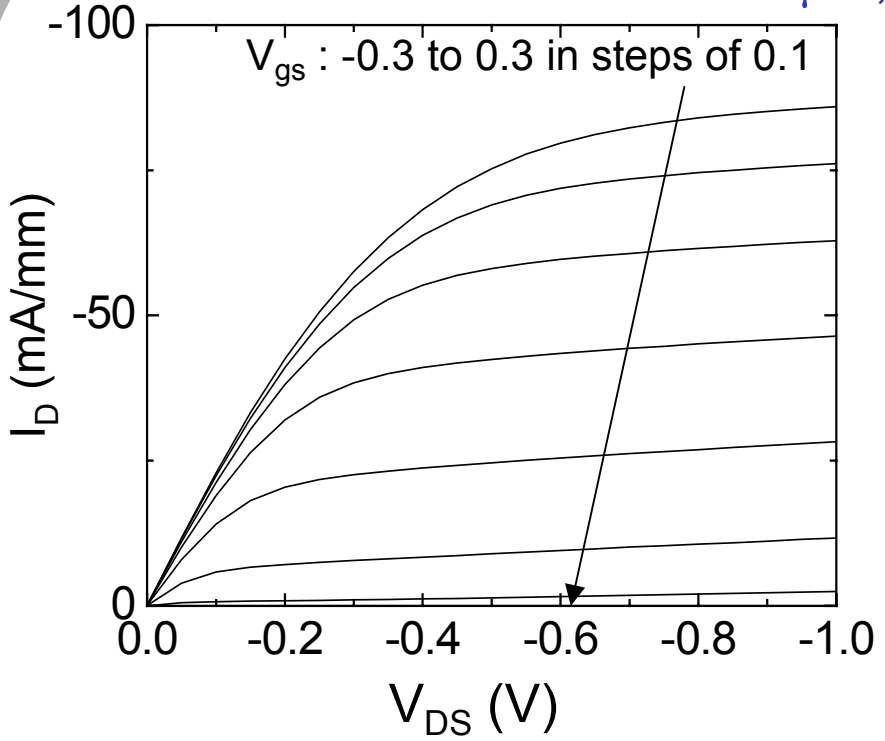


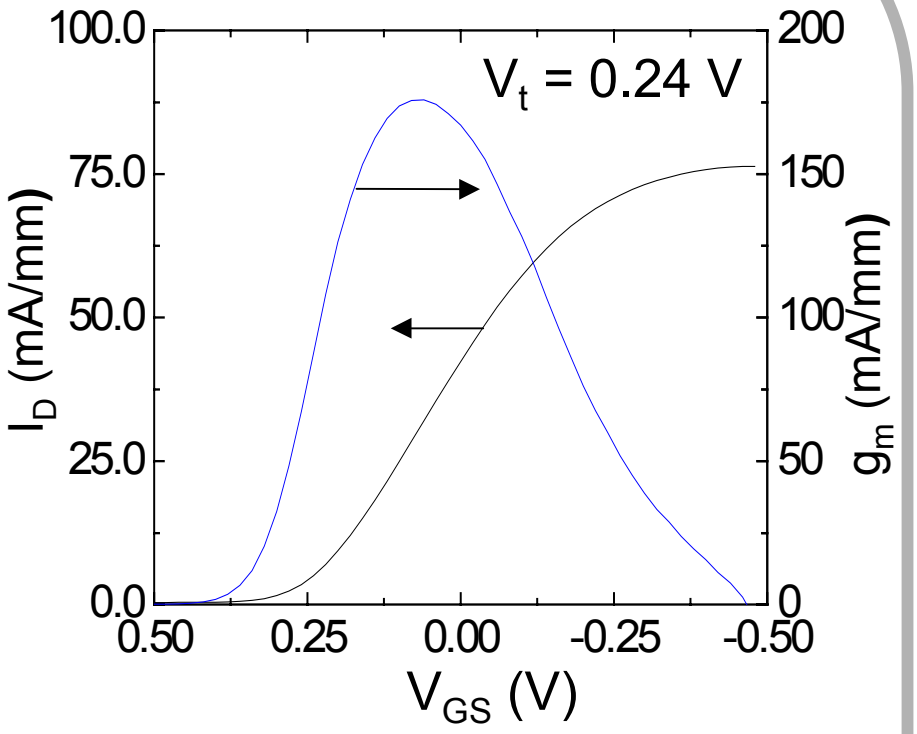
Excellent output characteristics:
g_o ~ 7.5 mS/mm
(V_{GS} = -0.1V and V_{DS} = -0.6V)

Max g_m ~ 265 mS/mm (V_{DS} = 0.6V)
DC V_{gain} : g_m/g_o ~ 35

DC characteristics: GOV61-7

Width = 20 μm, Length = 0.15 μm





g_o ~ 5 mS/mm
(V_{GS} = 0 V and V_{DS} = -0.6V)

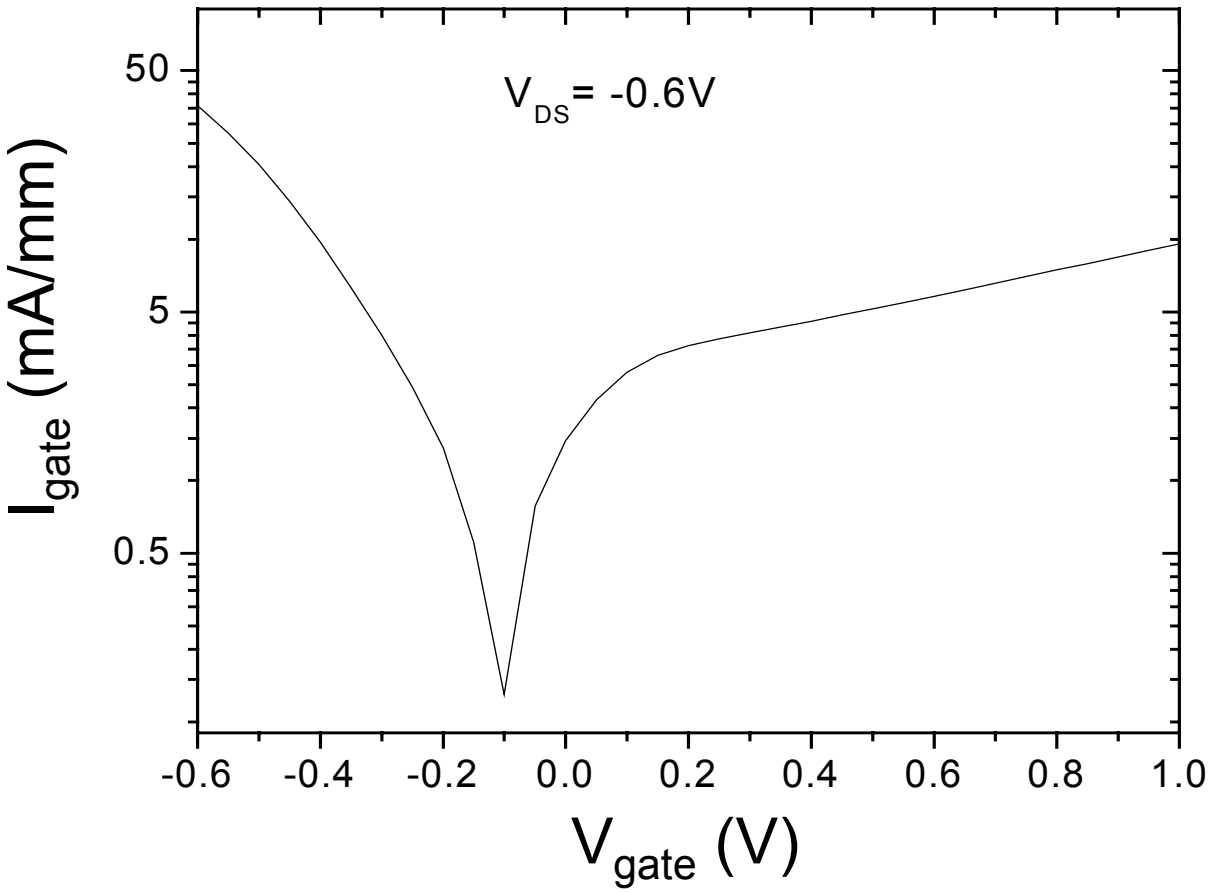
Max g_m ~ 176 mS/mm (V_{DS} = 0.6V)
DC V_{gain} : g_m/g_o ~ 35

$$I_{DSAT} \propto g_m \qquad g_{m,ext} = g_{mo}/(1 + g_{mo}R_s)$$

- Pt adhesion problem during Silicide formation resulted in large R_s
- Large variation in R_s across the wafer resulting in poor yield

Gate Leakage Current: GOV61-12

Width = 20 μm, Length = 0.15 μm

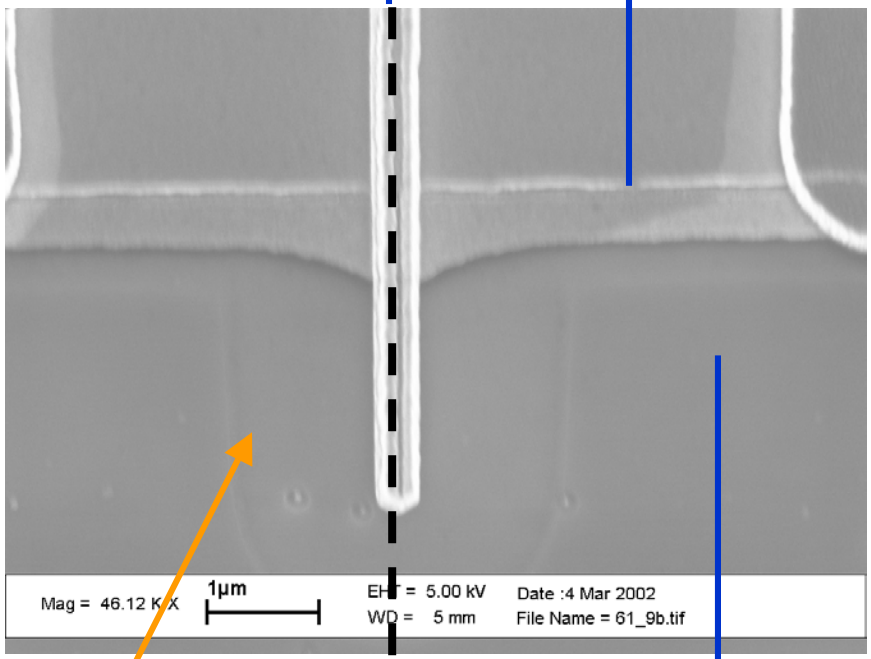


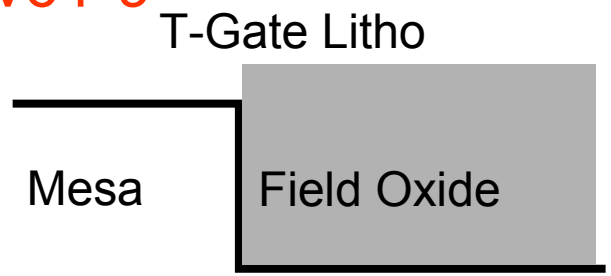
- Gate leakage current a little high, but typical for these gate stacks
- Possibly enhanced gate leakage at the edge of the mesas

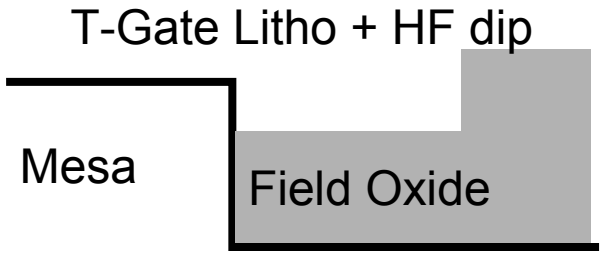
Gov61-9 processing

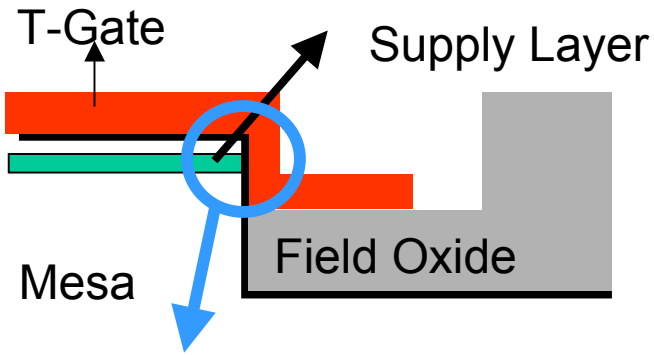
	61-9
Align mark litho/etch	
Mesa Litho/etch	
Mesa planarization(Quartz deposition & lift-off)	
T-Gate Litho (ebeam)	
HF dip/ T-Gate evaporation and lift-off	Timed HF dip too long. Etched field oxide
T-Gate sidewall formation	
Silicide Litho	T-gate sidewalls ensure high yield during HF prior to Pt evaporation
Pt evap/lift-off/ RTA for silicide formation	Dual layer resist provides excellent lift-off profiles
Metal 1 Litho	
Metal 1 evap/Lift-off	Devices all have extremely high gate leakage

Gate leakage: Gov61-9







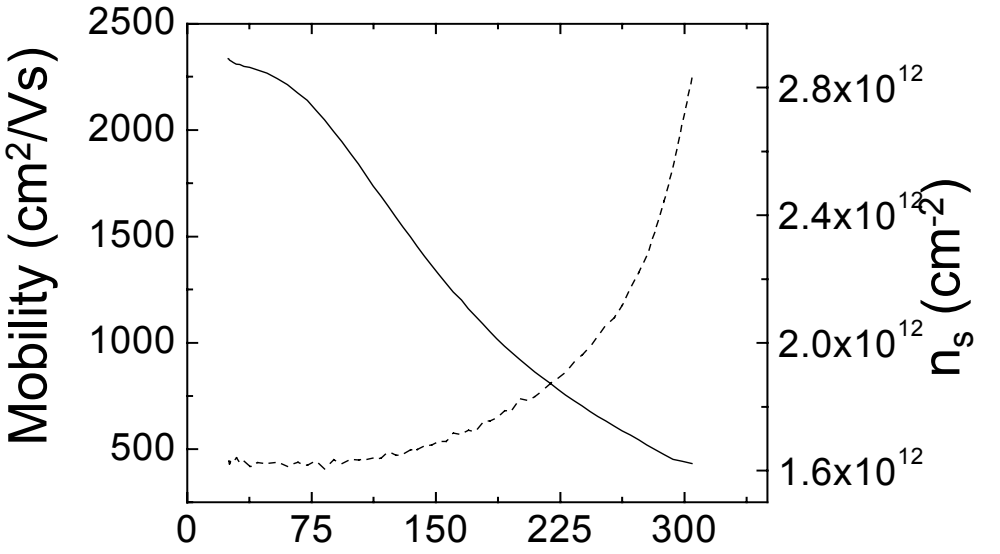


SOURCE OF GATE LEAKAGE

INCREASE THE FIELD OXIDE THICKNESS FOR RUN-66

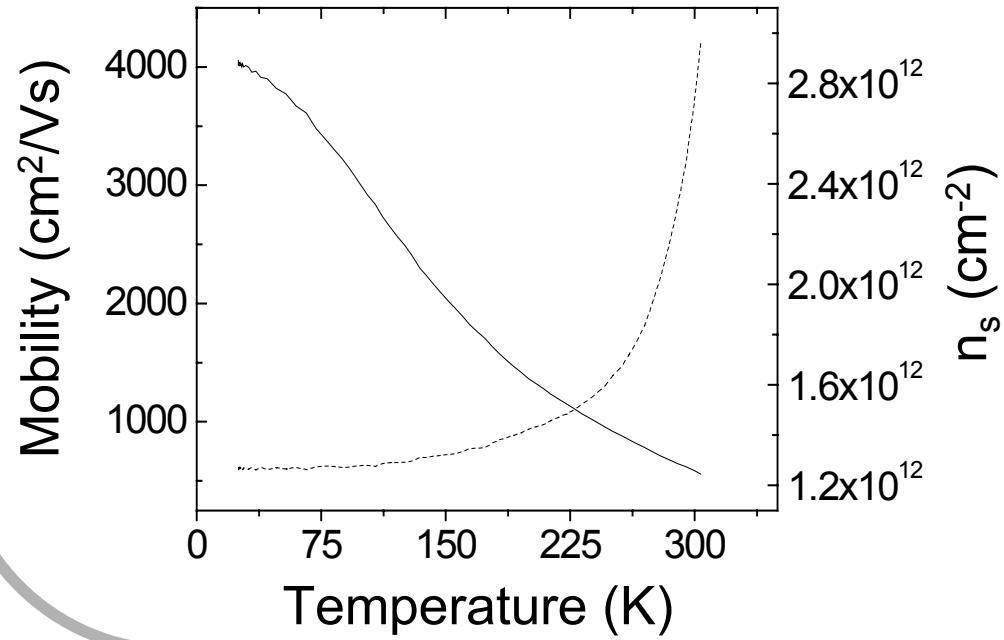
RUN 2: GOV66,67 wafers

Started with 6 wafers: Gov66-6, Gov66-10, Gov66-11, Gov67-6, Gov67-10, Gov67-11



GOV 66-7

At RT μ ~ 430 cm^2/Vs,
n_s ~ 2.8x10^{12} cm^{-2}

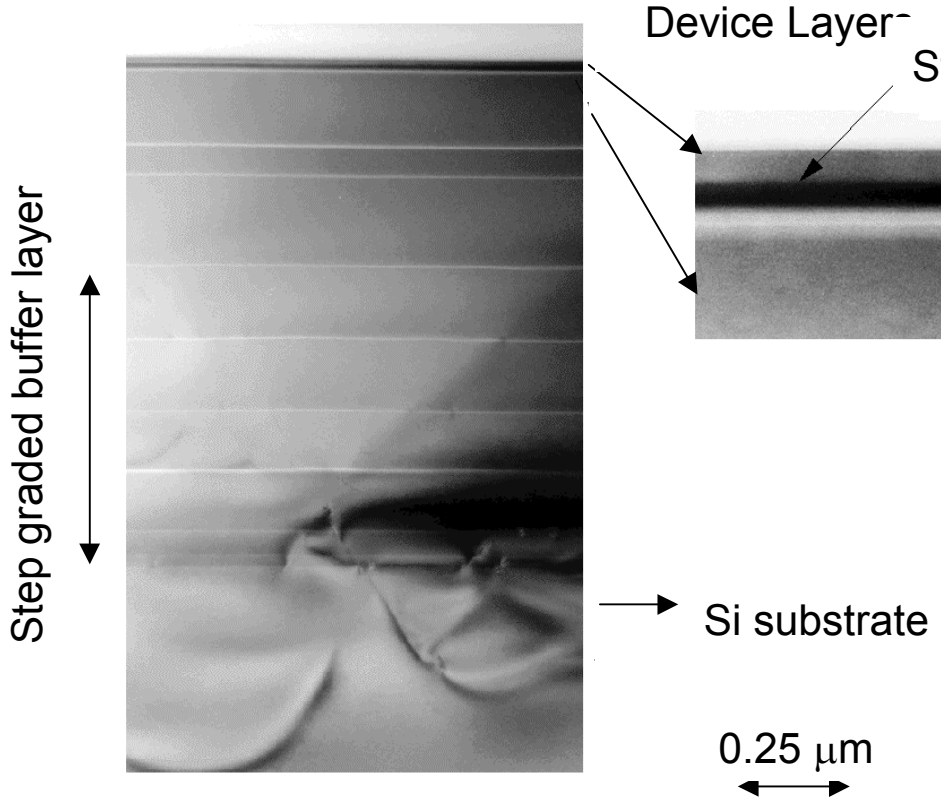


GOV 67-7

At RT μ ~ 550 cm^2/Vs,
n_s ~ 3x10^{12} cm^{-2}

XTEM: Gov64-7

Gov64-7 grown using identical conditions as Gov66,67 wafers



LAYER THICKNESSES

in ( ) is the target

SiGe cap : 7.7(9)nm
SiGe QW : 6.3(8.5)nm
Spacer : 4 (5)nm
Supply : 3(3.5) nm

- Layer thicknesses thinner than targeted
- Thinner cap explains lower threshold voltages
- Thinner supply and SiGe QW results in less confinement in the QW
  - larger parallel conduction path and hence lower μ

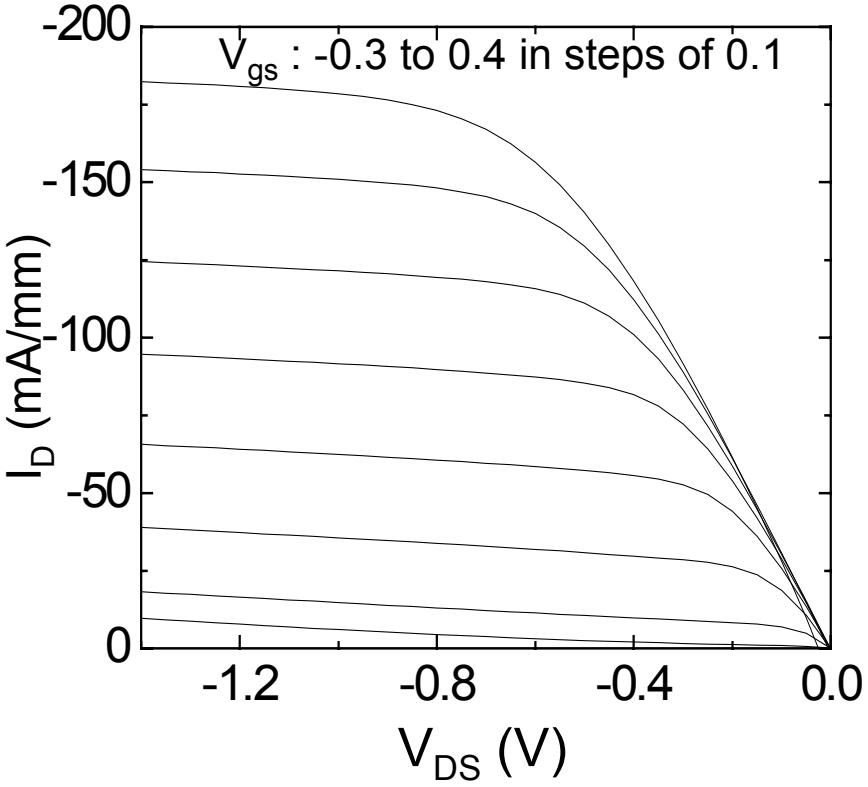
Gov 66-10, Gov 67-11 processing

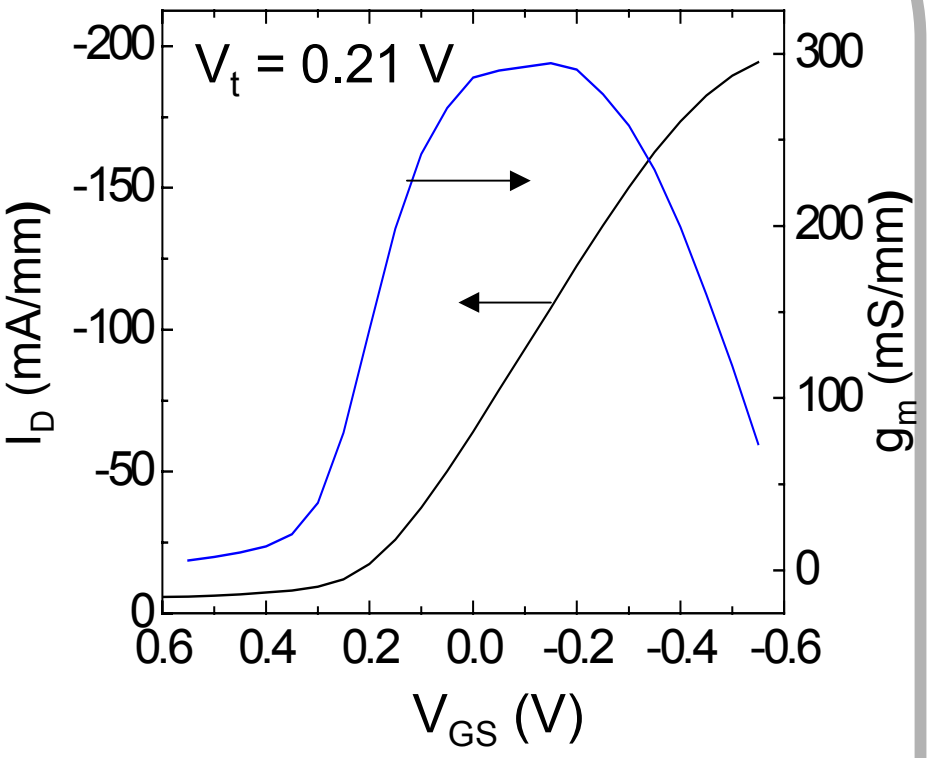
	66-10	67-11
Align mark litho/etch		
Mesa Litho/etch		
Mesa planarization(Quartz deposition & lift-off)		
T-Gate Litho (ebeam), metal evaporation + liftoff		
T-Gate sidewall formation		
Silicide Litho		
Pt evap/lift-off/ RTA for silicide formation		
Metal 1 Litho		
Metal 1 evap/Lift-off		

AC, DC device testing

DC characteristics: Gov66-10

Width = 20 μm, Length = 0.15 μm



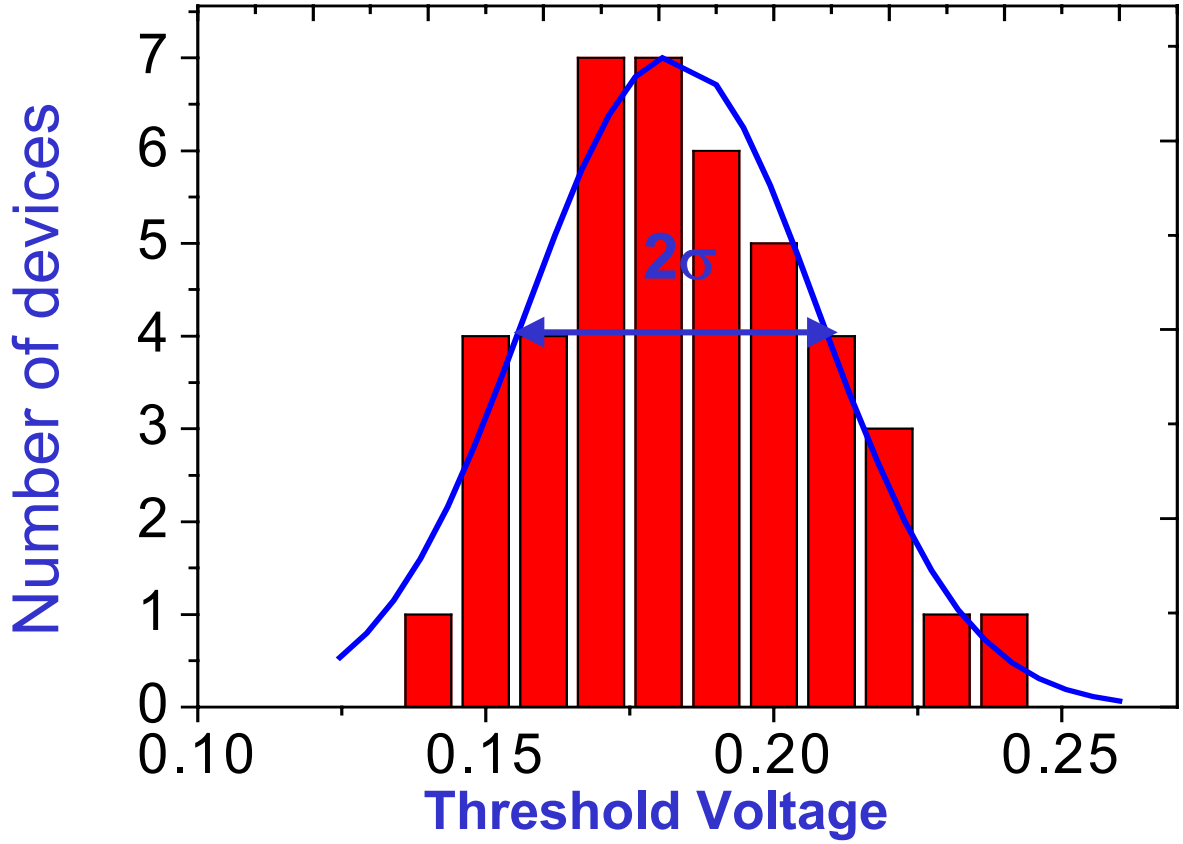


Excellent output characteristics:
g_o ~ 9 mS/mm
(V_{GS} = 0 V and V_{DS} = -0.8V)

Max g_m ~ 300 mS/mm (V_{DS} = 0.8V)
DC V_{gain} : g_m/g_o ~ 33

Threshold voltage variation: Gov66-10

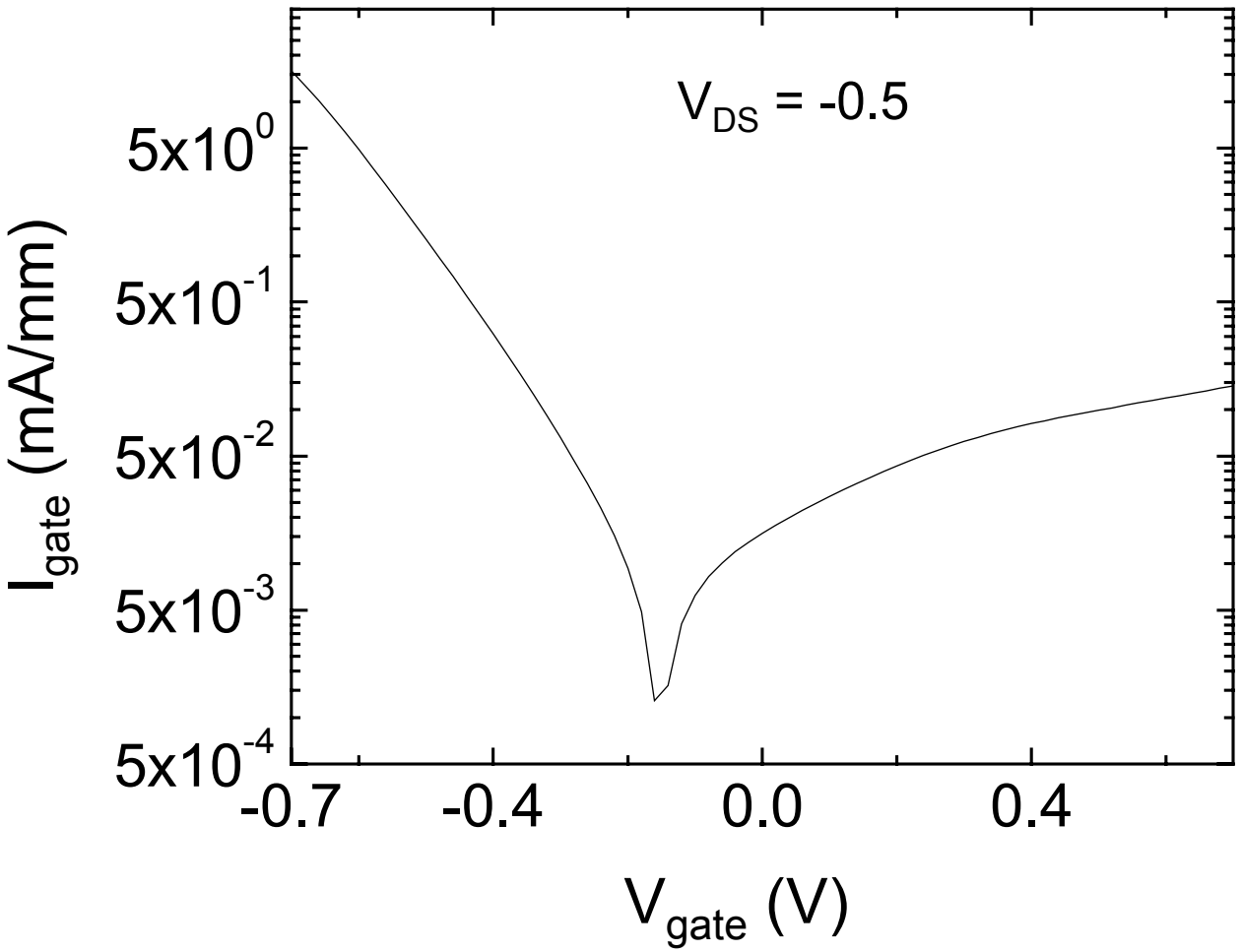
Assuming a gaussian distribution $P = \frac{A}{\sigma\sqrt{2\pi}} \exp\{-\frac{(x-\mu)^2}{2\sigma^2}\}$



- Number of devices measured : 45
- Yield : 100 %
- Standard deviation σ : 25 mV
- Mean V_t : 0.182 V

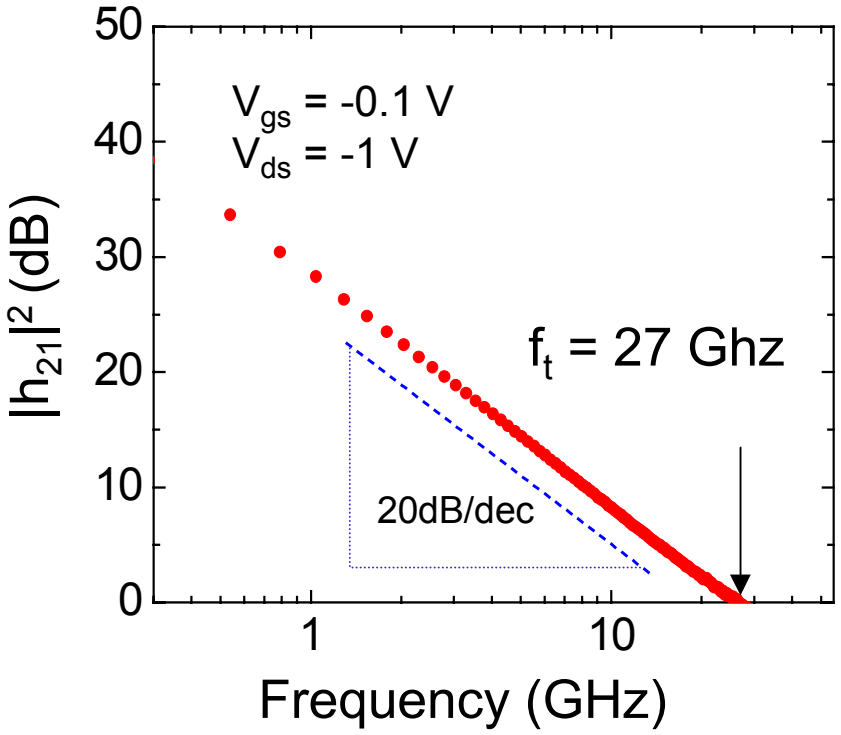
Gate leakage current: Gov66-10

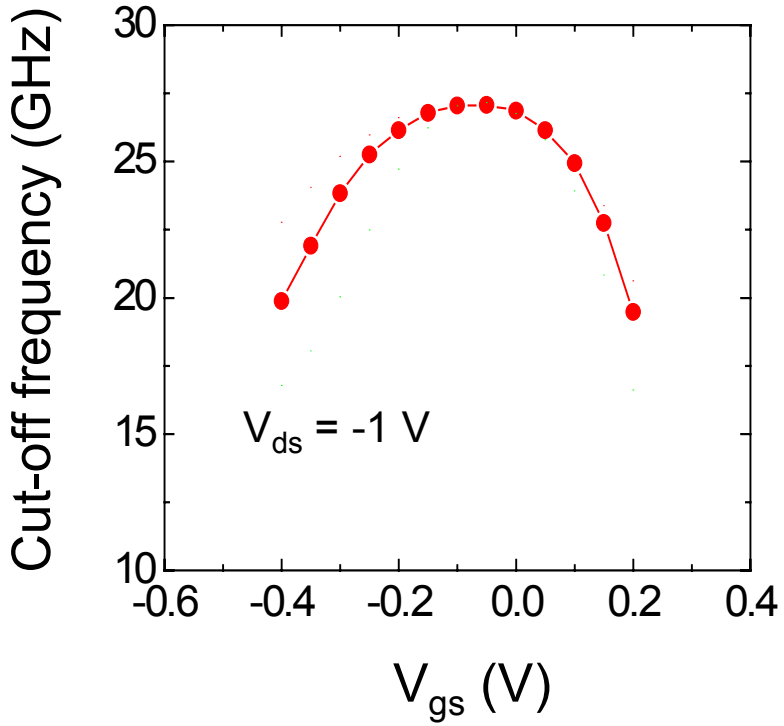
Width = 20 μm, Length = 0.15 μm



Low gate leakage

S-parameter: Gov66-10



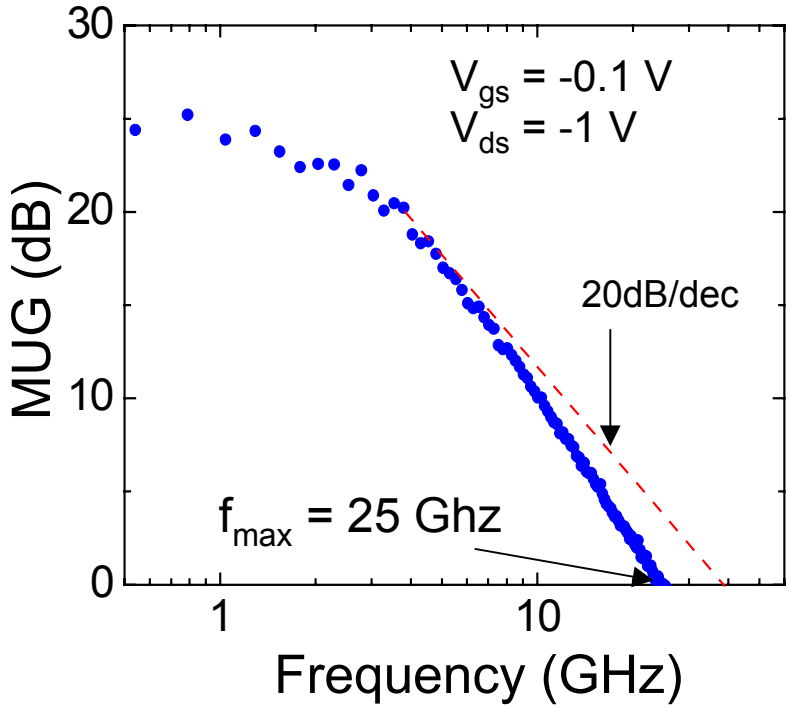


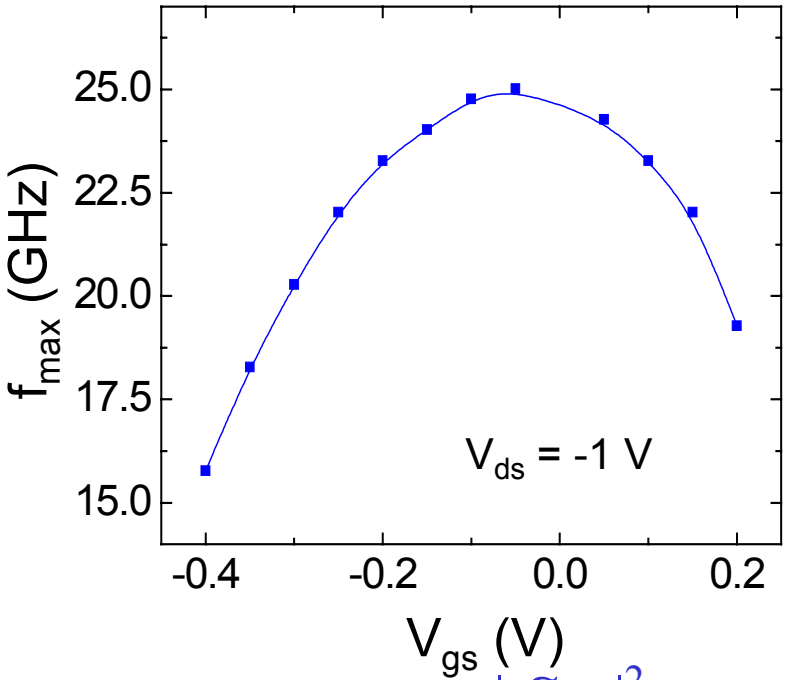
- F_t values consistent with measured mobilities and device layer structure

Discussion

Parameter	66-10	Koester et al. *IEEE EDL 2001*	Ratio 66-10/Koester (measured)	Ratio 66-10/Koester (expected)
Mobility, μ (cm^2/Vs)	**550**	**910**	**0.6**	**NA**
Gate to Source Capacitance (C_{gs})	**$\propto 1/d_{cap}$ (by XTEM)**		**1.3**	**NA**
Transcondustance, g_m (mS/mm)	**300**	**380**	**0.77**	**0.78**
Cut-off frequency, f_t (GHz)	**28**	**50**	**0.56**	**0.6**

Power Gain vs frequency: Gov66-10

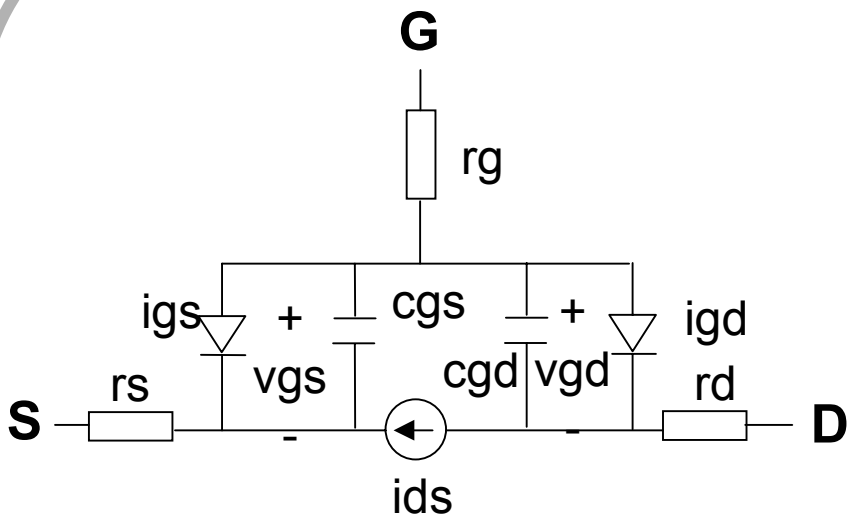




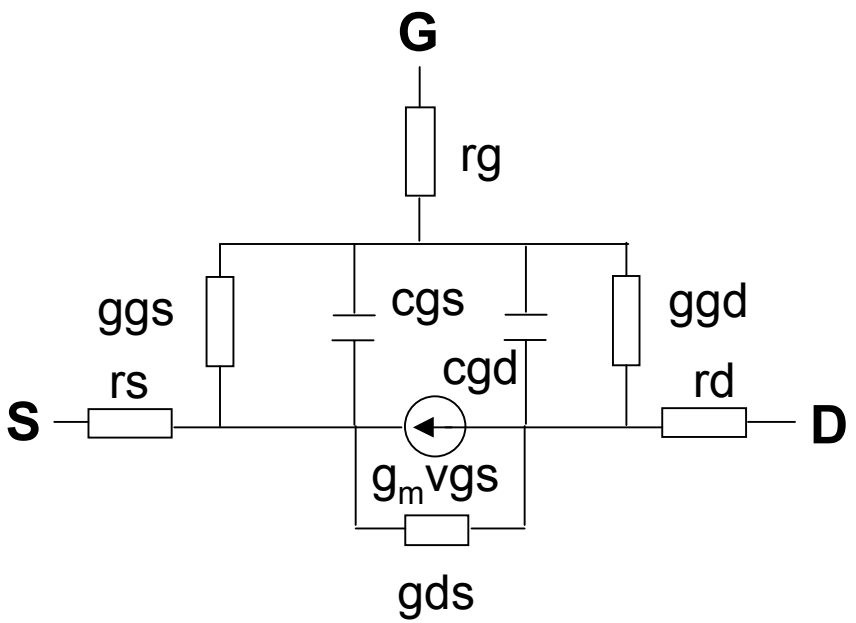
Maximum Unilateral Power Gain (MUG) $G_u = \dfrac{|S_{21}|^2}{\left|(1-|S_{11}|^2)(1-|S_{22}|^2)\right|}$

- **MUG drops anomalously fast (slope > 20 dB/decade)**
- **Standard FET small signal model does not replicate behaviour of S_{22} in the high frequency regime**

SPICE models of *p*-MODFETs



Transient Analysis



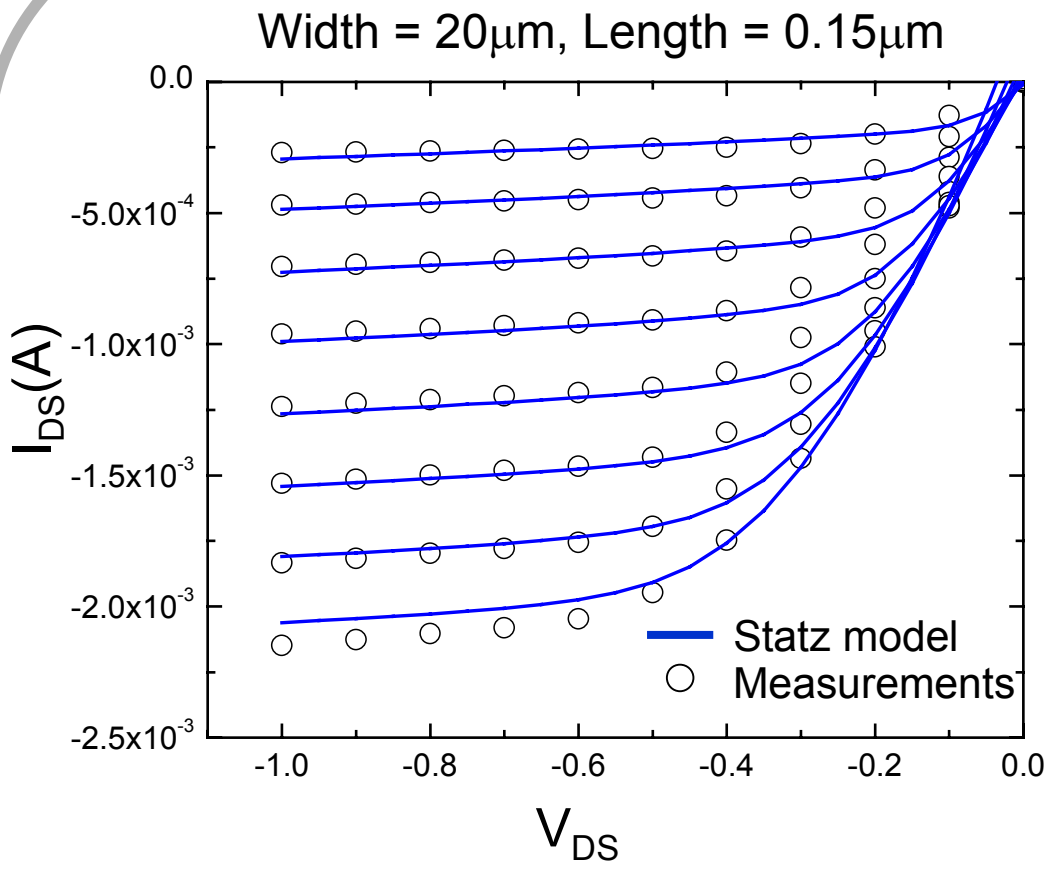
AC Analysis

Statz model used to model ids, igs, igd, cgs, cgd

g_m, ggs, ggd, gds for small signal analysis are obtained through partial differentiation

*Statz model is the most sophisticated SPICE model for MESFETs

Statz model DC parameter extraction: Gov61-12



Extracted Parameters

VTO = 0.1755 : Threshold Voltage
BETA = 1.025e-4
UCRIT = 0.8513
LAMBDA = 0.1962: Output conductance
ALPHA = 6.729
Rs = Rd = 60
IS = 4.16e-6** : **Gate Leakage current
n=2.963

STATZ model for I_{DS} and I_G

$$I_{DS} = beteff * V_{gst}^2(1 + LAMBDA.V_{ds})[1 - (1 - ALPHA.V_{ds}/3)] \quad for\ V_{sgt} < 0\ V_{ds} < 3/ALPHA$$

$$I_{ds} = beteff * V_{gst}^2(1 + LAMBDA.V_{ds})\ for\ V_{gst} < 0\ V_{sd} > 3/ALPHA$$

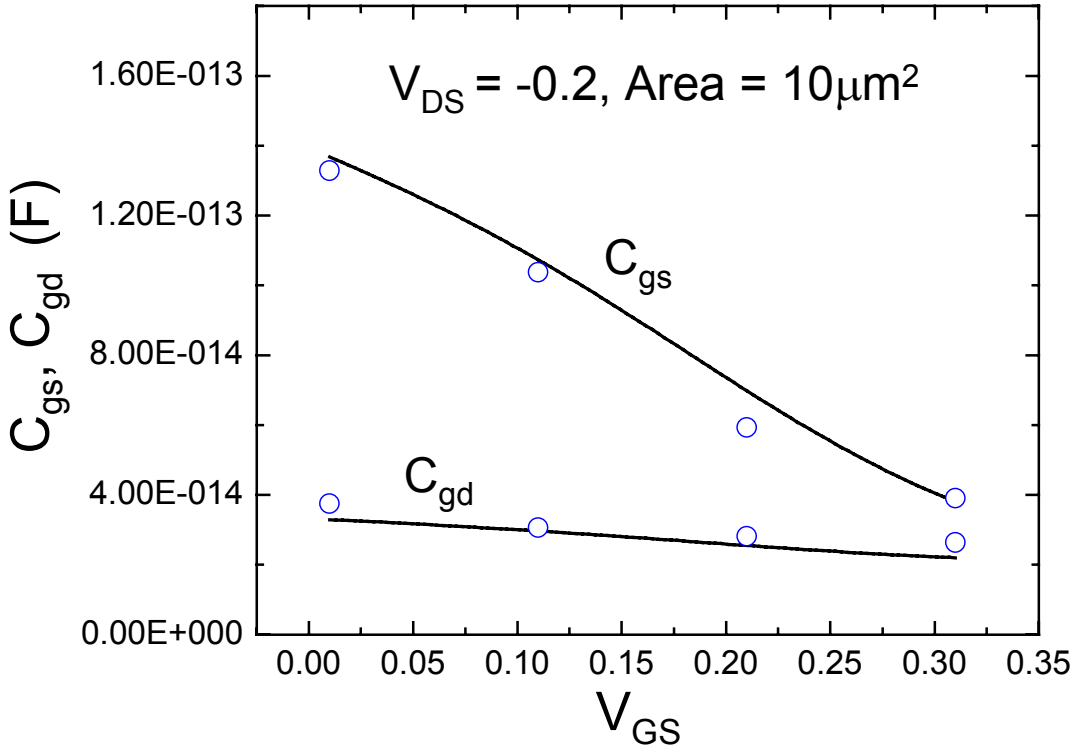
$$V_{gst} = V_{gs} - [VTO + GAMDS.vds],\ \ beteff = BETA./(1 + UCRIT.V_{gst}).(W/L)$$

$$I_G = I_S[(ezp(qV_{gs}/nkT) - 1) + (ezp(qV_{gd}/nkT)]$$

Statz transient model parameter extraction

C_{gs}, C_{gd} vs V_{gs} data from p-MODFETs fabricated by S. J. Koester*

* private communication



Extracted Parameters

From the DC Model
VTO = 0.1755
Assumed VB = 0.6

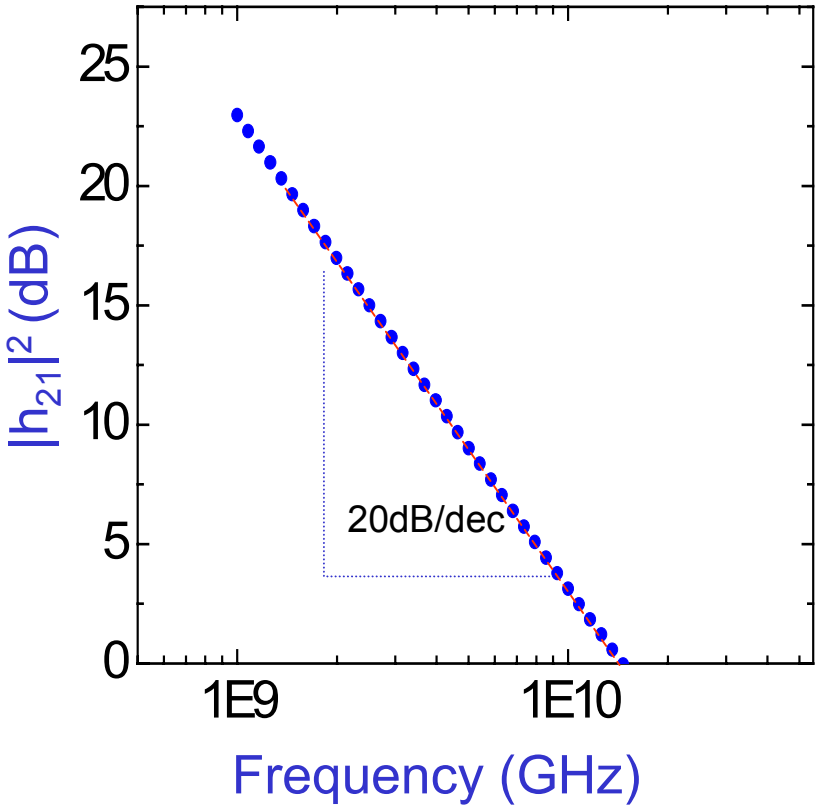
Extracted from best fit to capacitance data

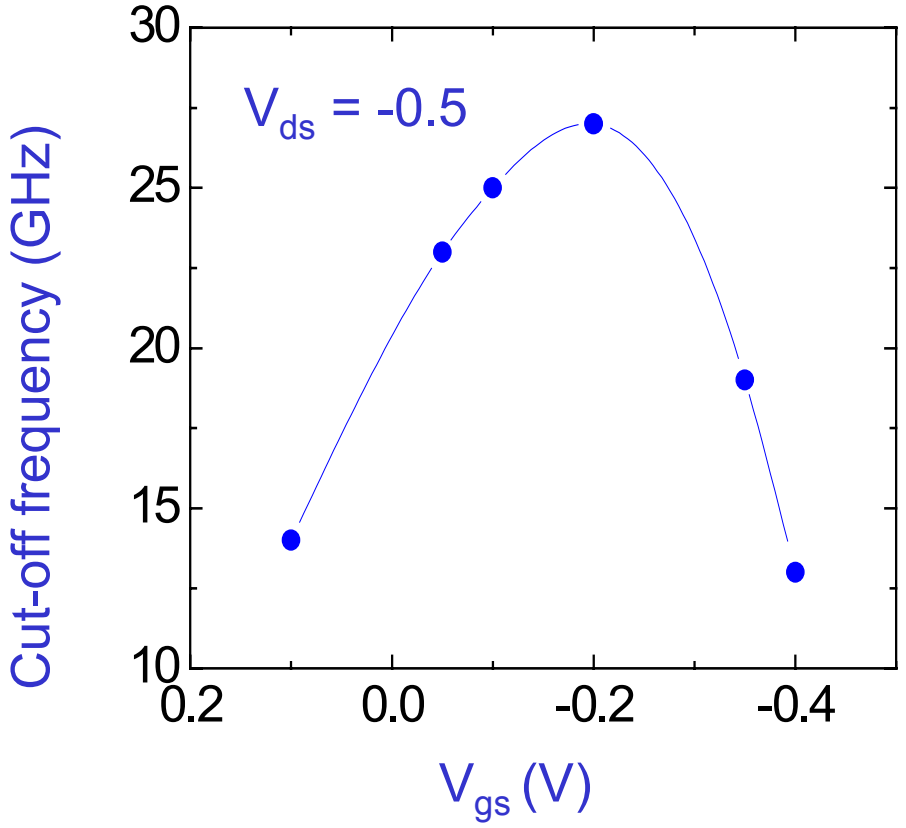
CGS0 = 1.685e-13
CGD0 = 1.786e-14

Complicated expressions for C_{gd} and G_{gs} in the Statz model.
In essence C_{gs} modelled using a standard diode-capacitance model
C_{gd} is assumed to be small and approx. independent of V_{gs} or V_{gd}

Simulated high frequency p-MODFET performance

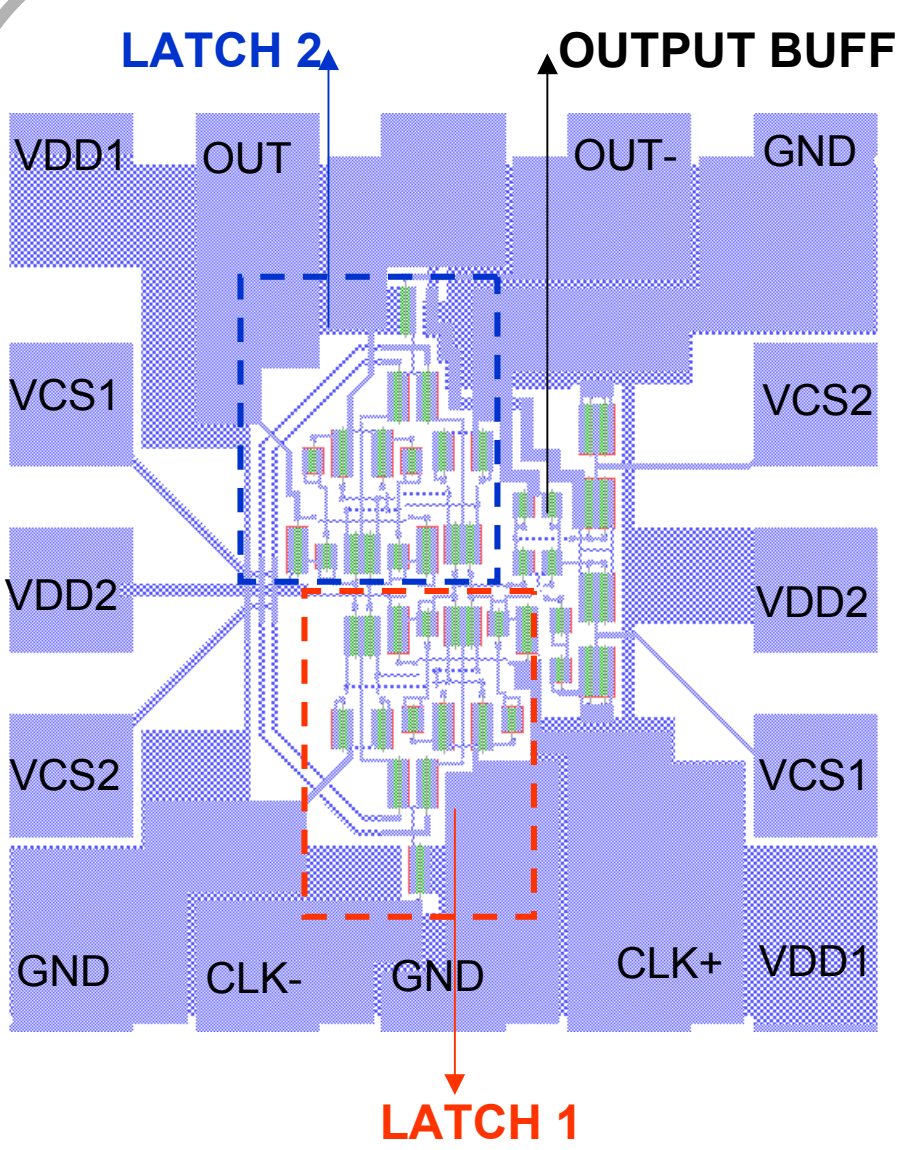
Cut-off frequency based on SPICE model parameters extracted

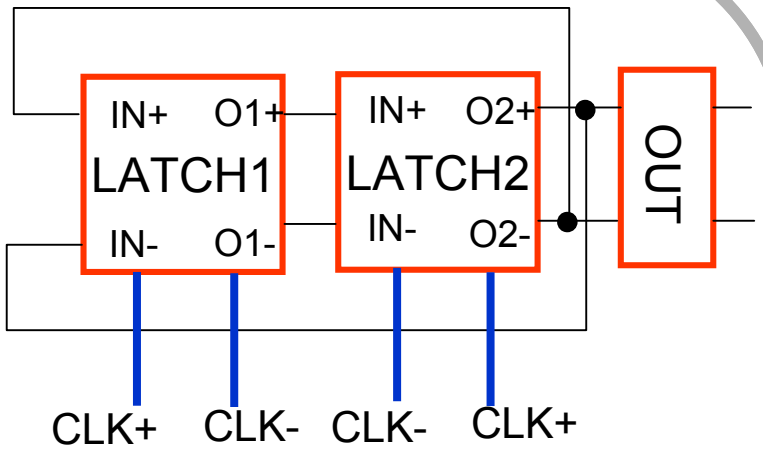




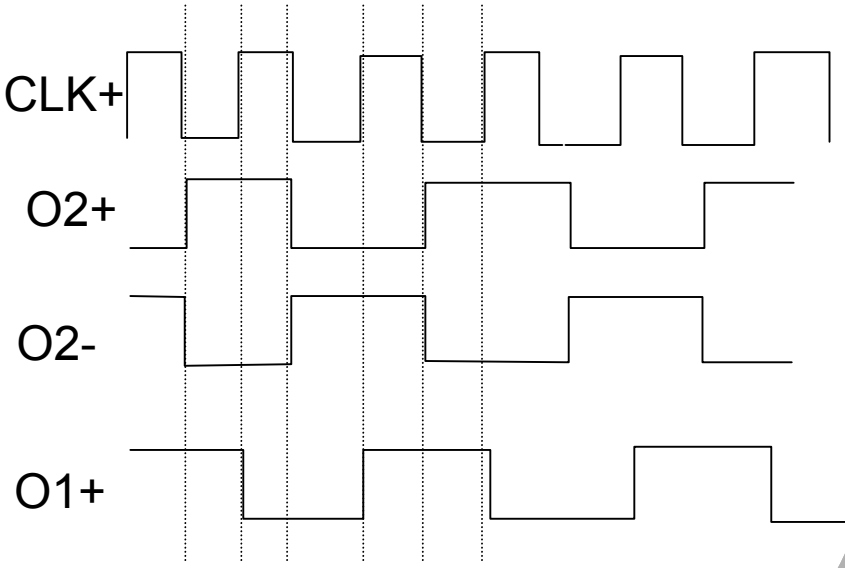
SPICE simulations of f_t qualitatively agree quite well measured values of f_t

Divider circuits: High level design

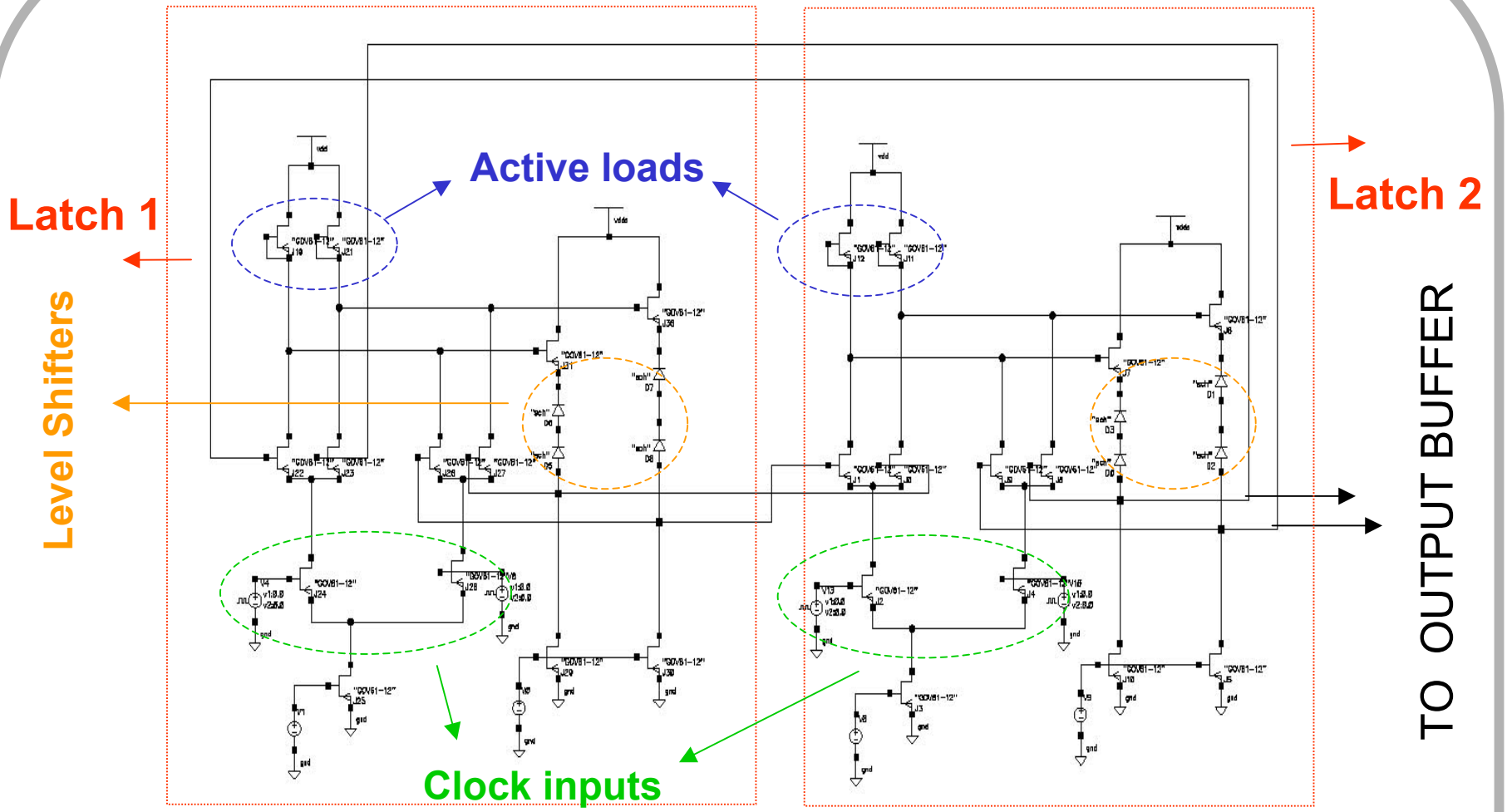




TIMING DIAGRAM



Circuit simulated in HSPICE

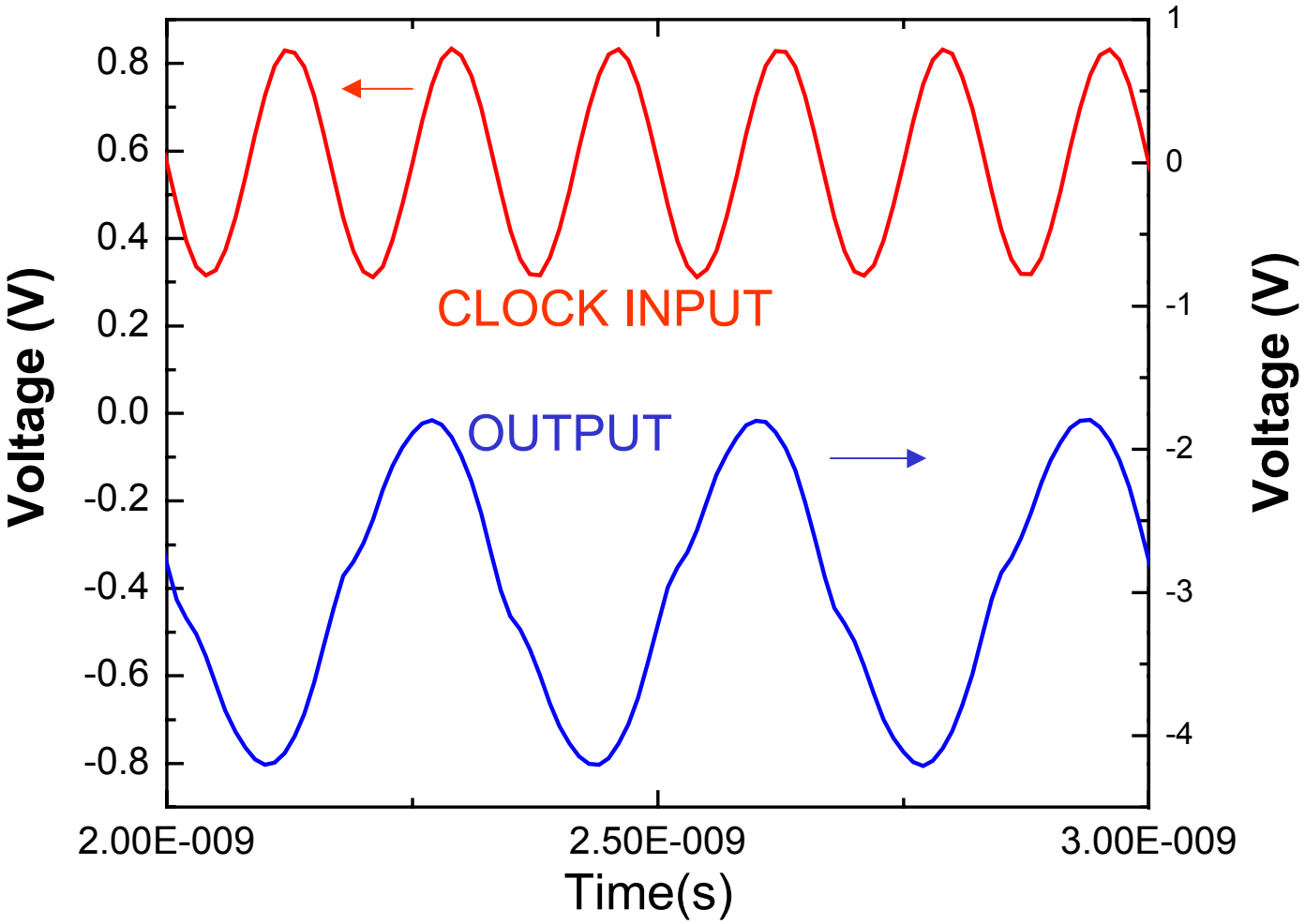


-**Loads**: gate-source shorted FETs (FETs must be normally ON for loads to function)
Drive current through loads (speed of circuit) depends on V_t

-**Level shifters :** Schottky diodes between gate-source of a FET.

Simulated frequency divider

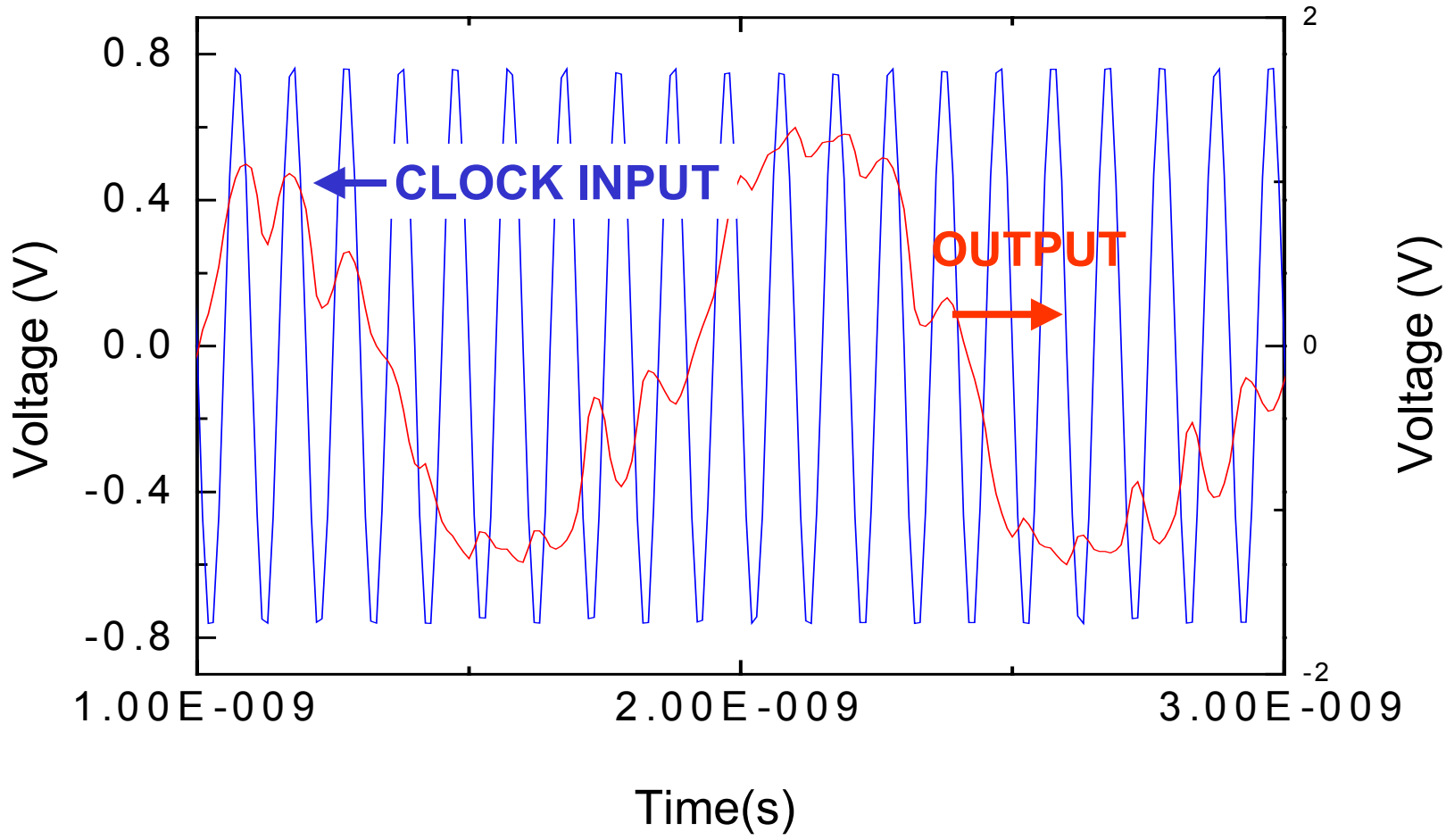
Using the SPICE parameters extracted from the DC, AC measurements



Clock frequency = 5 GHz

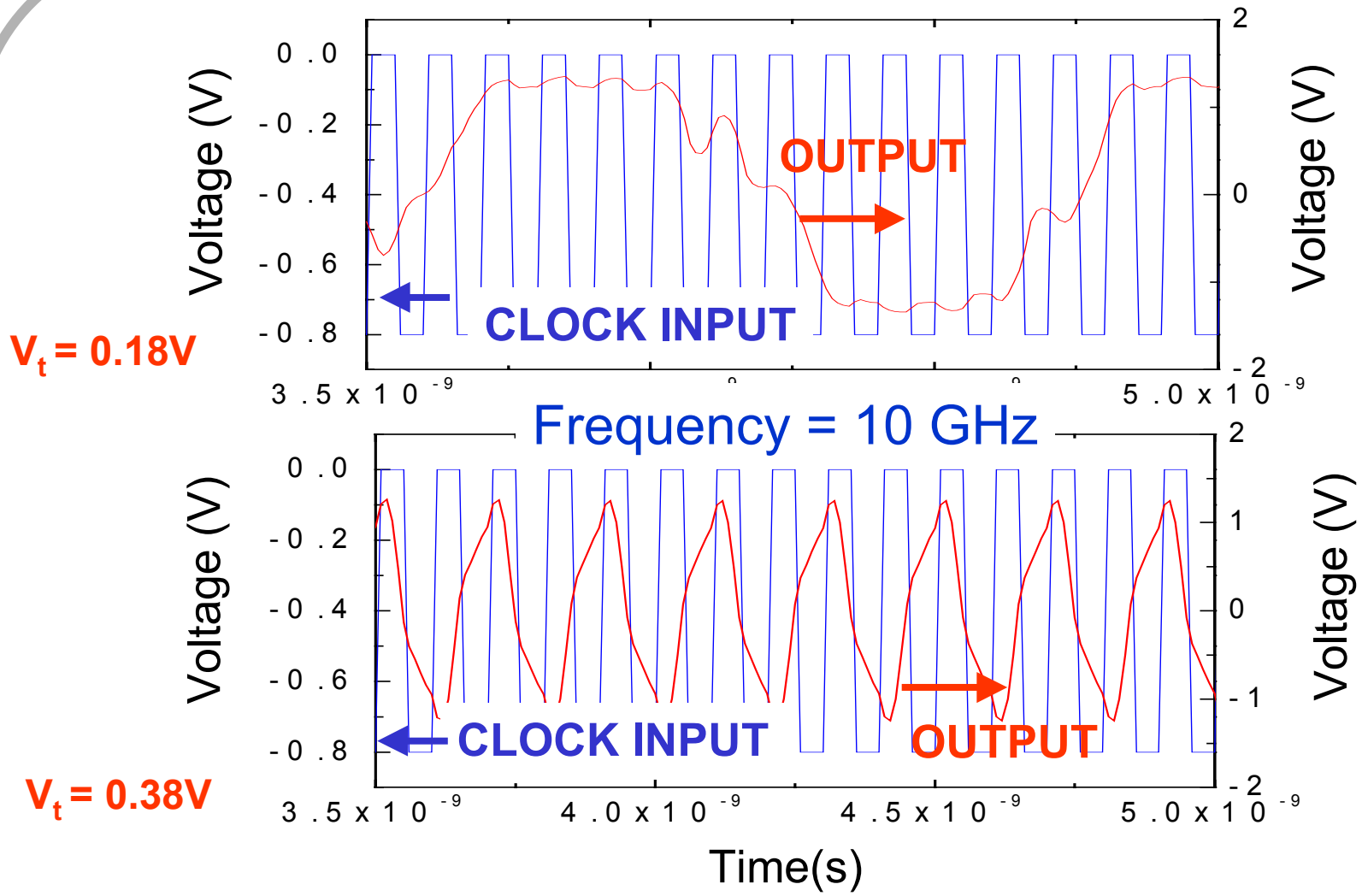
Effect of clock frequency on circuit operation

- Input frequency too high: output of the latch can't follow the input



Frequency = 10 GHz

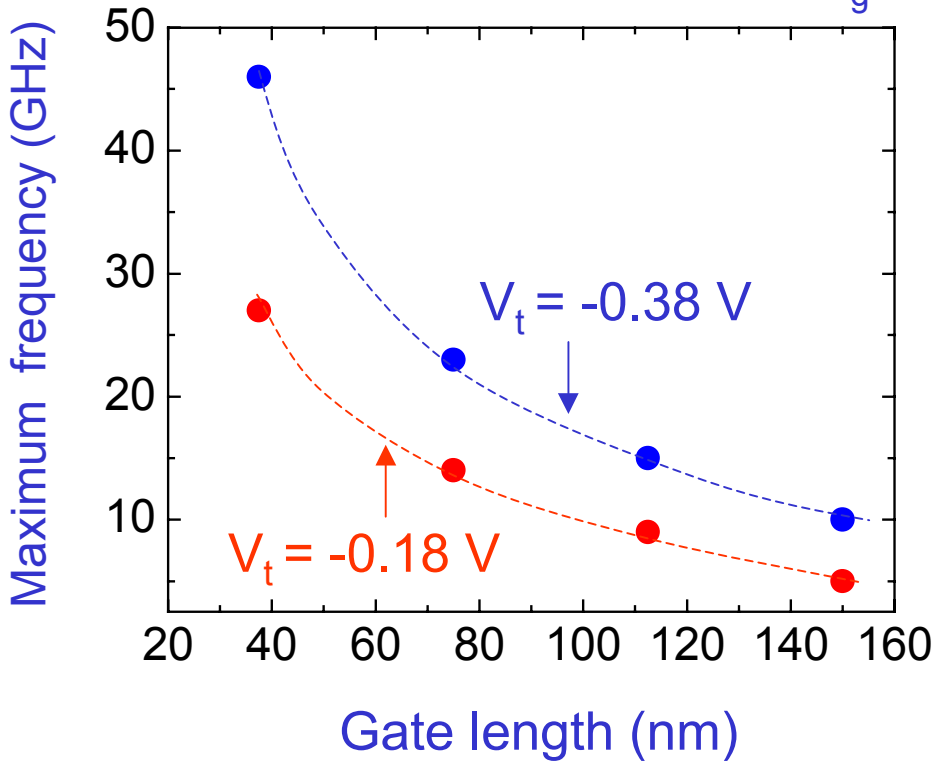
Effect of Threshold Voltage on Circuit operation



- The drive current through the active loads depend on V_t
-More "ON" the device at V_{gs}= 0, higher the drive current, faster the divider circuit

Effect of gate length on circuit operation

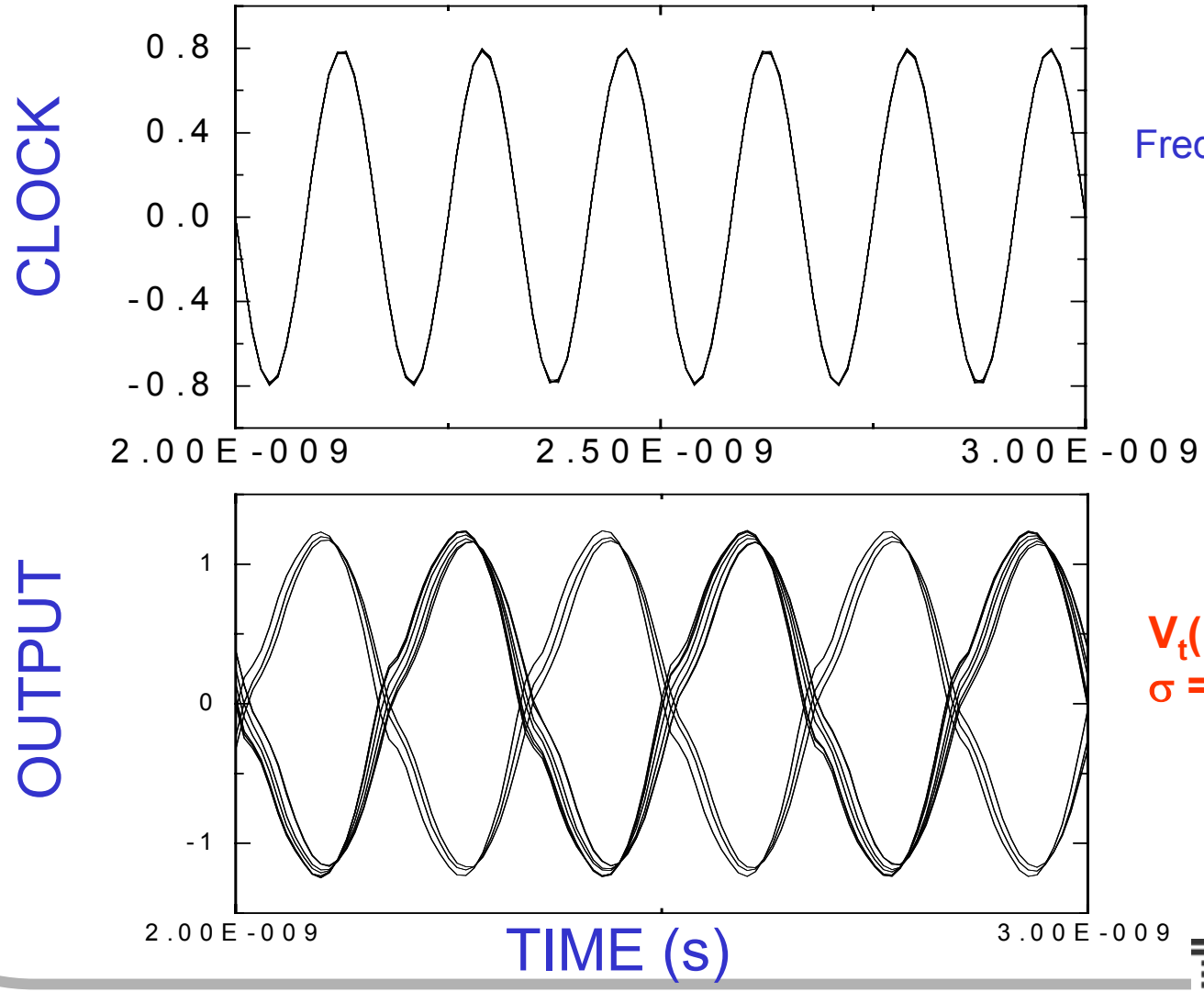
Devices fabricated in the current run have L_g = 0.15 μm



- **Scaling the gate length reduces C_{gs}**
  - Linear scaling of C_{gs} assumed. (i.e 2D effects of scaling ignored)
- **Transconductance g_m assumed constant**
  - g_m is expected to increase (sublinearly) as gate length is scaled.
  - This underestimates the max. frequency of operation

Monte carlo simulations of V_t variation on divider circuit

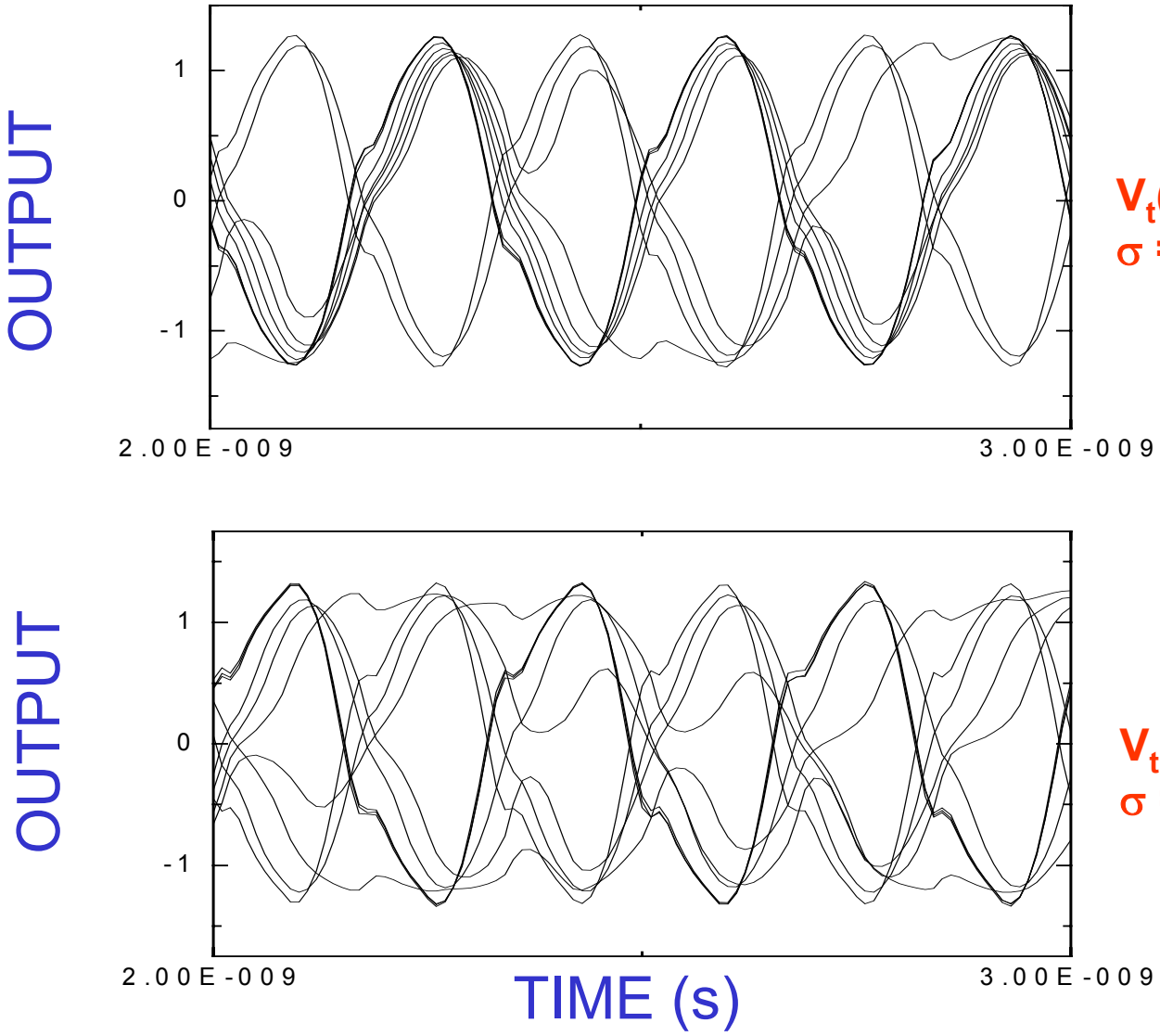
V_t is assumed to have a gaussian distribution
Random #'s are used to assign V_t's based on the distribution



Frequency = 5 GHz

V_t(mean) = 0.18
σ = 10mV

Monte carlo simulations of divider circuit



V_t(mean) = 0.18
σ = 20mV

V_t(mean) = 0.18
σ = 40mV

Tight V_t control required, σ < 20 mV to ensure circuits work

Summary

- ***p*-MODFET process developed with good yields**
  - novel DLC spacer process ensures high T-gate yield
  - Improved dual layer lift-off process prevents gate to S/D shorts
- **1st MODFET run served as a pipe cleaner**
  - several yield limiting processes identified.
  - processes with improved yields developed
- **2nd MODFET run**
  - Excellent device yield suitable for divider circuit fabrication
  - V_t(mean) = 0.18V, σ = 25mV over large area
  - AC and DC characteristics consistent with expectations based on layer structure
  - Expected completion of divider circuits 6/15/02

- **SPICE simulations**
  - DC and small signal parameter extraction for the p-MODFETs
  - Extraction of circuit diagram from CAD layout
  - Simulation of the frequency divider circuits based on the SPICE models extracted
  - Simulation of the effects of V_t variation on circuit operation