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IMPROVED HOT CARRIER AND SHORT CHANNEL PERFORMANCE IN VERTICAL NMOSFETS WITH GRADED CHANNEL DOPING

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Abstract:

Graded doping profile in the channel of vertical sub-100nm nMOSFETs was investigated in this study. Conventional single step ion implantation was used to form the asymmetric graded doping profile in the channel. No large-angle-tilt implant is needed. The device processing is compatible with conventional CMOS technology. In a graded-channel-doping device, with the higher doping near the source, drain induced barrier lowering and the off-state leakage current are reduced significantly. The graded doped channel also has a lower longitudinal electric field near the drain. Therefore, hot-carrier related reliability is improved substantially with this type of device structure.

Index terms: graded channel doping profile, vertical MOSFETs, hot carrier effects, short channel effects.

I. INTRODUCTION

There have been intensive studies in sub-100nm MOSFETs to improve the device performance and reliability [1]. The key challenge in scaling MOSFETs below the 100 nm is to maintain good short channel performance without sacrificing the drive current [2]. To reduce V_T roll-off and drain induced barrier lowering (DIBL), the channel doping has to be increased. However, higher channel doping results in lower carrier mobility and therefore lower drive current. Retro-grade channel doping [3-4] and SUPER-HALO channel doping [5-6] have been used to optimize the on-state drive current and off-state leakage current separately. The channel engineering is performed in the gate-to-channel direction in the above methods. Lateral channel engineering with graded channel doping has also been investigated, and shown improved drive current, reduced short-channel effects and reduced hot carrier effects [7-8]. In conventional planar MOSFETs, a large-angle-tilt implant has to be used to obtain asymmetric channel doping profiles. The angle is limited by the minimum feature size on the chip and gate stack height due to the shadowing effect of the gate stack. In order to make all the devices on the chip have graded channel doping, it might also need additional mask because the device on the chip may be patterned parallel and perpendicular to the wafer flat. On the other hand, vertical MOSFETs with delta-doped channel have been fabricated by MBE and showed improved performance compared to uniform doped channels [9,10]. In this study, sub-100 nm vertical nMOSFETs with graded channel doping were fabricated using *conventional* CMOS process *without* large-angle-tilt implant and sophisticated lithography. Enhanced device performance has been observed [11]. Such devices can be

used in low leakage, low power application such as DRAM, laptop computer, and wireless devices.

II. DEVICE SIMULAIONS

The MEDICI simulations [12] were used to study the device physics. All the 1-dimensional cuts of the simulation results shown in this section were made at 2 nm below the gate oxide interface.

The cross section of a vertical nMOSFET with graded channel doping is shown in Fig. 1. The channel doping profile in the simulated device with 120 nm channel length is linearly graded from $8x10^{17}$ cm^{-3} to $2x10^{18}$ cm^{-3}. The gate-to-source and gate-to-drain overlap is 10 nm. Fig. 2 shows the simulated energy potential along the channel in the "off-state" for the “normal” (higher doping level near the source) and “reverse” (higher doping level near the drain) mode. The potential barrier near the source junction is higher in the normal mode than that in the reverse mode due to the higher channel doping level near the source in the normal mode. Hence, drain induced barrier lowering (DIBL) can be reduced in the normal mode. Fig. 3 shows that in the normal mode, fewer electrons are injected from the source into the channel due to the higher barrier. Therefore, the off-state leakage current can be reduced.

Hot carrier effects are a significant reliability concern in sub-100 nm device. One most important hot carrier effect is the damage caused to the Si-SiO_2 interface, which can lead to a time-dependent degradation of device performance. The origin of all kinds of hot carrier phenomena is the large longitudinal electric field (E_{max}) near the drain end of

the channel. Electron and hole pairs are generated near the drain with the total number being exponentially dependent on the reciprocal of the E_{max}. Therefore, the greatest control over hot carrier effects is exerted by minimizing E_{max} [13]. Lightly doped drain (LDD) device structure has been widely used, in which part of the drain voltage is dropped across the lightly doped drain region in order to reduce E_{max}. The main disadvantage of the LDD device structure is the high series resistance introduced by the lightly doped drain region, which degrades the drive current [14]. Graded doping channel device can reduce the E_{max} by increasing surface potential more rapidly near the source end instead of the drain end compared to conventional devices, as it can be seen in Fig. 4. Fig. 5(a) shows the longitudinal electric field along the channel in the "on-state". The higher field in the source end results in higher drift velocity (Fig 5(b)) near the source, and the lower field in the drain end (E_{max}) reduces hot carrier effect significantly in the normal mode compared to reverse mode and the uniformly doped channel.

Near the source end of the channel, the electric field is higher in the normal mode than those in the reverse mode (Fig.5) and the uniformly doped channel. The electron injected from source into the channel will experience a rapid increase of longitudinal electric field. Therefore, the electron velocity rises rapidly at the source end of the channel. At the channel length below 100 nm, velocity overshoot takes place over a portion of the device, which is confirmed by experiment [15-16] and Monte Carlo simulations [17]. When the carrier velocity near the drain can reach rather high values in the high-field region near the drain, MOSFET currents are mainly controlled by the average velocity near the source end of the channel, and the inversion charge density $Q_i = C_{ox}(V_G-V_T)$, independent of the drain voltage[18] . Therefore, it is expected that the

graded doping channel device have enhanced drive current at very short channels when it is operated at the normal mode[19].

III. DEVICE FABRICATION

The process flow for the fabrication of graded channel doping vertical MOSFETs is shown in Fig. 6. It is compatible with a Si CMOS process and no large-angle-tilted implantation is needed. A 4 nm gate oxide was grown at 750°C for 5 min by wet oxidation. The dopants were activated by rapid thermal annealing at 950°C for 1 min. The final doping profiles in the device are obtained using secondary ion mass spectroscopy (SIMS) and shown in Fig. 7. A dip was found in the boron profile near the p-n junction. This is because the electric field resulting from the formation of p-n junction causes boron to segregate into the As-implanted region [20]. Two different heights of mesa were etched and the mesa height determines the channel length (120 nm and 80 nm).

Measured C-V curves in Fig. 8 indicate that the interface state density (D_{it}) is quite low ($< 10^{11}$ cm^{-2}). The measured gate leakage current is also very small, as shown in Fig. 9. Both measurements demonstrated that a high quality gate oxide was grown on the sidewall of the mesa in the vertical devices.

IV. RESULTS AND DISCUSSIONS

Fig. 10 shows the subthreshold characteristics of a 120 nm channel length device measured in the normal and reverse modes. At V_{DS} = 50 mV, the subthreshold swing is 100 mV/dec and threshold voltage (V_{T_lin}) is 0.45 V for both modes. At V_{DS} = 2 V, the

V_T shift due to DIBL is 100 mV/V for the reverse mode and 30 mV/V for the normal mode; and the off-state leakage current in the normal mode is two orders lower. These confirm that the short-channel effects are significantly reduced in the normal mode where the channel doping is higher near the source. Furthermore, the subthreshold swing in the reverse mode reduces from 100 mV/dec to 75 mV/dec as V_{DS} increases (V_{DS} = 50 mV to 2 V), due to the build-up of the hot carriers in the body, yet it changes only negligibly from 100 mV/dec to 92 mV/dec in the normal mode. This indicates that hot carrier effects are substantially suppressed in the normal mode.

Fig. 11 shows the substrate current versus gate voltage at a drain voltage of 3 V in the normal and the reverse mode for the 120 nm channel length device. The peak of the substrate current in the normal mode is almost one order of magnitude smaller than that in the reverse mode. This, again, suggests that fewer hot carriers and less impact ionization exist in the normal mode. Therefore, the breakdown voltage due to avalanche should be higher for the normal mode. Fig. 12 shows the output characteristics of the device before and after it is stressed at V_{DS} = 3 V and V_{GS} = 1 V for 10000 sec. The degradation of the drive current after stressing is much less in the normal mode than that in the reverse mode at higher gate bias. The maximum transconductance G_m in the linear region is degraded by 6.3% in the reverse mode while it is only degraded by 1.2% in the normal mode. Therefore, we confirm that the higher channel doping near the source can significantly reduce hot carrier effects.

Fig. 13 shows the subthreshold and output characteristics of the device with 80 nm channel length, where the short channel effects are more prominent. The linear V_T is identical (0.2 V) in the normal and reverse modes. However, the V_T shift due to DIBL is

100 mV/V smaller in the normal mode than that in the reverse mode. Competing with the charge build-up in the channel, the DIBL in the reverse mode is so significant that the substhreshold swing actually becomes worse as V_{DS} increases, unlike case for the 120 nm device. From the output characteristics, we also observe more significant kinks in the reverse mode than in the normal mode. These kinks are due to the raised body potential by hot holes.

V. CONCLUSIONS

Vertical nMOSFETs with graded channel doping profiles were studied by device simulation and fabrication. 80 nm and 120 nm devices were fabricated and characterized. No large-angle-tilt implant was needed to form the asymmetric channel doping. With a higher channel doping level in the source end, DIBL and the off-state leakage current are significantly reduced due to a higher potential barrier near the source junction. Meanwhile, with a lower channel doping level in the drain end, hot carrier effects are also reduced due to a smaller longitudinal electric field in the drain end.

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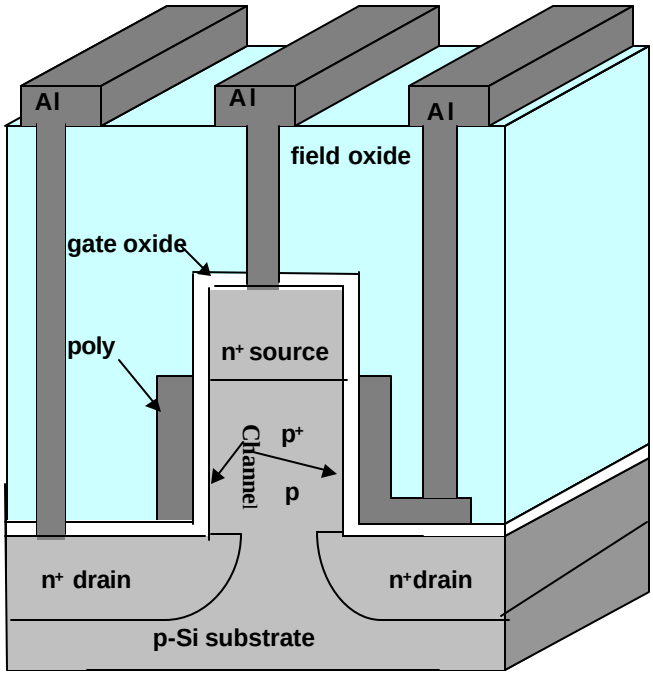


Fig. 1. Cross sectional schematic of a vertical device with graded channel doping in the "normal mode". In the "reverse mode", the source and drain contacts are interchanged.

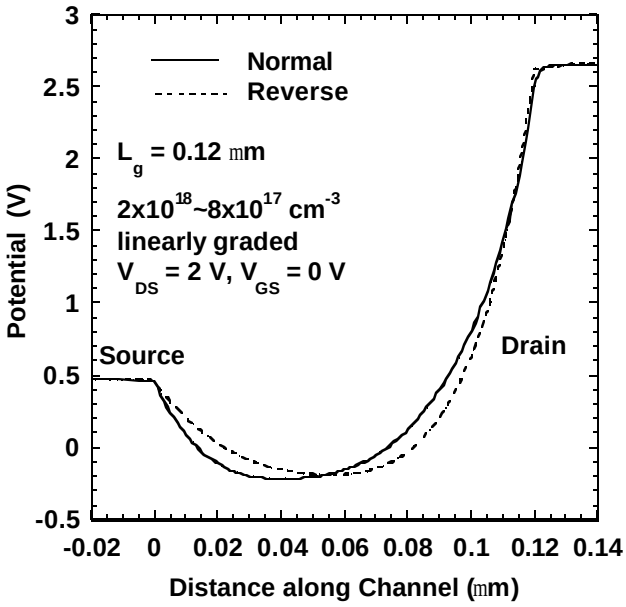


Fig. 2. Simulated energy potential profiles along the channel for the graded channel doping device in the normal and reverse mode at V_{DS} = 2V and V_{GS} = 0 V.

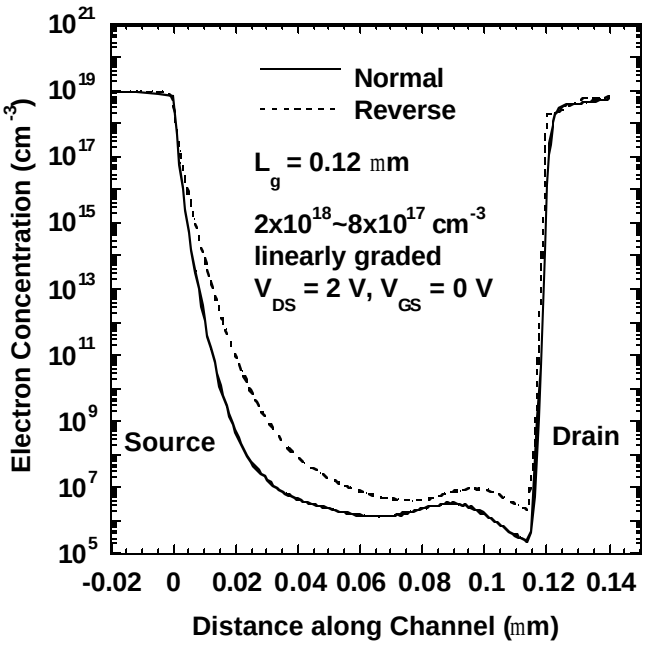


Fig. 3. Simulated electron concentration along the channel for the graded channel doping device in normal and reverse mode at V_{DS} = 2 V and V_{GS} = 0V.

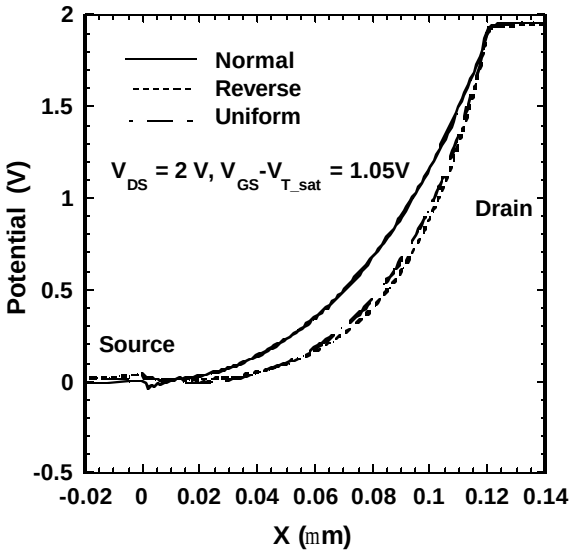
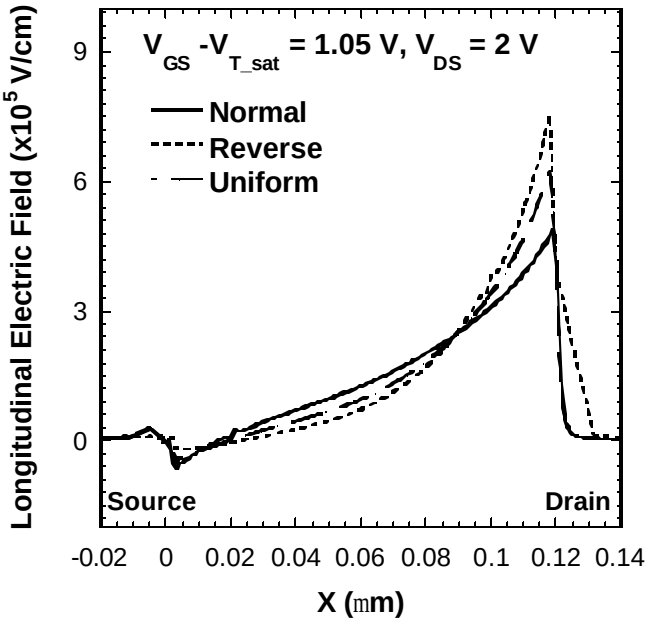
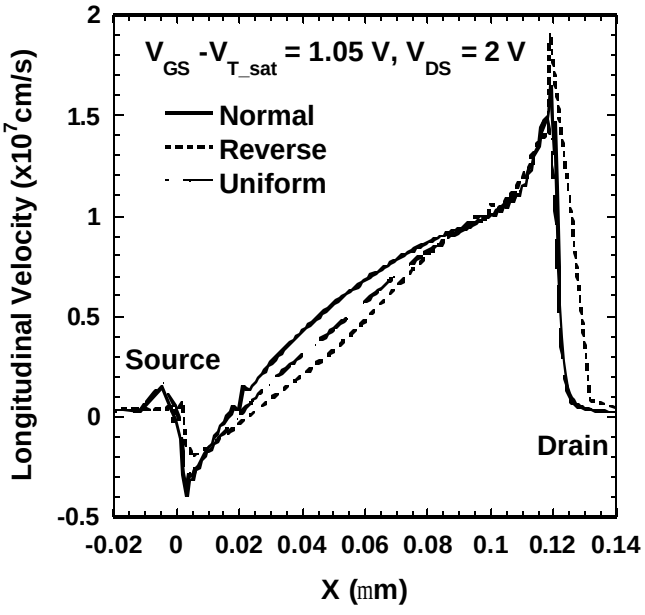


Fig. 4. Simulated energy potential profiles along the channel for graded channel doping device in the normal and reverse mode and a device with uniform channel doping at V_{DS} = 2 V, $V_{GS} - V_T$=1.05V. The doping in the uniformly doped channel device was adjusted to give the same V_{T_lin} as the graded channel doping device.

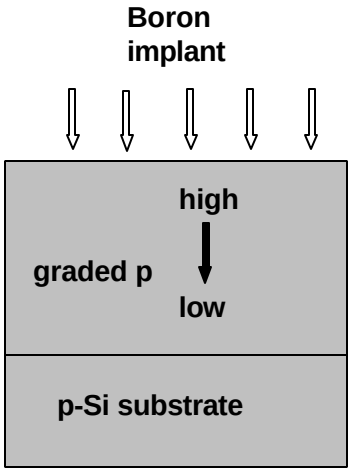


(a)

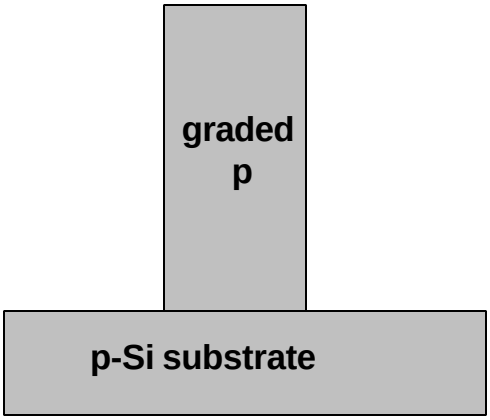


(b)

Fig. 5. Simulated longitudinal electric field along the channel for graded channel doping device in normal and reverse mode and the uniform channel doping device in the onstate.



(a)



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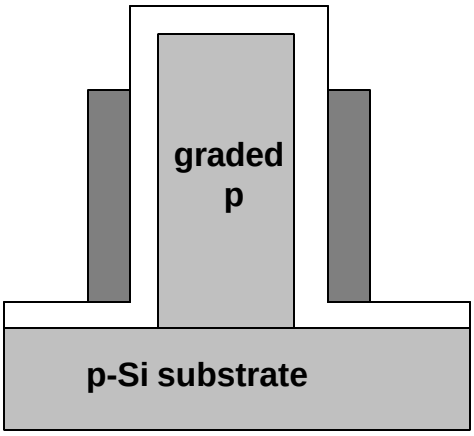
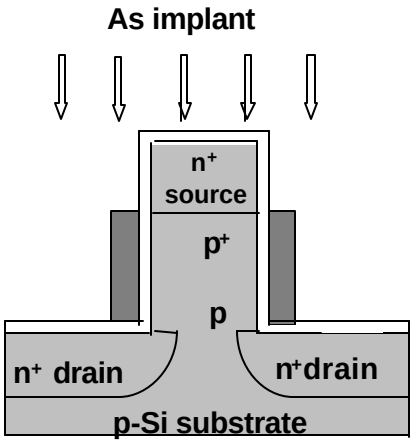
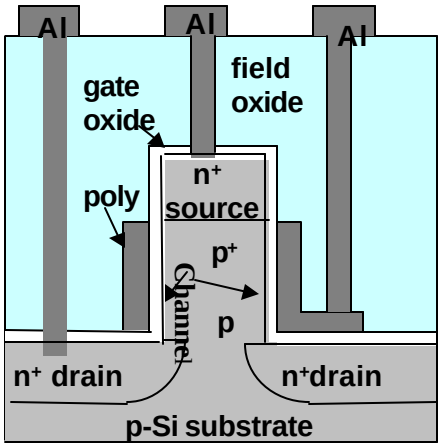


(c)



(d)



(e)

Fig. 6. Key process steps in the fabrication of graded channel doping vertical MOSFETs. (a) Boron implantation into Si substrate to form the graded channel; (b) RIE etch to form the mesa; (c) Gate oxidation on the side-wall of the mesa, poly deposition and poly etch. Poly line is extended on one side of the side-wall for contact. (d) As implantation for doping of the poly and formation of source/drain. (e) insulation oxide growth, contact opening, Al deposition and patterning.

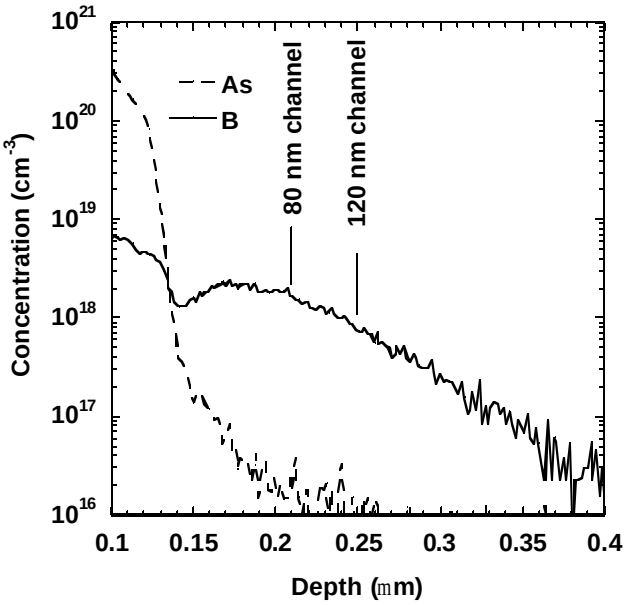


Fig. 7. SIMS profile along the channel for the graded channel doping devices. Channel 1 and Channel 2 indicate where the mesa etch stops for the 80 nm and 120 nm channel length devices, respectively.

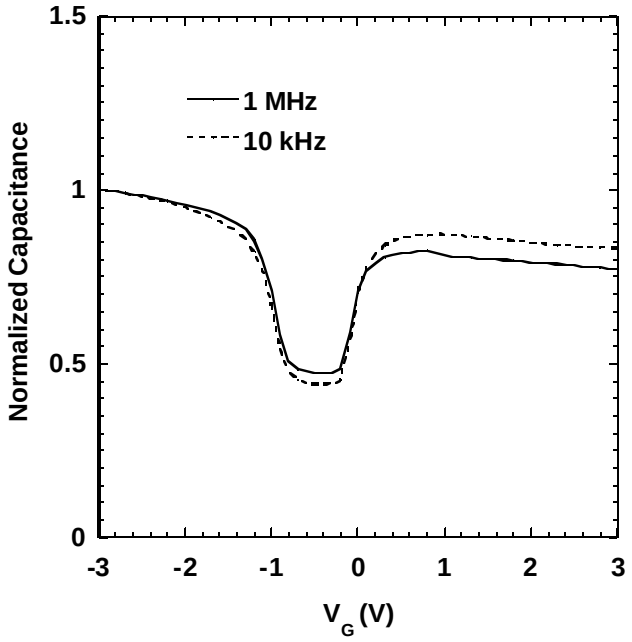


Fig. 8. Measured C-V curves of the vertical nMOSFET.

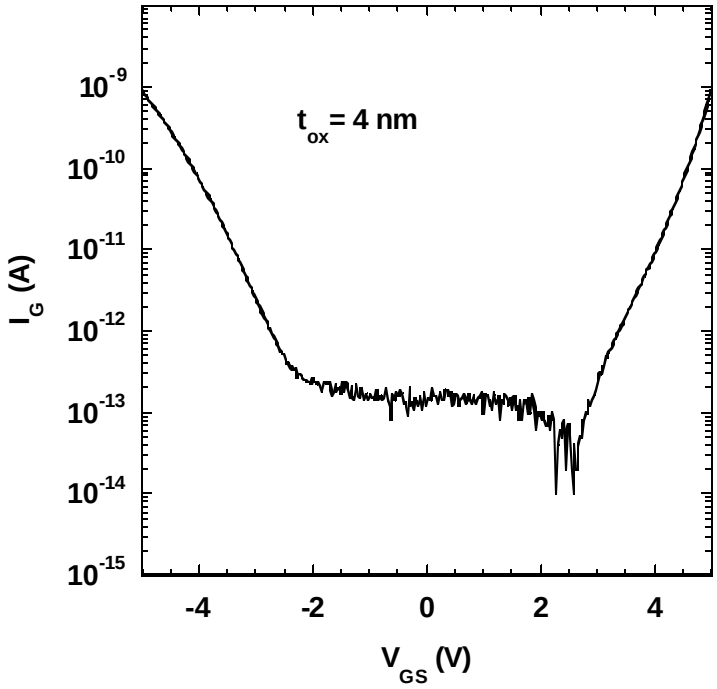


Fig. 9. Measured gate leakage current of the vertical nMOSFET.

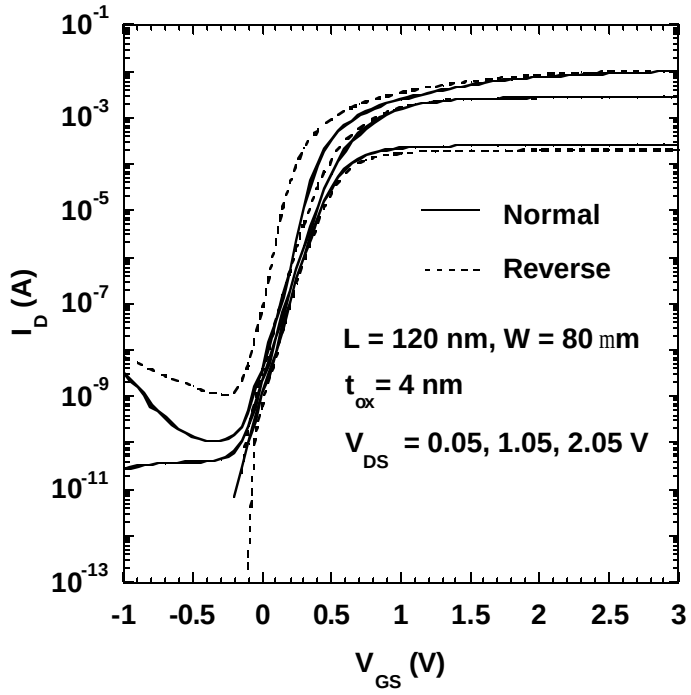


Fig. 10. Measured subthreshold characteristics for a graded channel doping device with 120 nm channel length in the normal and reverse mode.

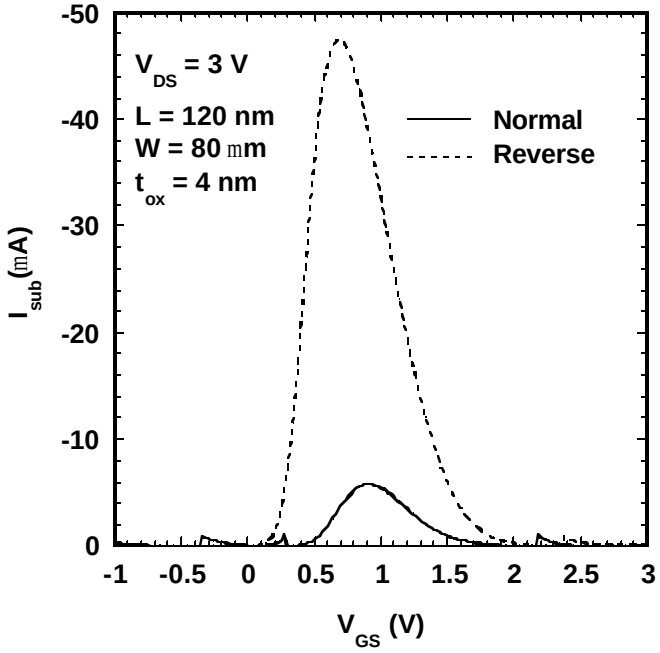
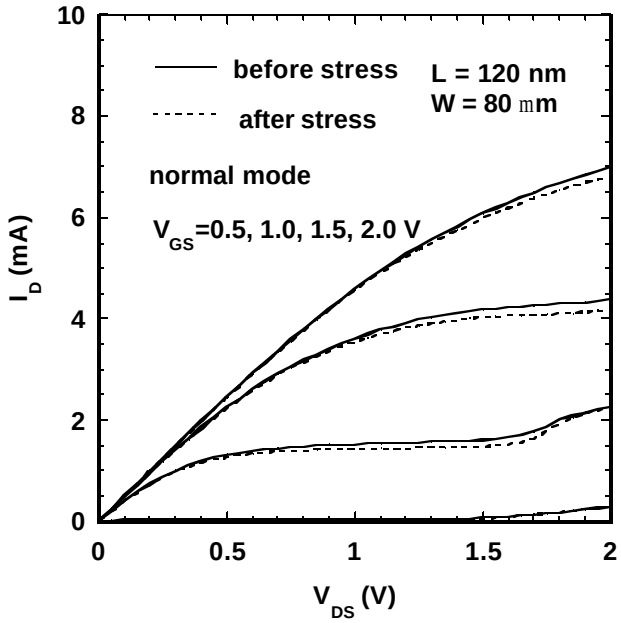
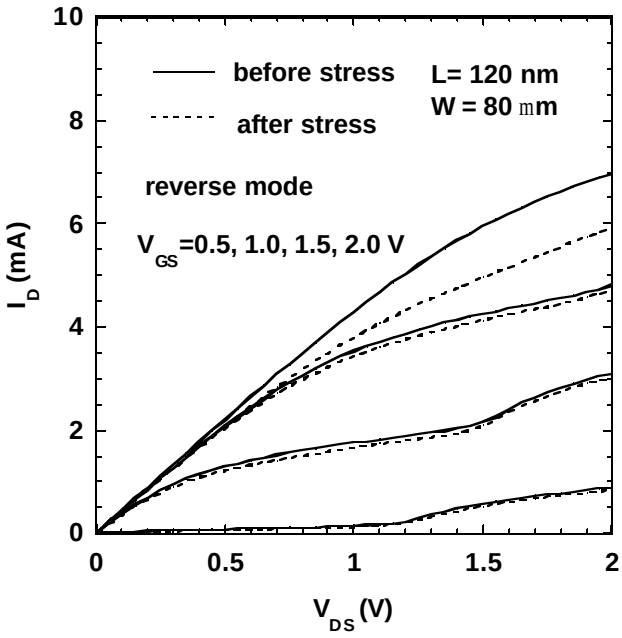


Fig. 11. Comparison of measured substrate current versus gate voltage in the normal and reverse mode for the 120 nm channel length device.

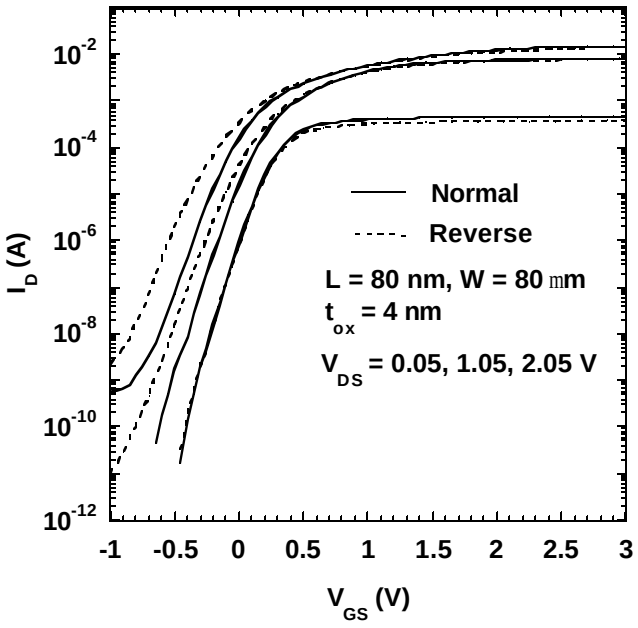


(a)

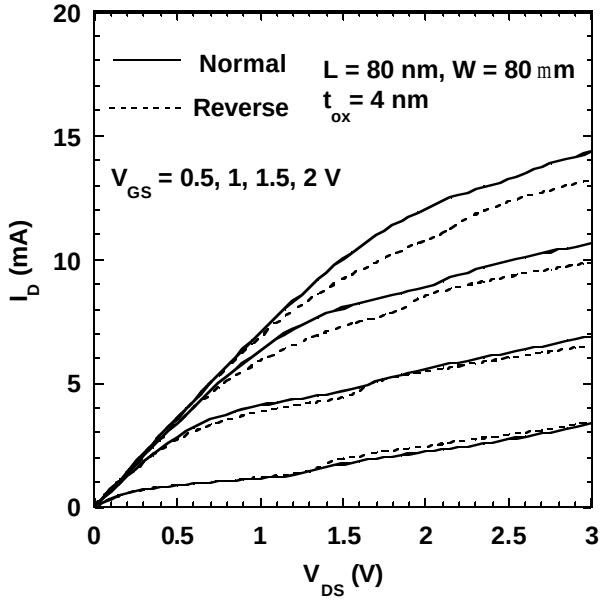


(b)

Fig. 12. Measured Output characteristics of the 120 nm device before and after stress (a) in the normal mode; (b) in the reverse mode.



(a)



(b)

Fig. 13. (a) Measured subthreshold, and (b) measured output characteristics for a graded channel doping device with 80 nm channel length measured in the normal and reverse mode.