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Ground Bounce and Ground Bounce Reduction Techniques of Power Gate Structure

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Abstract

In this paper, we address ground bounce caused by discharge current through a sleep transistor when making a power mode transition in a power gated CMOS circuit. Several ground bounce reduction techniques are proposed to reduce the magnitude of voltage glitches on the power and ground rails as well as methods to reduce the time required to stabilize power and ground. To evaluate our ground bounce reduction techniques in 0.13 um CMOS technology, we implemented arithmetic and logic units (ALUs) with a maximum frequency of 500MHz at 1.5V and simulated them with PowerSpice fixtured in a package model. The experimental simulation results demonstrate the effectiveness of the ground bounce reduction techniques.

Introduction

With the advent of Deep Sub-Micron (DSM) technology, reducing the supply voltage V_{dd} has become vital to reduce dynamic power and avoid reliability problems. Reducing V_{dd} alone, however, causes serious degradation to circuit performance. One way to maintain performance is to scale down both V_{dd} and the threshold voltage V_{th}. Reducing V_{th}, however, increases subthreshold leakage current exponentially. This problem escalates in DSM technologies. Managing leakage current has become an integral part of overall power management.

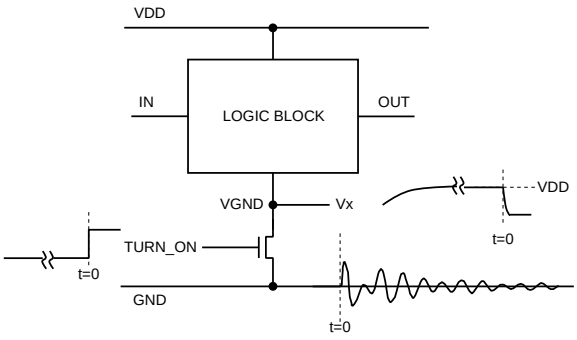


Figure 1: Basic structure of power gating circuit and ground bounce induced by its power mode transition.

The multi-threshold CMOS (MTCMOS) circuit [1] of Figure 1, including a "power gate structure", is a well documented method for reducing leakage power in the standby mode while maintaining high speed in the active mode. The logic gates of the MTCMOS circuit are implemented using low threshold voltage (LVT) transistors and are sinked to a virtual ground rail (VGND). VGND is linked to the ground rail (GND) through a high threshold voltage (HVT) transistor, called a "sleep transistor". The sleep transistor is controlled by a TURN_ON signal used for active/standby mode control.

In this paper, we address ground bounce caused by the discharge current through the sleep transistor during the power mode transition of the power gate structure and propose several ground bounce reduction techniques that reduce the magnitude of voltage variation in VDD and GND, as well as the time required to stabilize them. Our power gate structure consists of a set of sleep transistors that are sequentially turned on with the time difference ($\Delta T \neq 0$), while a conventional power gate structure is composed of a single sleep transistor or a set of sleep transistors that are turned on simultaneously without time difference($\Delta T = 0$).

We designed an arithmetic and logic unit (ALU) of a 16-bit multimedia digital signal processing (DSP) engine in 0.13 um CMOS technology. The ALU includes a multiplier, add-saturation unit, shifter-saturation unit, comparator, logic unit, and data-retention latches and operates at 500 MHz at 1.5V. To evaluate our ground bounce reduction techniques, three different configurations of the power gate structure are added to the ALU, including one conventional power gate structure, which were simulated with PowerSpice fixtured in a DIP-40 package model. Compared to the ALU whose leakage power is controlled by a conventional power gate structure, the maximum magnitude of voltage glitches in the ALUs with the modified power gate structures is reduced up to 85.5%. At the same time, the time required for VDD and GND rails to be stabilized is reduced up to 82.2%.

Behavior of Power Gate Structure

During the active mode, the sleep transistor operates in its linear region of Figure 2. The sleep transistor may be modeled as a resistor R as shown in Figure 3(a). This generates a small voltage drop V_X equal to $I_{active} \times R$, where I_{active} is the total current demand of the logic block operating in active mode. The sleep transistor is sized to minimize V_X with reasonable area consumption.

In standby mode, the sleep transistor operates in the cut-off region of Figure 2 and may be modeled as an opened switch as shown in Figure 3(b). This causes the VGND to float and so limit the leakage current to that of sleep transistor, which is very small and is proportion to the sleep transistor width. By cutting this power gate transistor off during the standby periods, however, the virtual ground rail is charged up to the VDD.

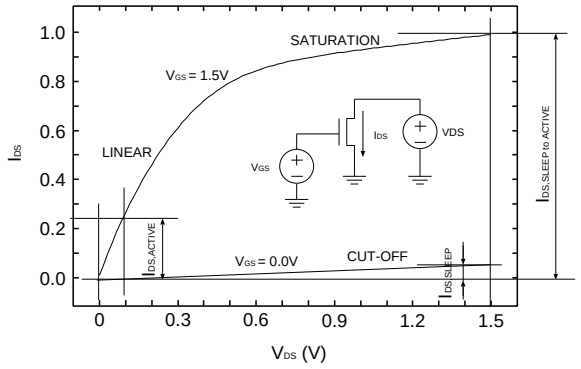


Figure 2: VI characteristics for NMOS sleep transistor.

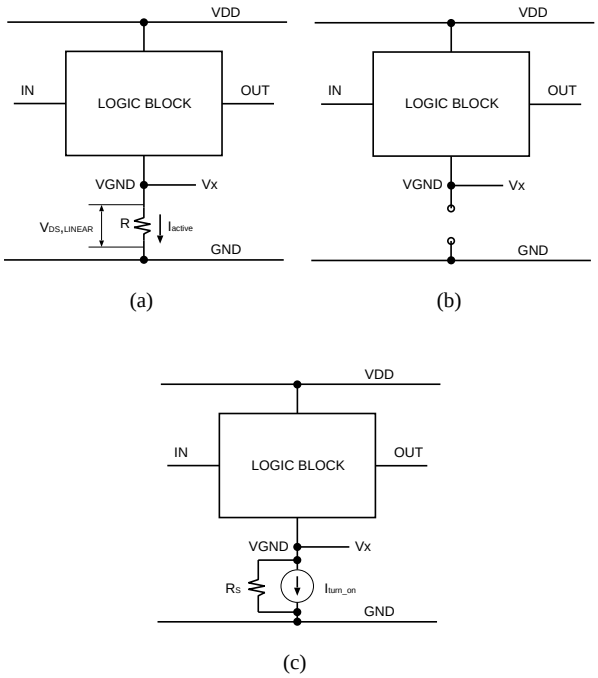


Figure 3: Sleep transistor in power gate structure modeled as (a) resistor, (b) opened switch, and (c) practical current source.

As the sleep transistor is turned on, the charge trapped in capacitive loads of logic part and virtual ground rail begins to discharge through the sleep transistor. Initially, the sleep transistor operates in the saturation region of Figure 2 and may be modeled as a practical current source as shown in Figure 3(c). The amount of current that can flow through the sleep transistor at this moment is much larger than the active mode current, I_{active}. The instantaneous current creates inductively induced voltage fluctuation in the VDD and GND rail.

Ground Bounce Caused By Power Gate Structure

Ground bounce, also known as simultaneous switching noise (SSN), is a voltage glitch induced in supply distributions due to changing currents passing through either wire/substrate inductance or package lead inductance associated with power or ground rails. These voltage glitches or surge/droop phenomena are proportional to Ldi/dt. If the magnitude of this voltage surge/droop is greater than the noise margin of a circuit, the circuit may erroneously latch the wrong value or switch at the wrong time [2].

In previous technologies, switching of input/output buffers and internal circuitry were the primary sources of ground bounce. In designs employing a power gate structure to control leakage power, however, ground bounce due to switching of the sleep transistor is a potential problem. Also, lower supply voltages reduce noise immunity and threshold voltage, which create greater noise sensitivity.

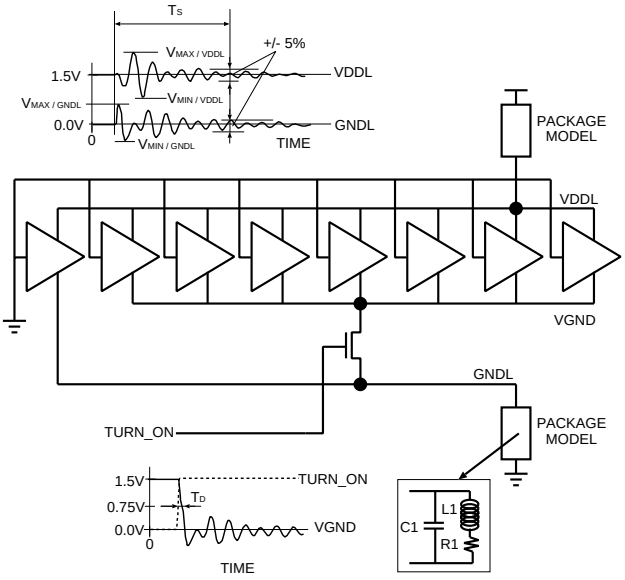


Figure 4: Simplified circuit model used to analysis of ground bounce problem induced by power-mode transition of power gate structure.

To understand ground bounce caused by the power mode transition, we propose and analyze simplified circuit models of Figure 4. Ground bounce measurement is made by turning on the sleep transistor of the power gate structure. The charge trapped in the capacitive loads and virtual ground (VGND) rail is discharged rapidly. The noise voltage waveform generated at the power supply (VDDL) and ground (GNDL) rails is measured. We define T_{D}, $I_{\mathsf{MIN/SLEEP}}$, $I_{\mathsf{MAX/SLEEP}}$, $V_{\mathsf{MIN/VDDL}}$, $V_{\mathsf{MAX/VDDL}}$, $V_{\mathsf{MIN/GNDL}}$, $V_{\mathsf{MAX/GNDL}}$, and T_{S} to characterize the ground bounce effect induced by the power mode transition of the power gate structure.

T_{D} is the time difference between 50% TURN_ON signal transition and 50% VGND level. $I_{\mathsf{MIN/SLEEP}}$ and $I_{\mathsf{MAX/SLEEP}}$ are the maximum and minimum current to flow through sleep transistor, respectively. $V_{\mathsf{MIN/VDDL}}$ and $V_{\mathsf{MAX/VDDL}}$ are the maximum and minimum level of voltage glitches on power supply (VDDL) rail, respectively. $V_{\mathsf{MIN/GNDL}}$ and $V_{\mathsf{MAX/GNDL}}$ are the maximum and minimum level of voltage glitches on ground (GNDL) rail, respectively. T_{S} is the time required for power supply (VDDL) and ground (GNDL) rails to be stabilized within $\pm$ 5% of VDD.

The circuit behavior may be described qualitatively by comparing transistor current expected in the conventional implementation to the current expected when sleep transistors are turned on sequentially. Figure 5 plots drain currents for four transistors of sizes S, $\frac{3}{4}$S, $\frac{1}{2}$S, and $\frac{1}{4}$S.

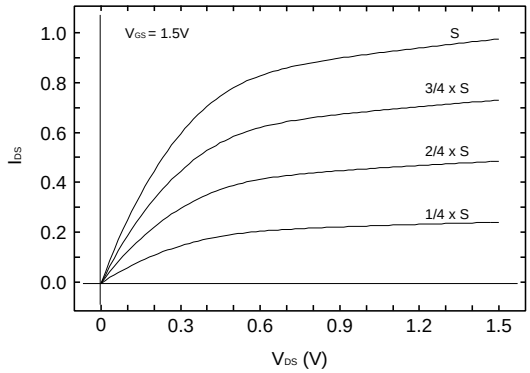
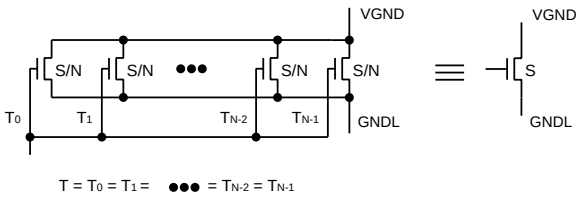
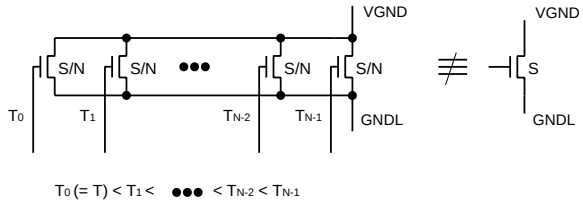


Figure 5: VI characteristics for NMOS transistor, as a function of transistor size, when V_{GS} = 1.5.

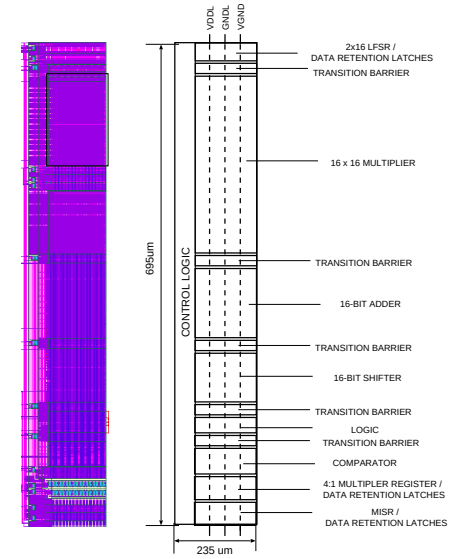


(a)

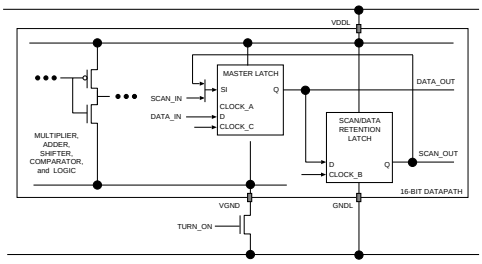


(b)

Figure 6: (a) conventional power gate structure and (b) newly proposed power gate structure.



(a)



(b)

Figure 7: Block diagram to show the connection among the logic part of 16-bit ALU, data-retention latches, and power gate structure.

Figure 6 (a) shows a conventional sleep device implementation, for which instantaneous turn on current would approach the value of the S sized device at 1.5V. Figure 6 (b) shows an implementation of our newly proposed power gate structure in which a number of sleep transistors are turned on sequentially. For $N = 4$, current at T_0 may only approach the value of the $\frac{1}{4}$S device at 1.5V, and maximum current is controlled by setting the delay between T_X and T_{X+1} so that V_{DS} is significantly reduced by time T_N.

Simulation Results

Figure 7 shows the layout and block diagram of the 16-bit fixed-point ALU of the multimedia DSP engine. The ALU includes a 16-bit × 16-bit multiplier, an add-subtract unit, a shift-saturation unit, a comparator, and a logic unit. To save and restore the state of latches during the power-down mode of the power gate structure, data-retention latches, as proposed in [3], are used in the datapath. During the power-down mode, the data-retention latch stores the state of the datapath in the SCAN/RETENTION latch of Figure 7 (b). Its VDD and GND pins are connected to VDDL and GNDL rails respectively.

Figure 8 shows a block diagrams of 16-bit ALUs whose leakage power is controlled by a conventional power gate structure. Even though it is composed of a set of sleep transistors, these share the TURN_ON signal and there is no delay between turn-on time of each sleep transistor. Therefore, behavior is equivalent to a single sleep transistor. Figure 9 show block diagrams of 16-bit ALUs with our proposed power gate structures which are composed of a set of sleep transistors. The turn-on time of each sleep transistor is controlled by (a) serially connected minimum size buffer and (b) 3-bit shift register, respectively. These ALUs were simulated with PowerSpice fixtured in a DIP-40 package model whose $R1$, $L1$, and $C1$ are 0.217 Ω, 8.17nH, and 5.32pF, respectively.

Figure 10 show the ground bounce waveform of VGND and sleep transistor TURN_ON signal, the inductive current that flows through inductive element of ground rail side, and the ground bounce waveform of VDDL and GNDL rails for ALUs with different power gate configuration.

Figure 11 shows the ground bounce effect comparison among the ALUs with a conventional power gate structure of

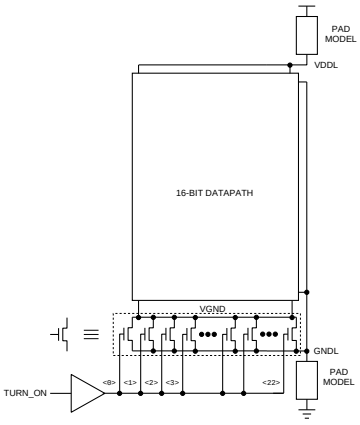
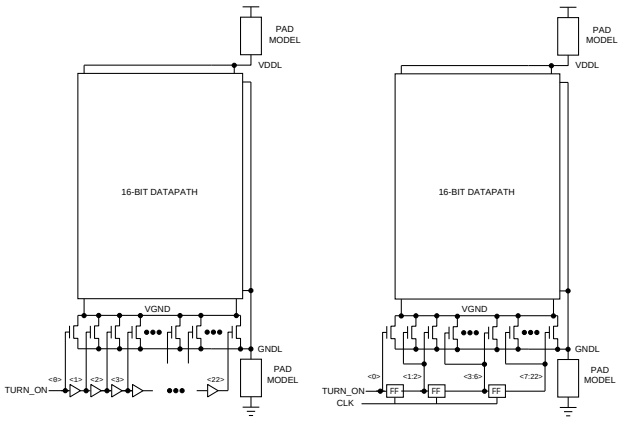


Figure 8: A block diagram of 16-bit ALU whose leakage power controlled by a conventional power gate structure.



(a) (b)

Figure 9: Block diagrams of 16-bit ALUs with our proposed power gate structures.

Figure 8 and our proposed power gate structures of Figure 9 (a) and (b), in terms of propagation delay between TURN_ON and VGND node, the maximum and minimum voltages of VDDL and GNDL rails, and the time required for VDDL and GNDL rails to be stabilized. The simulation results show that the proposed power gate structure has smaller voltage glitches at the power supply and ground rails and faster power supply and ground rail stabilization times.

Conclusions

In this paper, ground bounce caused by discharge current through a sleep transistor during the power-mode transition of the power gate structure was discussed. Several ground bounce reduction techniques were proposed to reduce the magnitude of voltage glitches in the VDD and GND rails as well as the time required for these rails to stabilize. We propose an evaluation setup of ground bounce caused by the power-mode transition of power gate structure. To demonstrate the effectiveness of our ground bounce reduction techniques in 0.13 um CMOS technology, we implemented arithmetic and logic units (ALUs) operated at a maximum frequency of 500MHz with the

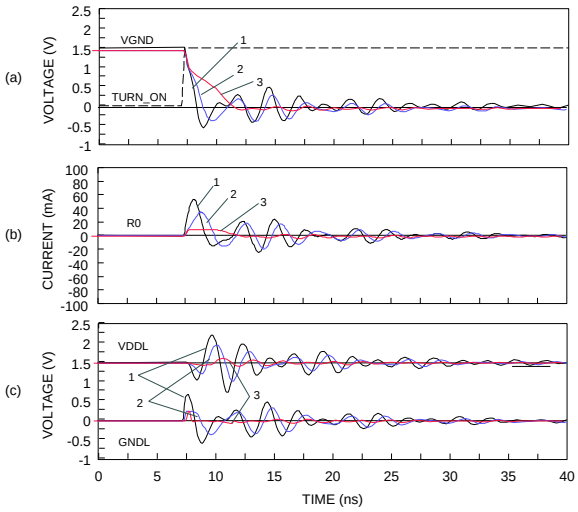


Figure 10: Waveforms of (a) VGND and TURN_ON, (b) inductive current, and (c) voltage glitches on VDDL and GNDL rails (1: Figure 8, 2: Figure 9 (a) and 3: Figure 9 (b)).

	Figure 8	Figure 9 (a)	Figure 9 (b)
T_D	0.645 ns	1.052 ns	1.754 ns
$\{I_{MIN/\ R0},\ I_{MAX/\ R0}\}$	{-24.37mA, 53.72mA}	{-19.301mA, 34.757mA}	{-3.331mA, 10.708mA}
$\{V_{MIN\ /\ VDDL},\ V_{MAX\ /\ VDDL}\}$	{0.770V, 2.208V}	{1.042V, 1.961V}	{1.420V, 1.614V}
$\{V_{MIN/\ GNDL},\ V_{MAX/\ GNDL}\}$	{-0.578V, 0.684V}	{-0.344V, 0.339V}	{-0.067V, 0.267V}
T_S	29.885 ns	22.410 ns	5.628 ns

Figure 11: Ground bounce comparison among ALUs of Figure 8, Figure 9 (a) and Figure 9 (b).

supply voltage of 1.5V and simulated them in PowerSpice with a package model. In comparison with the ALU whose leakage power is controlled by a conventional power gate structure, the maximum magnitude of the voltage glitches of the ALUs with our power gate structures is reduced by up to 85.5%. At the same time, the time required for VDD and GND rails to be stabilized is reduced by up to 82.2%. The same concept may be used for PMOS or PMOS/NMOS based sleep transistor implementations.

References

[1] S. Mutoh, T. Douseki, Y. Matsuya, T. Aoki, S. Shigematsu, and J. Yamda, "1-V power supply high-speed digital circuit technology with multithreshold-voltage CMOS," *IEEE Journal of Sold-State Circuits*, vol. SC-30, pp. 847–854, Aug. 1995.

[2] Y. Chang, S. K. Gupta, and M. A. Breuer, "Analysis of ground bounce in deep sub-micron circuits," in *Proceedings of 15th IEEE VLSI Test Symposium*, pp. 110–116, 1997.

[3] V. Zyuban and S. V. Kosonocky, "Low power integrated scan-retention mechanism," in *Proceedings of International Symposium on Low-Power Electronics and Design*, pp. 98–102, Aug. 2002.