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OXIDE BREAKDOWN MODEL AND ITS IMPACT ON SRAM CELL FUNCTIONALITY

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Abstract

It has been argued that oxide breakdown (BD) may limit CMOS scaling [1], but its impact on circuit functionality is not clear. Oxide reliability models assume that a single BD on a chip will cause circuit failure, but even hard breakdown (HBD) does not cause complete failure of some circuits [2].
The circuit chosen for this investigation includes an SRAM cell, the bit select and the sense amplifier circuit (Fig. 1.a). In this paper, we have only concentrated on the cell results because of the limited abstract extension but a similar analysis has been done on the other blocks. SRAM cell (Fig. 2) is a generic circuit (compared to custom logic), and cache memory occupies more than 40% of the chip area. Therefore, by demonstrating that SRAM arrays are relatively insensitive to gate oxide BD, we may realize a significant reliability margin for some chips. The technology of the cells used in this work was 0.13μm/1.2V partially depleted SOI technology [3]. Cell transfer ratios (width ratio of *n*-fet/pass-gate) are chosen to achieve stable cell operation. For SOI technology, it is necessary to consider that increased gate-body current will affect dynamic operation [4]. Regarding to this consideration, in this work we have analyzed for the first time SOI technology taken into account both the gate to body tunneling and the floating body effects. Only gate-to-diffusion (source or drain) breakdown was considered, since these represent the worst-case situations. Breakdown to the channel can be modeled as a superposition of two gate-diffusion events. Oxide HBD provokes ohmic conduction (I=(1/R)V) through the oxide, and was modeled with simple resistors (value ranging from 10 KΩ to 500 KΩ) between gate and drain or gate and source of the transistors of the cell (inset b in Figure 1). We have used the bitline differential voltage (which is the difference between two bitline voltages developed when the cell is accessed) and the read and write delays of the cell to evaluate the effect of the HBD on the cell performance. For comparison, the static noise margin (SNM) was also obtained to quantify cell stability [5,6] in the presence of BD at various locations in the cell. The SNM was used to compare the effect of HBD on cell performance with the previous results, although SNM may not be a direct measurement of the BD effect due to the dynamic variation of the beta ratio of the cell and pass transistors.
There are only three topologically distinct breakdown locations in an SRAM cell, denoted drain, *p*-source, and *n*-source in Fig. 2. Figure 3 shows that the bitline differential voltage, when the cell is in opposite state, seems not to be affected by the n-source oxide HBD. However, in the quiescent state, bitline differential voltage decreases as the conduction through the oxide increases. For HBD resistance about 25KΩ the bitline differential voltage changes in sign, that means a change in the stored value of the cell. This dependence of read success on BD strength correlates well with the SNM results shown in Figure 4. This figure shows the SNM when the cell is in half selected state (word line is pulled high while the bitlines are pre-charged high before the "read" operation), normalized to the SNM of the cell without BD. For the cells considered in this paper, a 50% degradation in SNM results from oxide BD when the current through the BD spot reaches ~20-30μA at V_{dd} for the worst-case *n*-source breakdown. Pass-gate or *p*-source breakdown may tolerate higher leakage. Figure 5 shows the impact of oxide HBD on the read delay of the stored value of the cell. As the HBD conduction through the oxide becomes higher, the read delay increases and an abrupt change on it is observed for HBD resistance about 25KΩ. On the other hand, the dependence of the SRAM write delay on oxide HBD shown in Fig. 6 indicates that the write delay decreases as the oxide HBD increases. For HBD resistance values below 30 KΩ the write process of the cell is completely damaged. In conclusion, this technique is effectively used to model the oxide HBD impact on circuit functionality and the results give targets for tolerable values of leakage in the SRAM cell caused by gate oxide breakdown.

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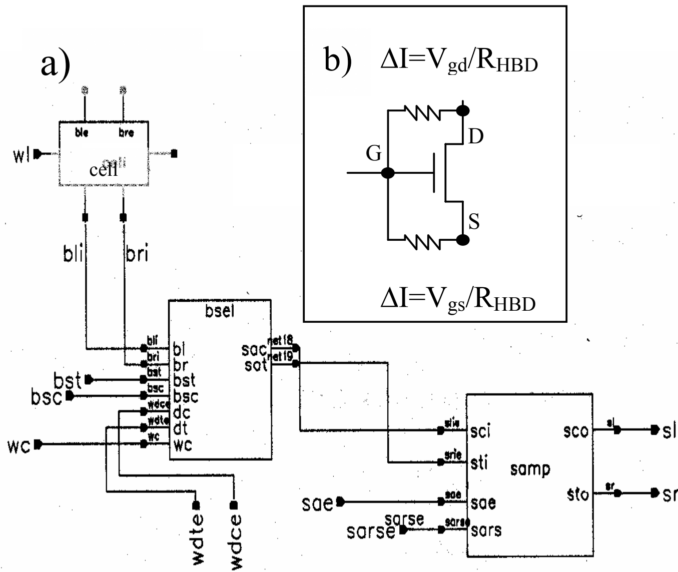

Figure 1: a): Circuit used to analyze the effect of HBD on circuit performance which includes the SRAM cell, bit select circuit and sense amplifier. b): Circuit to model the oxide hard breakdown (HBD) leakage current from gate to drain or from gate to source in a transistor.

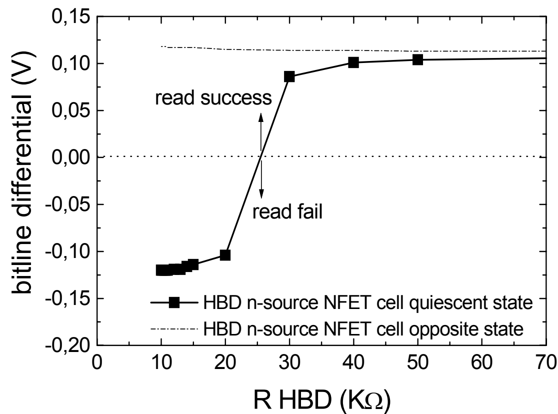

Figure 3: Bitline differential voltage of the SRAM cell in quiescent and opposite state (measured at 50% point of sense amp enable signal), with n-source BD (ohmic) in cell.

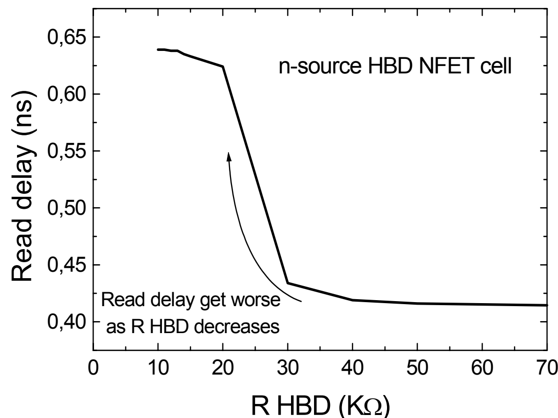

Figure 5: Read delay of the SRAM cell as a function of n-source HBD. The read delay was measured between the 50% point of the world line signal and the left sense amplifier output during a read operation.

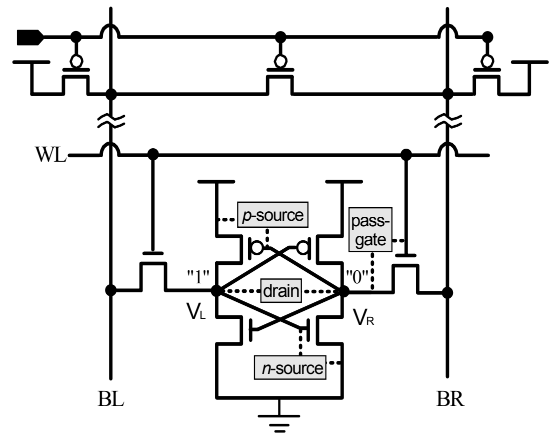

Figure 2: 6-T SRAM cell with possible BD leakage paths corresponding to the cell state shown.

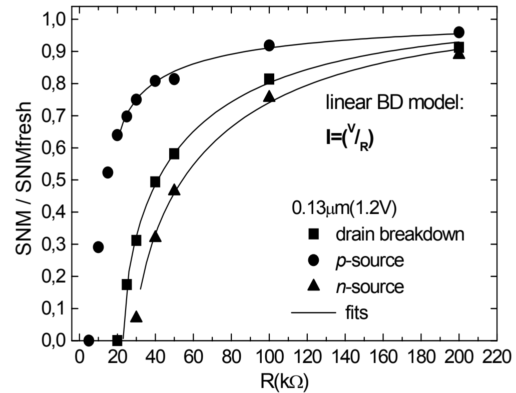

Figure 4: Normalized SNM for HBD as a function of ohmic breakdown resistance R at various locations in the cell.

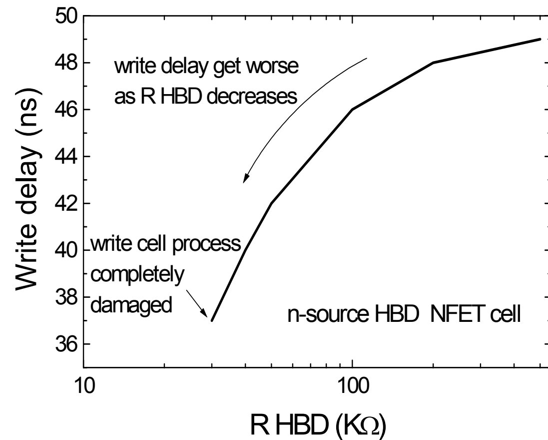

Figure 6: Write delay of the SRAM cell as a function of n-source HBD. The write delay was measured between the 50% point of the right bitline signal and the value stored in the left node of the cell during a write operation.