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Universal Tunneling Behavior in Technologically Relevant PN Junction Diodes

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a: Abstract

Band-to-band tunneling was studied in ion-implanted PN junction diodes with profiles representative of present and future silicon CMOS transistors. Measurements were done over a wide range of temperatures and implant parameters. Profile parameters were derived from analysis of CV characteristics, and compared to SIMS analysis. When tunneling current was plotted against effective tunneling distance (tunneling distance corrected for band curvature) a quasi-universal exponential reduction of tunneling current vs., tunneling distance was found with an attenuation length of 0.38nm, corresponding to a tunneling effective mass of $0.29m_0$, and an extrapolated tunneling current at zero tunnel distance of $5.3x10^7$ A/cm^2 at 300K. These results are directly applicable for predicting drain to substrate currents in CMOS transistors on bulk silicon, and body currents in CMOS transistors in silicon-on-insulator.

A: Introduction

Band-to-band tunneling presents a limit to scaling of future CMOS devices [1], both in bulk CMOS, where a heavily doped PN junction exists between the drain of the transistor and the substrate, and in partially-depleted silicon-on-insulator CMOS [2], between the drain and the partially-depleted silicon body. The problem is exacerbated because very heavy counter-doping (the halo [1]) in the vicinity of the source or drain is used to suppress short-channel effects. In the design of Taur *et al.* [1] a halo doping of close to 10^{19}cm^{-3} was used, and this doping is predicted to scale as the square of the dimensions [3] to maintain proportionately smaller depletion layer widths as dimensions shrink and voltages remain constant. The tunneling leakage in the heavily doped junction is a cause for increased power dissipation in the bulk FET, whereas in the partially-depleted SOI case it can cause unwanted threshold voltage shifts leading to extra sub-threshold drain-to-source leakage. This tunneling sets a limit to the minimum gate length of the FET subject to a constraint on standby power [4] and could determine the choice between a bulk-silicon technology, or the more difficult partially or fully depleted SOI technologies, so being able to accurately predict these currents is of considerable importance.

In contrast to the urgent requirements for evaluation of scaled CMOS, band-to-band existing tunneling data is very sparse. Most of it is out-of-date, hard to interpret, and inapplicable to the types of profiles and voltages found in modern FETs. For instance much of the older data [5-7] is on (111) silicon, other data is exclusively in the forward direction [6,8,9] while we choose the reverse direction because it is the worst case for high leakage currents. We do not attempt to study tunneling in FET structures, as in [10,11,12], since the field geometry in an FET is complex and we are interested first is establishing the tunneling parameters using simpler geometries. The work of Stork and Isaac [13], is relevant to our study, although doping values used there only overlap our study at the higher end of their data and the lower end of ours. That study was used by Taur *et al.* [1] to establish a current density vs. electric field relationship, but in fact it is difficult to extract such a relationship unambiguously from this data. The work of Hurkx *et al.* [14] has sufficient documentation to provide a valuable complement to out data.

In silicon, tunneling theory is messy because of the indirect and complex band-structure, leading to many competing tunneling paths which are difficult to quantify. The motivation for this work therefore is not so much to verify basic tunneling theory, which has been amply done before, in simpler systems, but to establish a data-base of empirical information which will be directly useful in evaluating scaling trends, as well as indirectly in the evaluation of numerical models for device simulation. While our empirical approach is acknowledged, tunneling theory will be used as a framework to attempt to unify the data and to seek universal behavior. The literature is split on the issue of universality with some early data giving it support [6,7], much of the later data [10,11,13-15] has focussed on trap-assisted tunneling, which, being process dependent, is not expressible in universal form even though intrinsic behavior may be present as well [13-15]. While some of our data shows trap-assisted type behavior, we will show that a large subset does indeed exhibit universal characteristics and is therefore suitable for quantifying the limits of devices. It is to be noted that our study was restricted to (100) silicon, and that tun-

neling paths may be in other directions inside of an FET, therefore future study on other orientations is warranted.

B: Theoretical Methods

a: Effective Tunneling Distance

The tunneling distance is the most important parameter for unifying I-V data in the band-to-band tunneling regime, over a wide range of sample types, doping, temperature and voltage. This is because tunneling depends exponentially on the tunneling distance i.e the shortest equi-energy path between conduction and valence bands, give or take an acoustic zone-edge phonon (~17meV for TA phonon in Si [16]). It also depends exponentially on bandgap, but bandgap is not strongly dependent on the experimental variables. A schematic diagram of the tunneling situation is shown in Fig. 1. The phonon-assisted models of Keldysh [17], Price and Radcliffe [18] and Kane [19] are applicable (see Fig. 1b), where an electrons and a hole tunnel in from the valence and conduction-bands respectively, combining near mid-gap, for comparable masses, with the aid of a phonon. To the degree of approximation of our analysis we assume equal electron and hole masses (c.f. light electron and hole masses of 0.19 and 0.16 m_0 respectively [16]), and we neglect the phonon energy which is small compared to the bandgap.

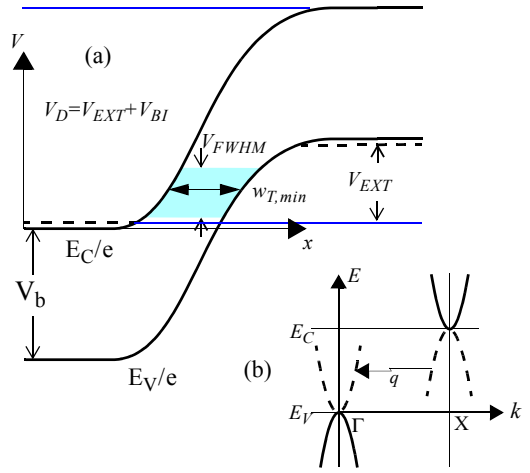

Fig. 1. Schematic band diagram of a P-N junction under reverse bias, (a) and energy-momentum picture for indirect tunneling (b) where V is the internal potential, V_{EXT} the external voltage, V_{BI} the built-in voltage, V_D the potential across the junction, and V_b the bandgap potential. E_C and E_V are the conduction and valence band edges, Γ and X are crystal momenta, and q is the phonon momentum. The minimum tunneling distance is $w_{T,min}$ and V_{FWHM} is the width of the energy distribution of the tunneling current.

The internal potential $V(x)$ is derived from the profile $N(x)$ using the depletion approximation:

$$V(x) = \frac{e}{\varepsilon}\int_{x_1}^{x}(u-x)N(u)du\ , \qquad (1)$$

coupled with the charge neutrality condition:

$\int_{x_1}^{x_2}N(u)du = 0$, where x_1 and x_2 are the near and far-side depletion layer edges, e is the electronic charge, and ε is the permittivity of silicon. The additional condition:

$$V(x_2) = V_{EXT} + V_{BI}\ , \qquad (2)$$

where V_{EXT} and V_{BI} are the external (applied) and built-in voltages respectively, allows the system to be solved. The tunnel distance, $w_T = x_V - x_C$, corresponding to an internal potential V_I is found by solving for the conduction and valence-band intercepts, x_V and x_C, i.e. $V(x_C)=V_I$, and $V(x_V)=V_I+V_b$, where V_b is the bandgap potential of silicon (E_G/e). Furthermore, by assuming, in advance an exponential dependence of tunnel current on tunnel distance, ($\propto \exp[-w_T/\lambda_T]$), we obtain a full-width-half-maximum spread, V_{FWHM}, of the tunnel current distribution in energy (see Fig. 1), and the average tunnel distance $\langle w_T \rangle$. The tunnel decay length, λ_T, for the purposes of averaging, is chosen to be consistent with the, to be determined, dependence of the current density on tunnel distance (~0.5nm). This process in iterative but in practice the averaging process depends rather weakly on the *a priori* assumed λ_T.

Rather than just the tunneling distance, it is actually the action-integral, in the WKB approximation, which determines the tunneling current. Denoting this integral by φ, the tunneling probability is proportional to $e^{-2\varphi}$ (square of the tunneling amplitude). For our phonon-assisted process the tunneling path is split into the electron part ($x_C \le x < x_p$) and the hole part ($x_p \le x \le x_V$) where x_p is the most probable co-ordinate for the phonon transition, which is taken to be the mid-gap point, for equal electron and hole masses. Using the WKB approximation [5]:

$$\varphi = \frac{1}{\hbar}\left\{\int_{x_C}^{x_p}\sqrt{2m_e e[V(x)-V_I]}dx + \int_{x_p}^{x_V}\sqrt{2m_h[V_b+V_I-V(x)]}dx\right\}\ , \qquad (3)$$

where m_e and m_h are the electron and hole effective masses (assumed to be equal here), and $\hbar$ is the reduced Planck's constant. Denoting φ_F for the case where the field is uniform ($V(x) = Fx$), $\varphi_F = (2/3\hbar)\sqrt{emV_b}\, w_T$, where w_T is as defined above. For curved bands, as in Fig. 1, $\varphi < \varphi_F$, for the same w_T, and we compensate for this by plotting our data against an effective tunneling distance w_{TE}, where $w_{TE} = w_T \varphi/\varphi_F$. We call the factor φ/φ_F the *curvature* correction. To simplify calculations the curvature correction is evaluated only at the V_I corresponding to the maximum tunneling probability.

The mean effective mass for tunneling, m, may now be derived from the slope of the $\ln J$ vs. w_{TE} plot,

$$m = \frac{9\hbar^2}{16eV_b}\frac{\mathrm{d}(\ln J)}{\mathrm{d}w_{TE}}. \qquad (4)$$

b: Profile Extraction

While chemical profiles can be obtained using secondary-ion mass spectroscopy (SIMS), as we have done in some cases, it is actually very difficult to obtain the profiles to the accuracy required (~1nm) for extracting tunneling distances. Furthermore; SIMS gives the chemical rather than the electrically active profile, so than cross-calibration with an electrical profiling method is necessary. In this study we use a CV technique to extract the profile information.

The well known CV method for extracting a profile of a one-sided junction gives the information:

$$N'(w) = \frac{CdV}{\varepsilon A dw}, \qquad (5)$$

where C is the capacitance, A the area, and, $w = \varepsilon A/C$, the depletion layer width (see also Sec. B-c, below) and $N'(w)$ the doping profile assuming one-sidedness. For a two sided junction with $w = x_2 - x_1$, and doping concentration $N(x_1)$ and $N(x_2)$ at the near and far sides of the junction, the following relationship holds:

$$\frac{1}{N'(w)} = \frac{1}{N(x_1)} + \frac{1}{N(x_2)}. \qquad (6)$$

The CV measurements alone are therefore insufficient to extract the profile of a two-sided junction without additional assumptions. By fitting the doping concentration to some parameterized function one could find the parameters by fitting measured and simulated CV curves, but solution of these equations would not lead to a unique solution. For instance, one is unable to unambiguously determine the degree of asymmetry of the profile this way, so that a physically justifiable trial function has to be used as the starting point. Having determined the parameters, the fitted profile could be used beyond the leakage current limited range of the C-V measurements.

In this work we adopt two trial functions for determination of the profile. When SIMS data is available it is scaled by a fitting factor A_E (electrical activation factor) and used, along with the built in voltage, which is related to the bandgap potential, V_b, (see next sub-section), to fit the CV data.

The other trial function is:

$$N(x) = N_{b0}[1 - e^{-x/\lambda}], \qquad (7)$$

where the parameter λ represents the exponential fall-off rate of the top dopant layer and N_{b0} the concentration in the bottom layer far away from the junction. Thus there are three parameters to be determined, V_b, N_{b0}, and λ. This function has the virtue of requiring few fitting parameters, having analytic solutions, and being able to emulate profiles varying from step to linearly graded. This functional form is justified when the junction is on the exponentially falling slope of the top dopant, and the depletion layer is narrow enough that the more slowly varying bottom dopant profile approximates a constant. We shall see later that even under conditions where this function is not a good approximation to the actual profile, it still determines tunneling distances with remarkable accuracy.

c: Built-in Voltage, bandgap and the depletion approximation.

The built in voltage, $V_{BI} = V_b - \Delta V_{BI}$, for a graded junction is a function of applied voltage through the dependence of the doping at the depletion layer edge, N_D and N_A, on the depletion-layer width. For a non-degenerately doped junction,

$$\Delta V_{BI} = \frac{kT}{e}\cdot\left[2 + \ln\left(\frac{N_C N_V}{N_D N_A}\right)\right], \qquad (8)$$

where N_C and N_V and the conduction and valence-band densities of states and, in the depletion approximation, the electron and hole concentrations are assumed to be the same as the doping densities. The leading '2' in this equation comes from the well known $2kT/e$ correction [16] applied to the depletion approximation to account for the non abrupt carrier

fall-off at the depletion-layer edges. While ΔV_{BI} is quite small in the doping range used for these experiments, (~50meV) it nevertheless leads to large errors in determining the bandgap if one neglects it. The main error arises because ΔV_{BI}, becomes quite large in the forward bias regime, where the doping is low, and which has a predominant weight in determining the built-in voltage [20]. For a linearly graded junction, Chawla and Gummel [16,21] investigated this effect and found that it resulted in a lowering of about 0.1V of the 'intercept' voltage (V-axis intercept of the C^{-3} vs. V plot).

For analysis of our experiments we use a variable ΔV_{BI} so the Chawla-Gummel effect is taken into account automatically. For a particular CV sweep we assume that, V_b is the constant parameter, to be extracted from the optimization routine, and that $V = V_{ext} + V_b - \Delta V_{BI}$, where V_{ext} is the applied (external) voltage, ΔV_{BI} is determined using (8) and the varying values of N_D and N_A are derived from the profile being fitted. As a consequence of the variable of ΔV_{BI}, the capacitance measured externally, C_{ext}, is different from the internal capacitance, C, because some of the AC voltage goes into changing ΔV_{BI}. This results in a correction to the depletion-layer width:

$$w_D = \frac{\varepsilon}{C} = \frac{\varepsilon}{C_{ext}(1+\xi)}, \qquad (9)$$

where $\xi = d\Delta V_{BI}/dV$. In a positively graded junction ξ is *negative*, which has the counter-intuitive result that the internal potential varies *faster* that the external potential so that $C_{ext} > C$. In the same spirit, a correction term of $(1 + \xi + w_D d\xi/dw_D)$ must be applied to the doping derived from (5) and (6).

For the profile fitting we assumed non-degenerate doping for the ΔV_{BI} corrections, yet the carrier concentrations at the depletion layer edge enter into the degenerate regime for our higher doped samples. Degeneracy has two opposing effects on the built-in voltage. The direct effect of higher Fermi-levels in conduction and valence bands increases the built-in voltage; yet the indirect effect, which is larger in our case, decreases the built-in voltage because of a softening of the carrier fall-off rate (the $2kT$ term in (8)) at the depletion layer edges. While retaining the simpler non-degenerate analysis for our optimization procedure, we make an accommodation for the indirect effect of degeneracy by replacing the temperature, T in (8), with an effective temperature, T_e, which is given by the inverse logarithmic slope of the doping density vs. Fermi level:

$$\frac{T}{T_e} = \frac{1}{\sqrt{2\pi}y} \frac{\mathbf{F}}{-1/2}[\mathbf{F}^{-1}_{1/2}(y)], \qquad (10)$$

where $\mathbf{F}_n$ is the n th order Fermi integral, and a mean doping factor $y = (N_D N_A / N_C N_V)^{1/2}$ is used. This procedure, while plausible, is a heuristic, i.e. lacks a rigorous proof.

As a check on the above methods, the results of our CV analysis are compared against numerical simulations using the FIELDAY [22] program, which includes full, degenerate statistics. CV curves are simulated using FIELDAY and the profiles derived from our analysis above, and the two sets of CV curves compared (see Sec. DSec. a).

C: Experimental Methodology

Our approach is to use simple geometries and structures, which are easy to quantify, yet use sophisticated, modern, ion-implanted structures, over a wide range of dose, which make our study relevant to present, and hopefully future, CMOS integrated circuit technology. Various types of implants were studied to investigate to what extent our data might be process independent. Planar, oxide-isolated, PN junctions were fabricated over a wide area range, on low-resistivity substrates, in order to reduce series resistance. This study emphasizes the reverse leakage regime, which is dominated by band-to-band tunneling. Only samples with strictly area independent reverse current densities were investigated, and small sized samples were chosen to allow large current densities to be measured without incurring excessive voltage drops due to series resistance. Capacitance measurements were the key to obtaining information on the doping profile and evaluating internal fields and tunneling distances. The measurements were done on small samples and at high frequencies to extend the measurement range to higher forward and reverse voltages and higher doping levels. SIMS measurements were done on selected samples to bolster the CV measurements. To obtain the highest accuracy, separate ion bombardment species, Cs vs. O_2, were used on some wafers to obtain the As vs. B information.

Samples were fabricated with a wide range of implant doses to obtain junction doping ranging from ~2×10^{18} to ~7×10^{19} cm^{-3} in eight steps. Measurements were done exclusively in a low voltage range (1V forward to 1.5V reverse) which represents the range of interest for scaled

CMOS. A temperature range from 100K to 350K was studied. Lower temperatures suffer from the complications of freeze-out, yet a moderately low temperature aids in analysis of the data in removing overt effects of the thermal distribution of the carriers, as well as reducing the leakage for the CV measurements. Temperatures of 150K and 300K were chosen for presentation of the data, although data was measured and analyzed at all (six) temperatures and for all samples.

a: Sample Preparation

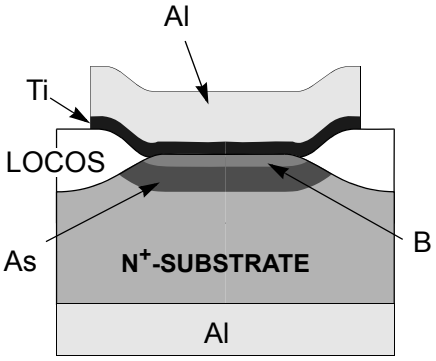

Fig. 2. Sample structure for the case of a P/N diode. Opposite dopant type, including substrate, would be used for N/P diode.

The sample structure is shown in Fig. 2. N-type or P-type substrates were used, having resistivities of 0.017-0.018W-cm and.04-.05W-cm respectively. This corresponds to doping levels of 1.4×10^{18} and 1×10^{18} cm^{-3} respectively, which is below the minimum junction doping used in this study. Oxide isolated areas were created using local oxidation (LOCOS), with many different sized areas being available from the mask-set, while the present experiments used mainly 10 and 50μm sized squares. The N and p-type implants were then done through a 3.5nm screen oxide. In all cases a germanium amorphizing implant of 3×10^{14} at 15Kev was done prior to the junction implants. Implant parameters were as given in Table I. The devices were fabricated on six, eight inch, silicon wafers divided into three junction types with shallow As, B or BF_2 implants and deep As or B implants as given in the Table. Two wafers were allocated to each type and each wafer was divided into four quadrants giving eight quadrants (Q1-Q8) per junction type. Following the implants the wafers were given rapid thermal anneals for 5s, to 1050C for the N on P, and to 1000C for the P on N wafers. The lower temperature for the P on N wafers was to minimize B diffusion. Then a pre-metallization forming-gas anneal was done at 400C for 30min. The screen oxide was then etched off using a short HP dip, and Ti/Al was deposited followed by a 200C 30min sinter. The temperature was chosen to reduce silicide spiking. The contact resistance was tested by measuring N/N and P/P samples of different areas, where the sample resistance was found to be limited by the spreading resistance to the substrate.

TABLE 1. Implant splits

Type	Top		Bottom (B or As)				
	Ener. (KeV)	Dose (cm^{-2})	Ener. (KeV)	Dose (1E14 cm^{-2})			
				Q1	Q2	Q3	Q4
				Q5	Q6	Q7	Q8
NP	3	As 2.5E15	20	0.6	1.2	2	2.6
				3.5	4	6.3	7.5
PN-B	2	B 1.0E15	100	0.21	0.43	0.71	0.93
			85	1.32	2.31	3.3	4.29
PN-BF_2	5	BF_2 1.0E15	100	0.21	0.43	0.71	0.93
			85	1.32	2.31	3.3	4.29

Results of SIMS analysis are shown in Fig. 3. A very pronounced boron dip is seen in the N on P wafer. The resolution of the dip, to this extent, is a measure of the quality of the SIMS technique. Since the N/P junction is formed in the vicinity of the dip it is essential to obtain the highest accuracy in the analysis on the N/P samples (P/N are less critical as seen in Fig. 3b). To achieve this the As was sputtered using Cs and the B using oxygen for these samples. It is also seen from Fig. 3b that the junctions are shallower and considerably sharper when BF_2 is used as the implant species. This reflects the fact that the kinetic energy of the B in BF2 is only 1.1KeV.

Following processing samples were screened to make sure the currents were proportional to area, and those selected were mounted on 8-pin TO-5 headers for further measurement.

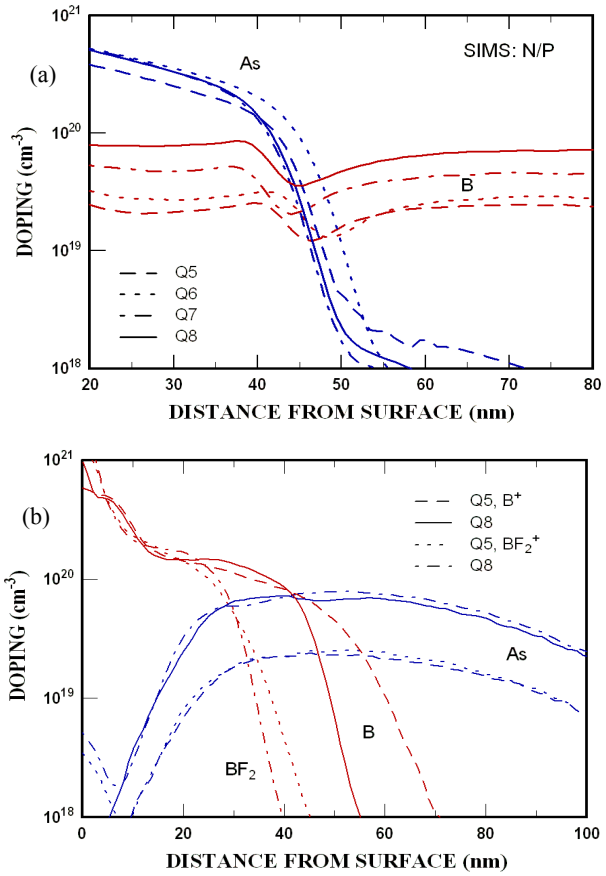

Fig. 3. SIMS profiles of (a) N/P and (b) P/N diodes for the indicated quadrants. For the N/P profiles the As was sputtered with Cs. For all other profiles O_2 was used The Boron and BF_2 implanted profiles are compared in (b).

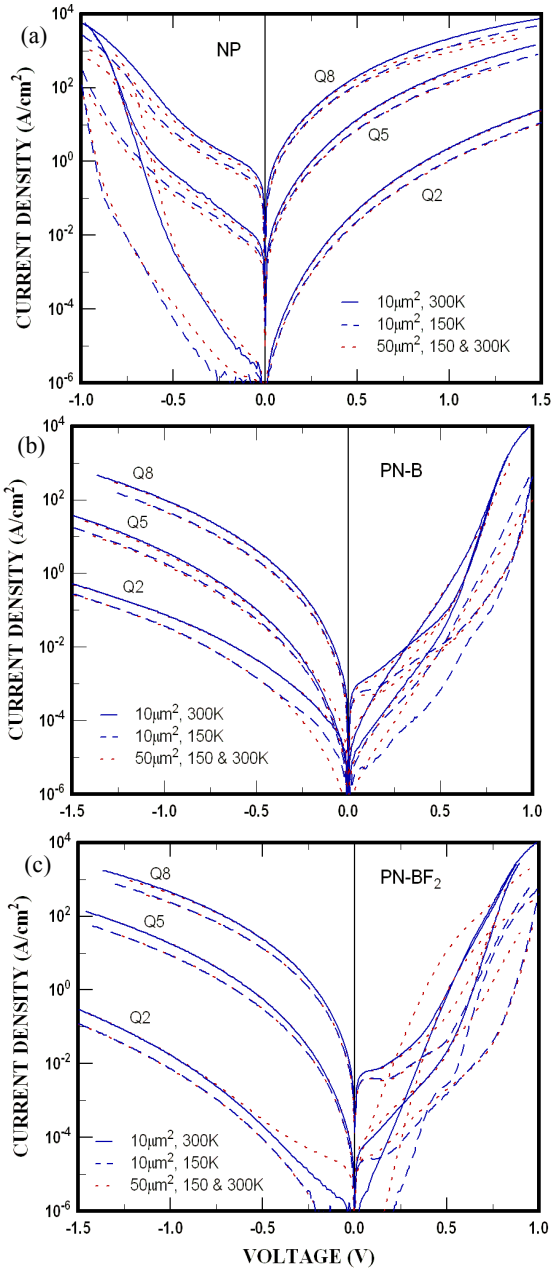

Fig. 4. Current-Voltage characteristics for the N/P (a) and P/N diodes using B (b) and BF_2 (c) implants, for quadrants Q2, Q5 and Q8, for temperatures 150 and 300K and for square samples of 10μm and 50μm size.

b: I-V measurements.

I-V measurements on the header-mounted samples were made using the HP 4245B parameter analyser. A 4-point technique was used to minimize lead resistance. It was also found during measurements that the resistance of the back-interface was significant, because of the small area of the cleaved, header-mounted piece. To eliminate this resistance, a spare sample was used as a probe of the substrate potential in the 4-point technique. Even though this was a P/N junction, the junction was sufficiently leaky to serve as a voltage-contact for the higher doped samples. Measurements were done at temperatures from 100K to 350K in ~50K increments. The temperature accuracy was ± ~2K. Absolute current vs. voltage characteristics are shown for all three doping types in Fig. 4a-c, for quadrants Q2, Q5 and Q8, for temperatures 150 and 300K and for square samples of 10μm and 50μm size. In reverse bias, which is the focus of this study, the curves for the two areas overlay except at very high currents where substrate series resistance is significant, and at very low currents where other sources of leakage may dominate. The forward characteristics are very variable, and gross departures from area scaling occur in some instances. This is because the band-to-band tunneling, which dominates the

reverse characteristics, is suppressed in the forward direction, and trap dominated leakage mechanisms take over. The lack of the negative resistance region in the forward characteristics (except for a hint of one for the PN-BF_2 sample at low temperatures, attests to the difficulty of achieving PN junctions in silicon which are strongly degenerate on both sides, by ion implantation, due to the strong interaction between the B and As dopants [23]. This contrast with epitaxial studies [8,9], at considerably higher doping levels, where a well-developed negative resistance region is obtained.

c: C-V measurements.

CV measurements were made with the Agilent 4294A Precision Impedance Analyzer. To minimize parasitics, two leads were bonded onto each pad, enabling the 4-probe technique to be extended right onto the wafer. Special calibration headers containing open, short and load (100Ω) standards were provided, and calibration was done right down to the header. Calibration files were prepared for each temperature. Capacitance was measured at a frequency of 18MHz, and at signal amplitude of 25mV. For the highest doped quadrants the smaller, 10µm, sized sample was measured to reduce the effects of series resistance. Parasitic capacitance was extracted by comparing the zero-bias capacitance for 10 vs. 50µm samples. DC voltage drops across the back-side contact were accounted for by subtracting the voltage drops determined during the I-V measurements. This resistance, being due to a Schottky-like contact to the metallized back side of the chip, does not affect the capacitance (apart from the de-biassing) because of the large parallel capacitance of that contact. These techniques enabled the capacitance (~2pF) to be measured in the presence of up to ~1mS of leakage conductance.

Capacitance vs. voltage characteristics are shown for all three doping types in Fig. 5a-c, for quadrants Q2, Q5 and Q8, and for temperatures 150 and 300K. The turn-up of the experimental curves at large reverse bias is due to leakage. Lower temperatures permit a somewhat larger range for significant measurements to be achieved.

D: Analysis and Results

a: Profile Extraction

The doping profile is extracted from the CV curves using the methods discussed in Sec. B-b, using the exponential trial function for all quadrants, and the SIMs data for the upper four quadrants. The profiles for selected quadrants (Q3, Q5, and Q8) are shown in Fig. 6 (all quadrants were measured but only selected data is shown here to avoid clutter). At high doping the exponential fit deviated markedly from the SIMs fit, yet all give excellent fits to the CV data, as shown in Fig. 5. This is because of the inherent ambiguity in the profile symmetry, as discussed in Sec. B-b. This may be seen clearly in Fig. 6b, at the highest doping, where the strong compensation actually results in a *retrograde* profile (steeper on the substrate side) compared to the assumed exponential profile. At the other extreme, for the lowest doped quadrant, Q1 (also seen for Q2 in Fig. 6b), the deple-

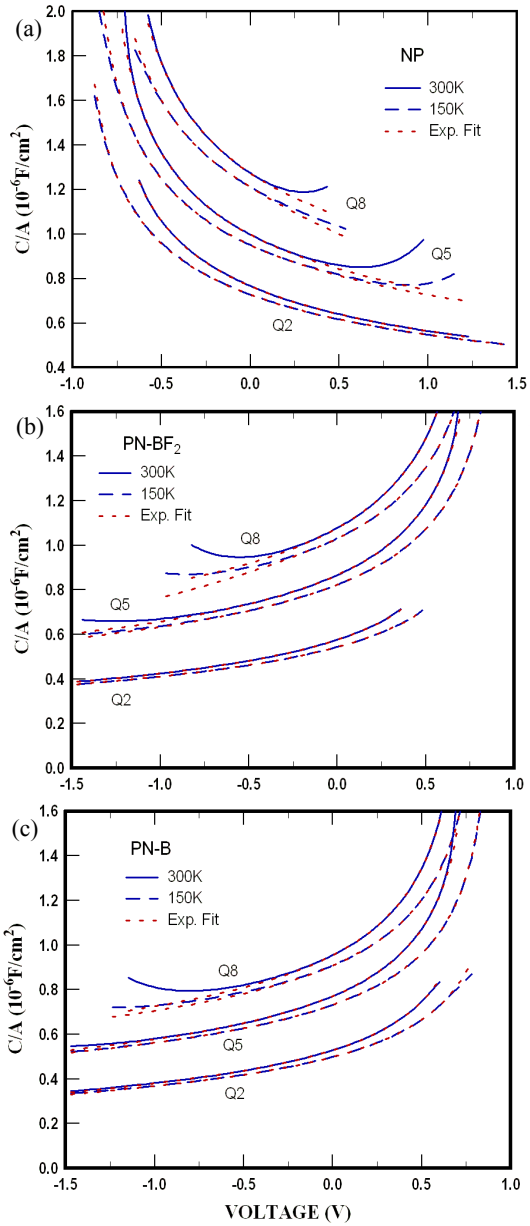

Fig. 5. C-V characteristics for the N/P and P/N diodes using B and BF_2 implants, for quadrants Q2, Q5 and Q8, for temperatures 150K (dashed) and 300K (solid) compared to simulated curves based on an exponential profile (dotted).

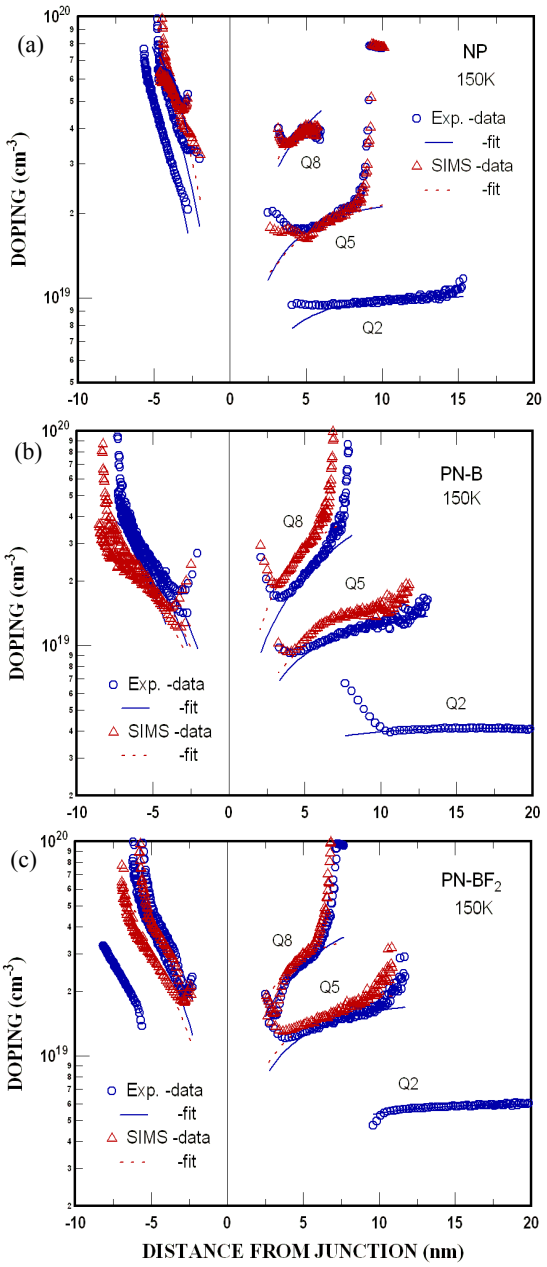

Fig. 6. Doping profiles derived from fitting the exponential trial function (□) and by scaling the SIMs data (Δ) to CV curves measured at 150K. Quadrants Q2, Q5, and Q8 are shown for (a) the N/P, (b) the P/N-B and (c) the P/N-BF$_2$ wafers.

tion edge scans past the doping peak, causing some difficulties in the use of the exponential profile, yet the peak is broad, so that the profile does not deviate greatly from the exponential form.

The bandgaps, derived from these fits are shown in Fig. 8, as a function of temperature. The temperature dependence is less than the literature value [17], especially at

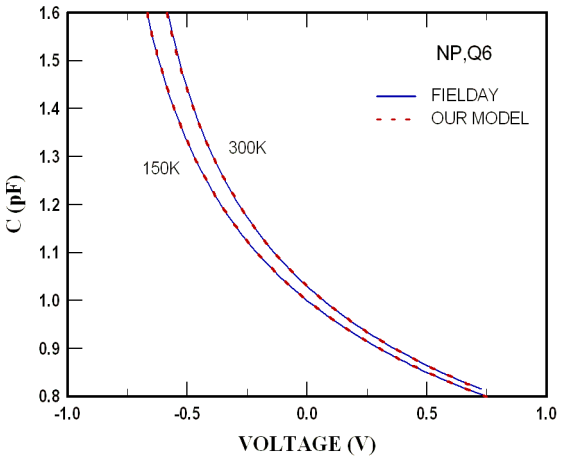

Fig. 7. C-V curves for a 10x10mm2 N/P diode comparing FIELDAY simulations with our model at temperatures of 150K and 300K, for an N/P sample using a SIMS derived profile. The bandgap and activation, for best fit, are compared below for the two models.

	Bandgap (eV)		Activation	
	Our model	FIEL-DAY	Our model	FIEL-DAY
150K	0.968	0.943	0.986	0.977
300K	0.961	0.935	0.966	0.967

lower temperatures, yet gives good agreement with the trend at higher temperatures. The magnitude of the disagreement (~50meV) is comparable with the uncertainty of our technique. It is interesting to note that the temperature depen-

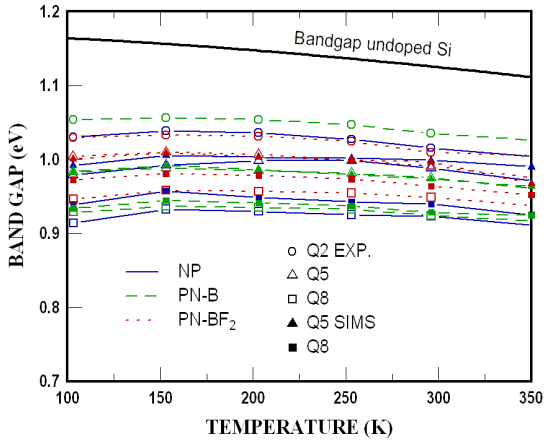

Fig. 8. Band-gap, determined from the CV fits, as a function of temperature. Line styles for wafer types are: N/P (solid), P/N-B (dashed) and P/N-BF2 (dotted). Open symbols are fits to the exponential profiles and filled symbols to the SIMs profiles. The bandgap formula is from [16].

TABLE 2. Doping parameters for N/P wafers.

Q	N_{b0} (10^{19}cm^{-3})		λ (nm)		dN/dx (10^{26}cm^{-4})	
	153K	296K	153K	296K	153K	296K
1	0.50	0.52	2.29	2.39	0.22	0.22
2	1.01	1.03	2.80	2.79	0.36	0.37
3	1.39	1.38	2.31	2.15	0.60	0.65
4	1.68	1.70	2.27	2.18	0.74	0.78
5	2.22	2.24	3.37	3.25	0.66	0.69
6	1.97	1.88	2.28	2.19	0.86	0.86
7	2.74	2.84	2.38	2.45	1.15	1.16
8	8.17	11.56	7.16	9.97	1.14	1.16

TABLE 3. Doping parameters for P/N-B wafers.

Q	N_{b0} (10^{19}cm^{-3})		λ (nm)		dN/dx (10^{26}cm^{-4})	
	153K	296K	153K	296K	153K	296K
1	0.23	0.24	2.69	2.93	0.09	0.08
2	0.42	0.42	2.95	3.89	0.14	0.14
3	0.77	0.80	4.75	4.96	0.16	0.16
4	0.97	1.02	4.81	5.01	0.20	0.20
5	1.50	1.45	5.37	4.94	0.28	0.29
6	8.89	10.07	24.19	26.55	0.37	0.38
7	9.39	15.93	21.87	36.46	0.43	0.44
8	14.80	13.3	12.51	28.39	0.46	0.47

TABLE 4. Doping parameters for P/N -BF_2 wafers.

Q	N_{b0} (10^{19}cm^{-3})		λ (nm)		dN/dx (10^{26}cm^{-4})	
	153K	296K	153K	296K	153K	296K
1	0.31	0.34	3.94	3.78	0.08	0.09
2	0.60	0.62	4.40	4.35	0.14	0.14
3	1.05	1.08	5.50	5.46	0.19	0.20
4	1.27	1.35	5.30	5.57	0.24	0.24
5	1.81	2.21	4.32	5.34	0.42	0.41
6	6.81	6.65	13.27	12.33	0.51	0.54
7	15.05	15.39	22.70	23.07	0.66	0.67
8	6.09	9.05	8.64	12.72	0.70	0.71

dence of V_b is substantially independent of the doping in this range, while V_b itself decreases with doping. There is close agreement between the two fitting techniques, notwithstanding the ~20mV higher V_b for the highest-doped quadrants on th N/P and PN-BF_2 wafers when using the SIMS based fitting function. Some systematic differences between the two methods could be due to perturbation of the doping near the junction, caused for instance by the boron dip, which is not simulated well by the exponential fitting function.

CV curves were simulated with the FIELDAY program (see Sec. BSec. b) and the SIMS profiles, using the previously derived activation factors and bandgaps as an initial guess. CV curves are shown in Fig. 6 for a particular sample (NP, Q6) and fitting parameters for this sample are compared in the accompanying table. For all of the samples the two methods give results which are almost identical except that FIELDAY requires an ~20mV lower bandgap. No significant extra corrections are required for the more degenerate cases (low temperature, high doping) indicating that our heuristic procedure is reasonable. It was hoped that the FIELDAY fits would increase the bandgap at lower temperatures to better agree with the literature, but this was not the case.

Doping parameters for all quadrants, by the two fitting methods, are compared at two temperatures (150 and 300K) as shown in Tables 1-5. The doping gradient at the junction

TABLE 5. Activation parameter for all wafers.

Q	Activation					
	N/P		P/N-B		P/N-BF_2	
	153K	296K	153K	296K	153K	296K
5	1.04	1.07	0.87	0.90	0.79	0.83
6	0.96	0.94	0.83	0.86	0.91	0.95
7	0.90	0.91	0.93	0.96	0.90	0.91
8	0.92	0.92	0.63	0.65	0.53	0.54

TABLE 6. Doping gradient from SIMS fit.

Q	dN/dx (10^{26}cm^{-4})		
	N/P	P/N-B	P/N-BF_2
5	0.74	0.28	0.43
6	0.82	0.36	0.54
7	1.14	0.50	0.72
8	1.34	0.41	0.82

is also shown. For most part the parameters are temperature independent (within the accuracy of the technique) lending support to our extraction method. Exceptions are in the case of high doping levels, where the profile approaches linear grading, where the parameters, N_{b0} and λ, are not separable. Here the gradient becomes a much better parameter (e.g. PN-B, Q6) .

The accuracy of both the CV extraction technique and the SIMS measurements is attested to by the reasonable values of the activation parameters in Table 5. An error of ~10%, in activation, in either technique would be quite apparent since activations of greater than 100% are not possible and activations of less than 80%, for most of the conditions, are not likely. It is not clear what causes the lower activations for Q8 of the PN-B and -BF_2 wafers, but this is consistent with the lower annealing temperature (1000C) for these wafers and the fact that Q8 of these wafers corresponds to the highest As doping condition. As seen in Fig. 3b, these quadrants are the most highly compensated, which could easily lead to sizeable errors in the extraction from the SIMS data.

The profile data were used to extract junction fields and effective tunneling distance, according to the methodology of Sec. B-a. It was remarkable to find that despite the obvious differences in the profile shape, the tunneling distances derived using the two techniques were very similar, as shown by plotting the difference between them in Fig. 9. The difference diminishes for the lower-doped quadrants, as expected, justifying our reliance on the exponential profile fit for the lower-doped quadrants.

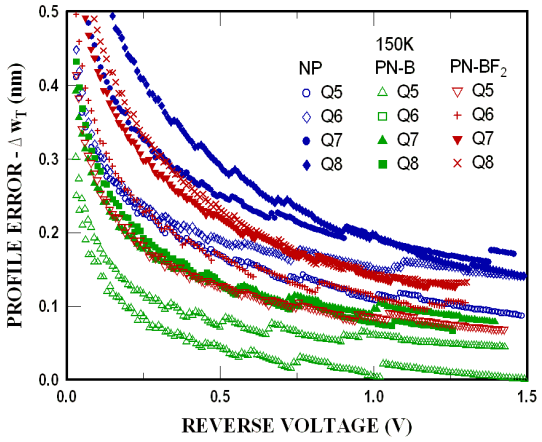

Fig. 9. Difference in effective tunnel distance calculated from profiles extracted using SIMS and exponential trial functions.

b: Current Density vs. Field

Our experimental I-V data were analyzed using the C-V extracted profiles. For the lower doped wafers (Q1-4) where no SIMS data were available, the exponential fitting function was used, and otherwise the SIMS derived fitting function was used. Our results were also compared to the results of Hurkx *et al*. [14] using his zero-bias depletion layer widths and substrate doping, along with our values for V_b, to derive profile parameters. Other work was not used because either not enough information was available [13], or the results were on <111> silicon [5,7].

The logarithm of the conductivity (current-density/voltage) as a function of the inverse maximum junction field is shown in Fig. 10. According to the most simple tunneling theory [16] this should give an approximately linear relationship for a junction with uniform internal field, under reverse bias since the tunneling distance is inversely proportional to the field, and the energy range for tunneling is proportional to the voltage. Both our data and that of Hurkx *et al.* [10] deviate considerably from this relationship, and there is considerable spread between the data from different wafers, dopings and sources. Furthermore, the trend is different from that used by Taur *et al.*[1] to predict future device behavior. Plotting just the current density (Fig. 10b) brings our results closer to Taur's trend line, yet the functional dependence of the individual curves is obviously different. The differences can be explained by the lower voltages used in our study, which violate the uniform field assumption, by the fact that Taur's curve is partly based of <111> data, and also to possible differences in the physics of the tunneling process, as we will discuss later.

c: Current Density vs. Effective Tunneling Distance.

Tunneling current is expected to be more closely correlated with the tunneling distance than the electric field, especially at small voltages where the field varies along the tunneling path. Therefore, following Sec. B-a, the current density was plotted as a function of the effective tunnel distance, which includes our curvature correction. Better unification of the data, and more linear plots were obtained when choosing to plot current density rather than conductance, or even the current normalized to the half width of the tunneling energy range (see Fig. 1), so that this method of presentation was chosen. Results at 300 and 150K are shown in Fig. 11, where a very satisfying unification of the data is achieved especially for the higher currents. Comparison of our data with [14], as shown in the figure, is also very reasonable, where deviations could well be due to our lack of knowledge of their precise doping profile. Obvious sample-

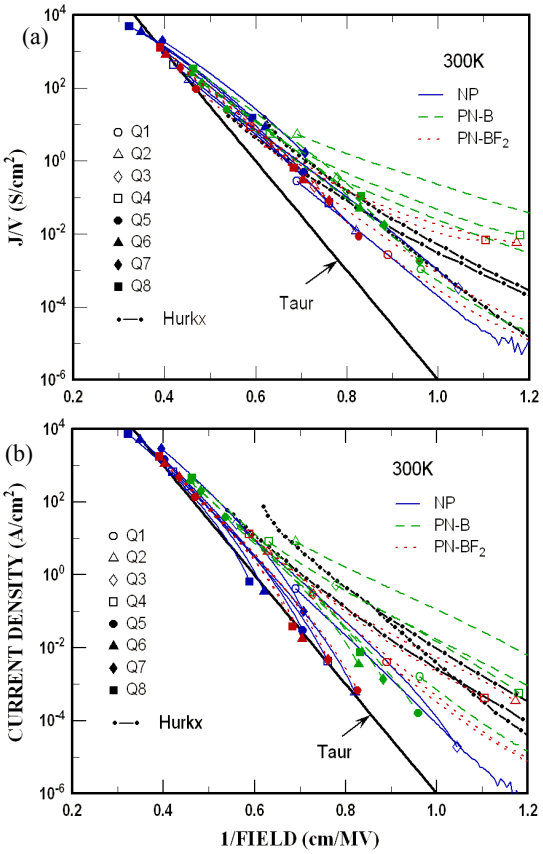

Fig. 10. Conductivity (a) and current density (b) vs. inverse maximum junction fields for all samples and all quadrants at 300K. The fitting curve of Taur et al.[1], and the data of Hurkx et al.[10] are shown for comparison.

to-sample deviations from the linear trend are seen at the lower current densities, where other leakage mechanisms may be operative, especially for some of the lower doped quadrants of the PN-B and PN-BF_2 wafers where the leakage is anomalously high. At higher currents the distribution for these wafers is very tight, with the curves essentially overlaying each other for the upper four quadrants, giving two sets of curves for the two temperatures. The correction of the tunneling distance for the non-uniform field (curvature correction), is shown in Fig. 12, and appears to be an almost universal function of applied voltage at 300K, in spite of considerable differences in profile shape from wafer to wafer and quadrant to quadrant, and is anyway not very large, being between 0.9 and 1.0 over most of the voltage range.

Data measured for all three implant types, for the four highest doped quadrants (Q5-8) and for temperatures of 150 and 300K, are shown in Fig. 13. Fitting this data, at the high current end, to straight lines given by the expression

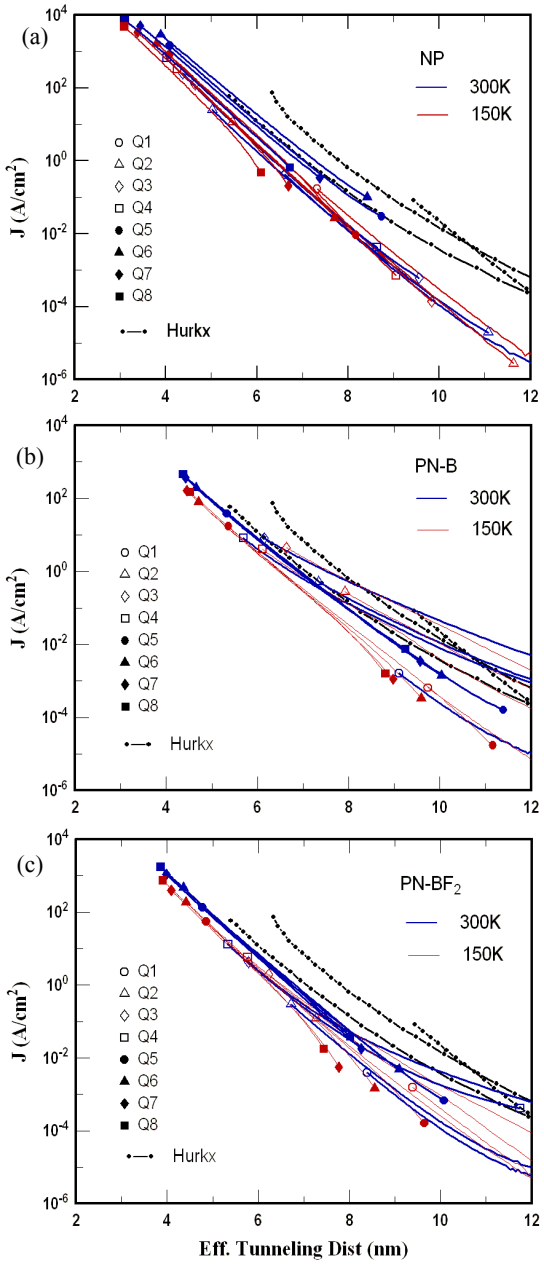

Fig. 11.Current density vs. effective tunneling distance, and comparison with the data of Hurkx et al.[14]. The inset shows the correction applied to the actual tunnel distance to account for junction curvature. Data are from all quadrants of the N/P wafers (a) the P/N-B wafers (b) and the P/N-BF_2 wafers (c).

$$J = A(T)\exp(w_{TE}/\lambda_T) \qquad (11)$$

one obtains λ_T = 0.38nm and A = 2.0×10^7 and 5.3×10^7 A/cm^2 at 150K and 300K respectively. The value of λ_T, from (4), gives a tunneling effective mass of 0.29m_0, assuming a bandgap of ~1eV.

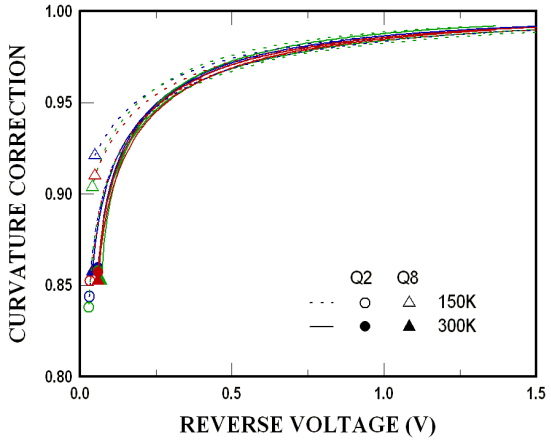

Fig. 12.Curvature correction, φ/φ_F, for non-uniform field, vs. applied voltage. Data for quadrants Q2 (lower doped) and Q4 (highest doped), and for all three wafer types NP, PN-B and PN-BF2, and at two temperatures, 150K and 300K, are superimposed.

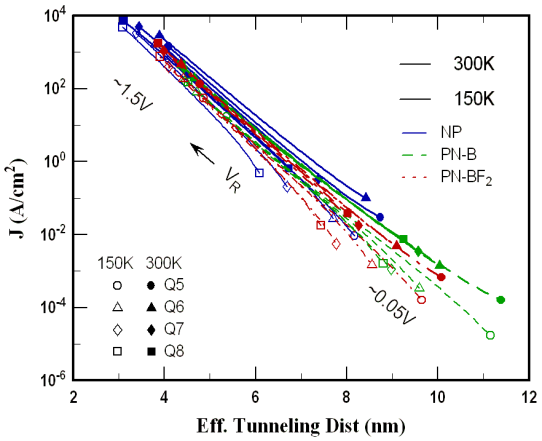

Fig. 13. Current density vs. effective tunneling distance for the highest doped quadrants (Q4-8) of all three wafer types and at 150 and 300K. Each curve, for a particular quadrant and temperature, covers a voltage range as indicated in the figure, although the internal voltages for the most heavily doped quadrants are reduced by series resistance.

d: Current Density vs. Temperature.

While a weak temperature dependence is evident in the original data, this dependence will be distorted by the change of the tunnel width with temperature, which decreases, at a constant voltage, at low doping levels and increases at high doping. To clarify this, the current was plotted as a function of temperature at a constant tunnel distance in Fig. 14 for Q5-8 of the three wafer types. The temperature dependence is similar to that reported by others [5,7,13,14], yet plotting it this way reveals that it is almost independent of the wafer parameters, except for the anomalous dependence at higher temperatures of Q6 of the NP wafer.

E: Discussion.

As we saw in Fig. 13, a remarkable unification of the data has been achieved when plotting the current density vs. effective tunnel distance. While from the theoretical perspective this leaves some difficult issues to be explained, from the empirical standpoint it is a boon for those wishing to estimate tunneling current in silicon devices. The near independence of the tunneling current on process and implant conditions, bearing in mind that our processes were engineered to produce high quality junctions, points to an intrinsic process where process induced-traps do not play a major role in the tunneling process. It is worth noting, however, that a tunneling process via a mid-gap trap would give the same decay length as in the Keldysh model, where a phonon mediates the mid-gap transfer. Some of our higher lying data at lower currents, as well as some of the referenced data [14] could be tunneling via traps. It should be noted that our tunneling currents for different wafers, in the higher range, agree closely with each other in spite of the fact that the compensation ratios for the different wafers were very different, ~30% for the highest doped quadrant of the NP wafer, ~65% for the PN-B and ~45% for the PN-BF_2 wafers. The tunnel current densities do not seem to be affected by this.

The effective mass, as derived in Sec. b-c, of $0.29m_0$, is very reasonable considering the values of the light electron and hole masses in Si (see Sec. B-a). Given the complex

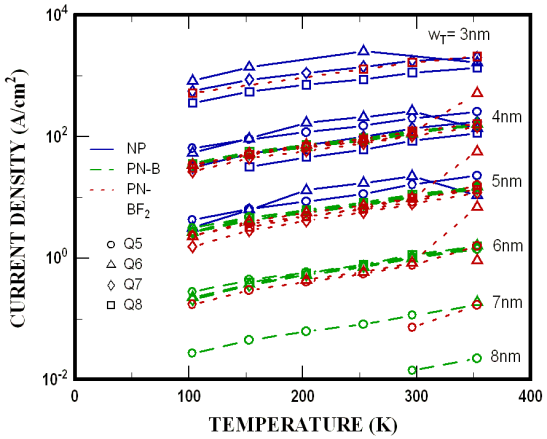

Fig. 14.Current density vs. temperature, at a constant effective tunneling distance, as indicated in the figure, for Q5-8 of all three wafers types.

band-structure of silicon, and our crude methods of analysis, this agreement is considered to be good, and awaits detailed numerical modeling for further refinement. The effective mass is very reasonable when compared to the light electron and hole masses in silicon, and bolsters the mid-gap transfer model. The magnitude of the intercept in the Keldysh model is approximated, under reverse bias conditions by [7]

$$J_0 = \frac{e^3 F_{max} V_R}{4\pi^3 \hbar^2 V_b} \sqrt{\frac{2m}{e}}, \qquad (12)$$

where F_{max} is the peak junction field, and V_R the reverse voltage. The effective-mass to use is unclear, but we will use the mass derived from the slope. Evaluating (12), with F_{max} = 2.5MV/cm, and V_R = 1V, gives $J_0 = 1.1\times10^8$ A/cm$_2$. This is within a factor of two of our 300K value, indicating that the phonon-mediated mechanism is reasonable, but (12) gives a super-linear voltage dependence, in contrast to our assumed lack of dependence on voltage.

The main theoretical question concerning our results is the weak voltage dependence of the tunneling pre-factor. The voltage dependence of the current density, at a constant effective tunneling distance, is shown in Fig. 15, where data from different wafers quadrants are combined. None of the data shows the super-linear behavior (power law of 5/3 for a graded junction at high voltages) predicted by (12). For most part the data are sub-linear, approaching almost a constant at 300K for the PN-B and PN-BF2 wafers, while being closer to linear at 150K. This conclusion is somewhat dependent on the value bandgap used in the extraction of w_{TE}, with the voltage dependence increasing for a higher assumed bandgap, and is also dependent on the form of the curvature correction (see Fig. 12), yet we believe this anomalous voltage dependence is significant, and needs to be verified against more sophisticated models.

As a check against more sophisticated theory, we compare our data with recent tunneling theory of Rivas et al. [24] based on the data of [8]. While this data is in the *forward* bias regime, the very heavy doping leads to considerable overlap of the bands making this situation applicable to our case, especially in light of the weak voltage dependence of the current density at room temperature. Using the band diagram in [24], which corresponds to the peak current condition, we estimate a minimum tunneling distance of 4.3nm, which along with a curvature factor of ~0.9 leads to an estimate of the current density, based on our data, of 1500A/cm^2. This in good agreement with the *theoretical* estimate in [24], even though the experimental value, in [8] was about an order of magnitude higher. We suggest that the discrepancy lies in the doping profile of [8], which is at the limits of the SIMs technique.

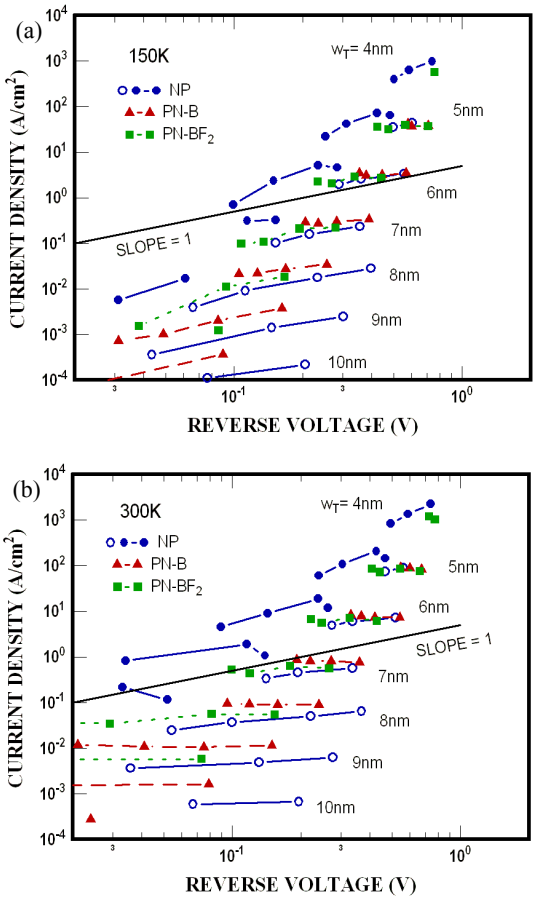

Fig. 15.Current density vs. voltage at a constant effective tunneling distance, at 150K (a) and 300K (b), with each curve plotted across quadrants of the same wafer. Open symbols indicate quadrants 1-4 (wafer NP only), and filled symbols indicate quadrants 5-8 of all wafers as indicated.

A critical aspect in our analysis was the extraction of doping profiles and tunneling distances from CV data. It was seen in Figs 5, 6, 8 and 7, and in Table 5, that the CV analysis yields very credible results. Our results are also a source of new bandgap data, as a function of doping, for silicon. The reason that this seemingly obvious method has not been used much to date is perhaps the sensitivity of the extracted bandgap to the modeling assumptions, and the difficulty in obtaining highly accurate CV data from heavily-doped P/N junctions. In Fig. 16 the bandgap is plotted against the doping (P or N) at the junction, and compared to data in the review paper of van Overstraeten and Mertens [25], and

Swirhun *et al.* [26] The bandgap may be affected [25] by free-carriers, or by the total dopant concentration, yet the capacitance, being primarily a property of the depletion region, should, to first order, be unaffected by free-carrier bandgap lowering. One might argue that the potential in the contacts, hence the built-in voltage will be directly affected by free-carrier bandgap lowering in the contacts, but this is not so; the situation is analogous to a contact potential which is cancelled by the potential developed by the hetero-barrier formed between regions of higher and lower bandgap (Second-order effects caused by band-bending and by non-local interactions [27] may be important but are beyond the scope of our analysis.). Our data of Fig. 16 support this contention. Some of the lowest bandgaps are found in higher-doped quadrants the PN-B wafer, which has a greater compensation, and lower free-carrier concentration, than the other two wafers. Our data agrees well with that of Ref. [25] although there is a systematic shift of ~50meV, with a slightly steeper trend-line, which is at the borderline of the uncertainty in the data, and the assumptions of our analysis.

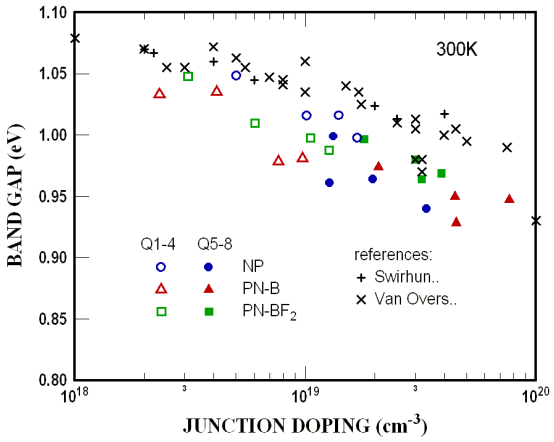

Fig. 16. Silicon bandgap, at 300K, as a function of junction doping. For Q5-8 the junction doping was extracted from the SIMs data, and for Q1-4 the doping was extracted from the CV using the exponential fitting function. Reference data is from [25] and [26].

As an illustration of the engineering utility of our data and method of interpretation let's examine the advanced FET structure of Taur *et al.* [1] and estimate the tunneling leakage current. The tunneling region, shaded in Fig. 17, is the region of shortest distance between contours separated by ~1V (the bandgap) and is 5.4nm in length by ~10nm in width. A curvature factor of ~.97 is inferred from Fig. 12 by noting that the total potential (1.6V) is 0.6V greater than the bandgap, thus the effective tunneling length becomes

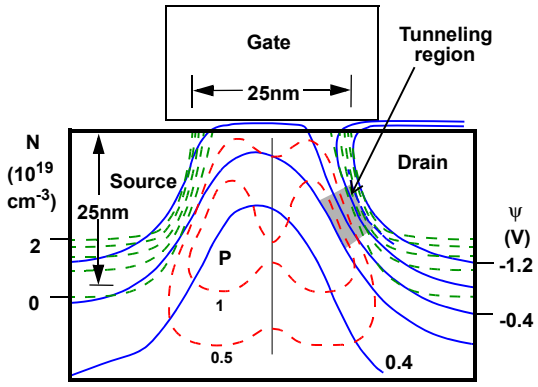

Fig. 17. Advanced 25nm gate-length FET structure proposed by Taur et al. [1], reproduced with permission, with minor changes. Drain voltage is 1.2V. Solid contours are electrostatic potential, in 0.2V intervals, and dashed contours indicate doping, in 5E18cm-3 intervals with open contours being N-type and closed contours P-type. Region of shortest tunneling distance is shaded.

5.25nm. The tunnel current density, from Fig. 13, is ~40A/cm^2, or ~4nA/μm. While low, in device terms, this current increases exponentially with further scaling so will quickly become important. For instance, if the whole geometry is shrunk by 2×, tunneling region of 2.6×5nm^2, the current will increase to 2.5μA/μm, which is prohibitively large for most applications.

A proviso, concerning the above analysis is that our experimental results are for tunneling in the <100> direction while devices are generally aligned along the <110> direction, in addition to the angle out of the plane (see Fig. 17). This might necessitate further experiments using different crystal orientations, the <110> direction should be sufficient. Alternatively, if our present results verify existing, detailed, models, these models could be used with confidence to simulate future devices.

F: Conclusions

Using technologically relevant ion-implanted profiles, we have shown that tunneling perpendicular to the (100) surface, at high currents, is independent of the implant dose and type, for the conditions studied. The current density, in this regime, decreases exponentially with tunneling distance with an attenuation length of 0.38nm, corresponding to a tunneling effective mass of 0.29m_0, and a prefactor of 5.3x10^7 A/cm^2 at 300K and 2.0x10^7 A/cm^2 at 150K. The magnitude of

the prefactor is consistent with a phonon-assisted tunneling process, although its dependence of the applied voltage is much weaker than expected. The doping dependence of the bandgap, extracted from the CV data, agrees with published data derived from transport in Si bipolar transistors. Our data was shown to be useful in analyzing ultra-scaled MOS transistors and should be useful in quantifying the limits of silicon CMOS, especially when incorporated into 2-D or 3-D device simulators. The need to extend this work to other crystal orientations, especially (110) was emphasized.

G: Acknowledgments

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