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S. M. Rossnagel
IBM Research Division
Thomas J. Watson Research Center
P.O. Box 218
Yorktown Heights, NY 10598

T. S. Kuan
SUNY Albany
Albany, NY

Research Division
Almaden - Austin - Beijing - Haifa - India - T. J. Watson - Tokyo - Zurich

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ALTERATION of Cu CONDUCTIVITY in the SIZE EFFECT REGIME

S. M. Rossnagel, IBM Research, PO 218, Yorktown Heights NY 10598
T.S. Kuan, SUNY Albany, NY

ABSTRACT

The resistivity of thin Cu films depends on film thickness as the dimensions approach the electron mean free path for Cu of 39 nm. The key size-dependant contributions are from electron-surface scattering, grain boundary scattering, and surface roughness-induced scattering. Measurements with pseudo-epitaxial Cu films deposited on Si have been undertaken to reduce effects of grain boundaries and surface roughness, which suggest an electron-scattering parameter of $p = 0.12$. Overlayers of metal films on the Cu generally increase the resistivity for Ta and Pt overlayers, and may reduce the resistivity for Au and Al. The resistivity increase may also be reversed if the overlayer oxidizes.

INTRODUCTION

A key issue in the continuing evolution of microelectronics has been the impending resistivity increases in the Cu lines used for interconnects due to size-related phenomena. The classic "size effect," a term which is often used generically to describe these effects, begins to become important when the dimensions of the circuit features approach 2-3 times the room temperature mean free path for electron-phonon collisions, which for Cu is 39 nm. At this point, non-specular interactions between the electrons and the surfaces of the lines result in a net slowing down of the electron motion and an effective increase in the resistivity. However, the size related phenomena which are relevant to electrical resistivity also include significant contributions from grain boundary scattering and surface roughness, which in addition to impurities result in additional electron scattering and reduced conductivity.

Addressing whether these size-related effects can be managed in any practical, manufacturing way is of major concern to the microelectronics industry. The critical, or minimum dimensions in the interconnect, or "Back-End-Of (the) Line (BEOL)" technologies in manufacturing today are migrating from 180 nm to 130, 90, 65 and eventually 45 nm. The 90 nm node begins manufacturing in 2003, with each succeeding generation approximately 1.5-2 years following. Size-related resistivity issues have been observed as early as the 130 nm node, and are fairly visible in the 90 nm node. In the 45 nm node, if unsolved, resistivity increases due to size-related phenomena will cause an 100% or more increase in line resistance. If significant increases in sidewall roughness are also present in this generation due to the usage of porous, low-k dielectrics, the resistance increase in the metal lines may become quite significant.

A fundamental problem exists in measurements of Cu resistivity effects, a number of which have been carried out in the past several years. Due to the scattering nature of the resistance increase, each process (surface scattering, grain boundary scattering, roughness and impurities) adds essentially linearly to the net resistance. And with the exception of impurities, each of the processes scales as roughly 1/dimension. To further complicate things, with the exception of impurities, each effect is interrelated. For example, grain size usually scales with dimension.

Surface roughness is often, but not always, related to film thickness. It is difficult, then to decouple the net measurement, which is usually just a simple resistance, into each relevant phenomena. A number of experiments have been attempted to shed light on the significance of each parameter (1-5).

BACKGROUND

Each of the effects involved: electron-surface scattering, electron-grain boundary scattering, surface roughness enhanced scattering, and impurity scattering, have been addressed both theoretically and in many experiments. For completeness, we briefly summarize each area below.

[a] electron-surface scattering

In most metals outside of the nanometer realm, electron-surface interactions are proportionately rare. In pure, large grain materials, electrons move in the presence of weak potential gradients until typically a collision with a phonon occurs. At room temperature, for common metals such as Cu, W, and Al, the mean-free-path for this electron movement is a few tens of nanometers. At low temperatures, this path length increases due to the reduction in phonons, and the conductivity increases. When an electron reaches the edge or surface of the metal, it may undergo a scattering event. Depending on the nature of the surface, that event may be completely specular, in which case forward momentum is conserved, or partly-to-completely diffuse, in which the electron essentially stops and restarts in a random direction. Fully diffusive scattering results in the largest increase in resistance.

While there have been numerous studies on the mathematical form of the size effect, a recent model by Kuan et al (6) has proposed an approximate simplification. This model will later be extended to grain boundary and surface roughness effects as well. The form for the resistivity, ρ, of a metal in the size-effect regime is (6):

$$\rho/\rho_0 \approx 1 + 0.375\,(1-p)\,\lambda/d \qquad (1)$$

Where ρ_0 is the bulk resistance, λ is the electron mean-free-path (which is a function of temperature, but will be assumed to be constant for this approach), d is the thickness of the film and p is the scattering parameter, which varies from 1 for fully elastic or specular scattering to 0 for fully diffuse scattering. In this approximation, if the scattering is fully specular, the second term in Eqn. 1 is eliminated and there is no size dependence of the resistivity. For the case of a square line (which is the worst case), the numerical factor of 0.375 changes to 0.75, indicative of the increased number of surfaces for the electron to scatter from. A rectangular line will have a numerical factor between these two values based on the aspect ratio of the line.

As a function of dimension, the resistivity for Cu at room temperature is shown in Figure 1 for fully diffuse scattering (p = 0). Also shown in the figure are dotted lines indicating the critical dimensions for the various semiconductor nodes. These lines indicate the minimum dimension, which is usually a via diameter. The dimensions of the wires or trenches in each of these

generations is roughly the via dimension from the prior generation. For example, the trench width in the 45 nm generation will be roughly 65 nm.

Figure 1. Calculated Cu resistivity for film thicknesses in the range of the electron mean free path for the case of elastic scattering (p=1) and for diffuse scattering (p=0).
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[b] grain boundary scattering

The impact of grain size on electrical resistivity was first described in detail by Mayadas and Shatkes in 1970 (7). Effectively, each grain boundary functions as an internal surface for electron scattering with some probability of transmission or reflection from the interface. Much like the conventional size effect describe above, grain boundary scattering only becomes significant when the mean free path is similar to the dimensions of the grains. The model by Kuan et al approximates the effect of grain boundary scattering on resistivity as (6) :

$$\rho/\rho_0 \approx 1 + 1.5 \{R/(1-R)\} \lambda/g \qquad (2)$$

Where g is the average size of the grains, and the scattering coefficient, R, varies from 0 for no scattering (i.e, complete electron transmission) to 1.0 for complete scattering by the boundary.

For many metal thin films and structures, the grain size of the metal scales almost linearly with the film thickness or line width. Earlier scaling studies with Cu have suggested a value for R of approximately 0.3 (8). With these two approximations, the scaling of resistivity for Cu with dimension is shown in Figure 2. A second trace is also included for Figure 2 in which the grain size of the Cu is 5 times the film thickness.

Figure 2. The electrical resistivity of Cu as a function of film thickness due to the contribution of 'bulk' resistivity and grain boundary effects.

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[c] surface roughness induced scattering

In addition to the conventional specular-to-diffuse electron-surface scattering effect described above, there is a simple roughness-related aspect to the scattering. This is shown in Figure 3, in which an electron approaches a rough, undulated surface. At the impact point, (a), shown in the Figure, the electron scatters from a surface which is mostly pointed away from the initial direction of motion. The impact of this scattering event on the resistivity will be larger than from a purely horizontal surface. Because of the somewhat random nature of roughness in surfaces, a two dimensional Monte Carlo model has been developed by Inoki et al which follows a large number of electron trajectories through the film (6,9). This model uses a sinusoidal surface roughness with a constant wavelength and varying amplitude (Figure 4).

Figure 3. Sketch of electron motion approaching a rough surface.

Figure 4. Sketch of electron trajectories for a film with (a) a smooth upper surface, and (b) a sinusoidal upper surface with wavelength L.

In practical terms, it is very difficult to anticipate the exact level of surface roughness of a given film or line. For even the simplest cases of thin films in the 40-60 nm thickness range, the surface roughness can change significantly based on processing or annealing conditions, as seen in Figure 5. In the case of patterned lines which are inlaid in a dielectric layer using damascene processing, the sidewalls and bottom of the lines will be very susceptible to the reactive ion etching process and the mask used to define the trenches. Due to roughness at the mask edge, vertical striations on the sidewalls of trenches are very common, and these vertical, sidewall ridges can be many nanometers in height, extending in from the trench sidewall.

An estimate of the impact of surface roughness on electrical resistivity can be made using the Monte Carlo model and a simplified model for the surface roughness. As an example, the model was applied to a film with a sinusoidal surface roughness with a period of 20 nm. As a function of the amplitude of the surface roughness, the resistivity could be estimated, and this is shown in Figure 6.

Figure 5. TEM cross sections of 60 nm thick Cu films with 7 nm Ta layers above and below the Cu film. (top) 60 nm epitaxial Cu at 25C, (middle) deposition at 25C, (bottom) deposition at 25C, annealed at 400C.

Figure 6. Cu electrical resistivity of 20 and 60nm Cu films estimated using a 2 dimensional Monte Carlo model with a flat bottom surface and a sinusoidal top surface with a wavelength of 20 nm.

Following the earlier Kuan et al formalism (6), the surface roughness can be introduced into an equation for resistivity using a numerical factor, S, which is an empirical constant equal to or greater than 1.0 which multiplies the general surface scattering term in Eqn. (1).

$$\rho/\rho_0 \approx \{1 + 0.375\,(1-p)\,S\,\lambda/t + 1.5\,\{R/(1-R)\}\,\lambda/g\,\} \qquad (3)$$

The roughness factor, S, can be estimated from the Monte Carlo model, although there are many complications based on the simple premise of the model.

With some degree of caution, this model can be extended to surfaces with other ranges of surface roughness. For example, a regular roughness with a wavelength of significantly larger than the electron mean free path would have an S value much closer to 1.0 than the case cited here. What is probably most important to realize in this model is that it estimates the effect on only a single surface on the resistivity of a planar, 2-dimensional film. In a patterned line with 4 potentially

rough surfaces, the resistivity increases will scale up quite rapidly due to the roughness, regardless of whether the electron-surface interaction is specular or diffuse.

(d) impurities

The presence of an impurity atom in the Cu lattice can result in an electron scattering event. For dilute impurities, this has often been characterized as a proportional resistance increase per some unit of impurity level, such as part-per-million. For Cu, published values for the resistivity increase for impurities have been in the 0.xx micro-ohm-cm / ppm level (10,11). While many of the studies of this kind have been done in tools designed for surface analysis, it is instructive to gauge the effect of impurities in a manufacturing scale deposition system. Since the background gas composition at base pressure in most deposition systems is a strong function of the type of the pumping system (cryopump or turbo pump, for example) as well as the history of the chamber, it is hard to make a general conclusion of the impact on resistivity simply from the base pressure. As a rough gauge, however, measurements were made of the resistivity of Cu films deposited by sputtering with Ar (1 mTorr) in a commercial PVD tool (12) with a cryo-pumped chamber base pressure in the mid 10^{-8} Torr range, and then of additional samples deposited with the addition of oxygen up to the 0.1 mTorr range. The Cu target in this case had a purity of 99.99999% (7-9's), the argon purity was 99.9999% (6-9's), and samples were degassed and introduced through a loadlock (Figure 7).

Figure 7. Sheet resistance of 50 nm Cu films deposited by Ar sputtering at 1 mTorr as a function of the pressure of oxygen introduced into the chamber during deposition. The Cu deposition rate was 25 nm/min.

While the effect of impurity incorporation in Cu can be significant, it appears that depositions at or near the base pressure of this PVD system will have minimal impact on the resistivity.

THICKNESS-RELATED RESISTIVITY EXPERIMENTS

Numerous groups have measured the resistivity of Cu films and lines in the sub-100 nm size regime (1-5, 13,14). Without exception, each measurement shows strong increases in the resistivity with decreasing thickness. The general difficulty, though, with many of these measurements is decoupling the relevant, underlying effects from the net resistance measurement. This difficulty is due to the coupled nature of the thickness, grain boundary dimensions, surface roughness and composition, and the time-dependant nature of the grain size. In this latter area, multiple studies over the past 7 years have observed and quantified a fairly rapid (hours-to-days) grain growth process for Cu which occurs at room temperature (15-16). In thicker films, this effect can lead to resistance changes of -25% or more, and the effect is strongly dependant on deposition conditions, temperature, and the nature of the Cu-to-substrate bonding. While this is an interesting phenomena to consider and has implications for manufacturing process integration, for any sort of resistivity study it requires that virtually all polycrystalline Cu films be exposed to elevated temperature (300-400C) in a controlled environment either during or after deposition to reach the stable, terminal grain size condition.

Even after annealing of the Cu films, the grain sizes in the resultant films are not much different than the film thickness. While this is clearly visible with techniques such as FIB or XRD, it is also functionally apparent in the measurement of the film resistivity, which remains well above bulk values even for film thicknesses much greater than the electron mean-free-path (Fig. 8). TEM analysis also shows a high dislocation density in these PVD films which contributes as well to the elevated resistivity and does not scale with thickness.

As a parallel to this observation in planar films, it is also possible to observe the grain size distribution in patterned lines. Due to the grain growth phenomena observed with electroplated Cu films, it has become a common manufacturing process to anneal the electroplated Cu films prior to polishing back with Chemical-Mechanical-Polishing (CMP). This allows significant grain growth from the thick planar films above the patterned wafer down into the trenches and vias on the wafer surface, and the resulting grain size can equal or exceed the dimensions of the trench or via. This is often described as 'bamboo structure,' even though there does not appear to be the same preferred orientation and regular structure which was observed routinely with patterned Al(Cu) lines many years ago.

As the dimensions of the Cu lines decrease to the sub-100 nm range, it has been reported that this grain growth process does not occur nearly as readily as with larger features (14,14b). In the current study, lines of 60 nm width and low aspect ratio were deposited by conventional seeding, electroplating, annealing and polishing. Observations of the apparent grain size using Focused Ion Beam (FIB) analysis (Fig. 9) appear to confirm the earlier observations: the grain size of the lines is at or below the line width. This will cause a significant increase in the net line resistance which is larger than what would be expected by scaling alone.

Figure 8. Electrical resistivity of Cu films as a function of film thickness deposited on silicon dioxide samples (with a 2 nm Ta adhesion layer) following annealing at 400C for one hour in forming gas (nitrogen plus 5% hydrogen).

Figure 9. Focused Ion Beam (FIB) images of 60 nm Cu lines deposited by conventional PVD seeding, electroplating, annealing and polishing.

In the interest of examining surface-related effects on resistivity in the thickness regime near the electron mean free path, one solution to the elevated electrical resistance due to the multiple grain boundaries is to eliminate or at least significantly reduce the number of grain boundaries in the film. Cu epitaxy has been long understood (17,18), and this generally requires the use of highly oriented sapphire or MgO substrates and elevated deposition temperature (400C). Earlier work with epitaxial Cu films did show significant reductions in the electrical resistivity (6).

In the current study, we have chosen to examine an alternate path to highly oriented, large grain size Cu films which is more consistent with manufacturing-scale PVD deposition systems. In work first reported by Chang (19) and others (19a-c), there is a near lattice match (6% off) between the Si (110) and 2 times the Cu (100) planes. The Si(110) plane is accessible on a cleaned Si (100) wafer. Depositions were undertaken with PVD Cu onto Si samples which were

etched immediately prior to introduction into the vacuum system by immersion in a dilute HF solution, followed by a drying with clean nitrogen gas (but with no water rinse). This cleaning step leaves the Si surface oxide free and hydrogen-terminated, which precludes any additional oxidation for a few minutes upon air exposure; long enough to evacuate the sample in a loadlock.

In an unusual aspect of this pseudo-epitaxial deposition sequence, the magnetron sputter deposition onto the cleaned Si surface was done at room temperature. Cu and Si will form a compound (CuSi2) at roughly 220-240C. Therefore, wafer samples were clamped onto water-cooled chucks and the deposition process time was kept to a minimum to reduce sample heating. TEM studies of the resultant films show a high degree of orientation and are consistent with a grain size 5-10x the film thickness. (Fig. 10)

Figure 10.   TEM cross-section and electron diffraction trace of the same Cu(100) film deposited on Si(100).

The electrical resistivity of these films can be readily measured, although it must be corrected in some cases for the contribution of the semi-conducting Si substrate which forms a Schottkey barrier at the Cu-Si interface. When compared to the above-described case of post-annealed Cu, the resistivity of these films as-deposited was significantly lower, although not as low as the predicted value for the size-effect-altered resistivity. (Fig. 11) In addition, the film resistivity was stable with time following deposition, indicating that no additional grain growth was occurring. This eliminates the need for annealing. The films were also relatively stable in air and showed only minor increases in resistivity, nominally due to surface oxidation of the Cu, over periods of many days. The dislocation density in the films is qualitatively lower as well, and one indication of this is that the thick-film resistivity values approach the bulk Cu value, which is quite unusual for sputter-deposited films, and even more striking because these films have never been annealed above 25C.

Figure 11.   Electrical resistivity as a function of film thickness for Cu films deposited on SiO_2 (post-annealed) and near-epitaxial Cu (100) films deposited on HF-cleaned Si(100.

The surface roughness of these pseudo-epitaxial Cu films was measured with AFM and compared to films deposited in a non-epitaxial condition, such as on SiO_2 or an adhesion layer of Ta. The r.m.s. roughness of 45 nm pseudo-epitaxial films was at the signal-to-noise limit of the AFM tool, which is 0.1 to 0.2nm. Cu films deposited on silicon dioxide, but not annealed, showed a roughness of 2x higher.

The resultant incremental resistivity of these Cu(100) thin films above bulk values at thicknesses on the order of the electron mean free path is due mostly to the residual grain boundaries as well as non-specular electron-surface scattering. The effect of surface roughness is relatively low (a few %) based on extension of the Monte Carlo model results to the measured surface roughness.

The measured value at a film thickness of 45 nm is 3.0 micro-ohm-cm, or 78% above the bulk value. Roughly half of this increase can be attributed to grain boundary scattering with grain sizes of 220-250 nm, which is consistent with experimental measurements. Most of the rest of the observed increase (over large-dimension bulk Cu) is due to non-specular surface scattering events. However, it is not possible using this simple approach to directly determine the surface scattering parameter, p.

ALTERATION OF SURFACE SCATTERING PROCESS

The key to addressing whether there is a solution to size-related resistance effects for metals such as Cu is clearly at the surface of the Cu film. A phenomenological approach to this problem has been suggested by Egelhoff, who has related the degree of scattering to the change in the Fermi surface for electrons in the near-surface region (20). The Fermi surface will be sensitive to any roughness at the surface, even at the atomic scale. It will also be perturbed by the presence of other atoms at the surface, particularly metallic atoms of other species. The level of non-specular scattering of electrons from the surface will relate essentially to the level of opportunities for the electrons to scatter to alternate surfaces (20).

Following this phenomenological approach, it is instructive to consider several different conditions. The simplest is that of a perfect single crystal of Cu, which has an ideal planar surface, held in vacuum. The Fermi surface will be perturbed at the Cu-vacuum interface since the density of atoms (and electrons) will rapidly drop to zero. Some measurements of Cu whiskers, which nominally are single crystal with fairly smooth surfaces, have suggested a scattering parameter of 0.6.(21)

Another relatively simple interface could be a simple grain boundary separating two Cu grains which were each much larger than the electron mean free path. As the electrons approach this interface, the Fermi surface on each side of the interface is mostly the same since there is a large degree of symmetry in the Cu Fermi surface. Aside from the perturbation of the Fermi surface caused by the atomic roughness of the grain boundary, there should be a fairly low level of diffuse scattering in this case. Following the model of Mayadas and Shatzkes, and experimental results of reflection parameter, R, in the range of 0.3, this suggests a level of diffuse scattering due mostly to atomic-scale roughness consistent with a scattering parameter, p, of 0.7.

In real world applications, however, Cu surfaces must touch surfaces of other materials. For electromigration resistance, it has been found that a metal such as Ta provides a strong bonding to the Cu surface which limits the surface mobility of Cu atoms and reduces electromigration problems. Surfaces such as dielectrics (silicon dioxide, for example) bond poorly to Cu and result in significant levels of electromigration. Due to the complicated nature of the Ta Fermi surface, it has been predicted that the Cu-Ta interface should enhance diffuse electron scattering (20).

Experiments were undertaken with nominally epitaxial, large-grain Cu films at thicknesses of 20-45 nm, which are in the thickness regime where the size effect is quite significant. Following deposition of the Cu films (at 25C onto HF-cleaned, H-terminated Si), subsequent films of Ta were deposited in-situ. This allows examination of the top surface only, and there are no changes

to either the bottom surface or the grain size of the Cu film. All films were deposited by magnetron sputter deposition in production-scale deposition chambers. As shown in Fig. 12, the sheet resistance of the Cu films was increased by up to 10% by the addition of a few nm of Ta to the upper Cu surface.

Figure 12. Sheet resistance of 45 nm Cu film as a function of Ta overlayer thickness

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Following deposition, however, when the samples were exposed to air the sheet resistance dropped on the order of minutes to hours to the approximate value of the Cu films with no Ta overlayer or perhaps slightly less (Fig. 13).

Figure 13. Sheet resistance of 45 nm Cu films as a function of time (in air) for cases of 0.3, 0.5, 0.8 and 1 nm Ta overlayers. The dotted line is the average of 10 similar Cu-only samples.

The time required for resistance reduction back to the average, uncoated value was dependant on the thickness of the Ta overlayer. This suggests that the Ta film is oxidizing, and the thinner films simply react to completion more rapidly than the thick films. Films of tantalum oxide on Cu would be expected to have little impact on the film resistivity due to the lack of a Fermi surface to facilitate scattering, consistent with earlier predictions (20). As a control, companion film samples stored in vacuum showed the same increases in sheet resistance due to Ta deposition, but did not change with time following deposition. Upon subsequent air exposure, these films showed a similar time dependence to the resistance reduction due to oxidation.

Overlayers of other high atomic weight materials which were also oxidizeable showed similar effects. In the case of a non-oxidizing metal, such as Pt, the effects were different. The resistivity increased for a few nm Pt overlayer, but eventually decreased for very thick layers (Fig. 14). The samples were stable in air. The increase is likely to be due to surface scattering or else interdiffusion into the Cu and subsequent impurity scattering, and the eventual decrease for very thick films is due to the conductivity of the Pt layer, which is in parallel with the Cu layer. The Ta films, which were beta-Ta with a resistivity of 250 micro-ohm-cm, were much too resistive to show this decrease due to parallel resistance effects.

Figure 14. Resistivity of 45 nm Cu film as a function of Pt overlayer thickness.

When Al was used as the overlayer, the films showed apparent decreases from the uncoated Cu case. As shown in Figure 15, overlayers of 0.4 to 1 nm of Al tended to result in time-dependant decreases in the sheet resistance. Much like the Ta case, the thicker films took a longer time to oxidize. For the thinner films, it appears that simply the time taken to remove the vent the sample from the vacuum chamber and make a resistance measurement (a few seconds) allowed partial oxidation of the films. However, in each case up to 1 nm of Al, the net result was a reduction in the resistance from the average, uncoated Cu value.

Figure 15. Resistivity of Cu films as a function of exposure time in air for various Al overlayer depositions.

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Experiments were also performed to examine the influence of surfactant-like layers which have been explored in relation to giant magneto-resistance structures (22,23). The role of the surfactant is to reduce surface roughness during deposition of the Cu. Using a silicon dioxide substrate (in place of the HF-cleaned, H-terminated Si), a thin, 1 nm Au layer was deposited by evaporation. Following the Au, Cu was deposited at a sample temperature of 250 C. The resistivity of the resultant films was lower than pure Cu at similar thicknesses (Fig. 16). However, subsequent AFM measurements of the films showed increased surface roughness and significant agglomeration of the Cu films. Surface chemical analysis (XPS) showed Au at the film surface at a higher level than expected due to simple dilution in the bulk of the films. Since the Fermi surface of Au is very similar to that of Cu, it is likely that the increased resistivity due to the surface roughness is countered by an increase in the specular electron scattering at the Cu-Au surface.

Figure 16. Cu film resistivity as a function of film thickness for the case of pure Cu (post annealed) and Cu deposited at 250C over 1 nm of Au. All depositions were on thick silicon dioxide layers.

DISCUSSION

Ideally, this experimental approach should avoid a number of the complications of making estimates of the scope of surface scattering. By using large grain, highly oriented and nearly epitaxial Cu films, concern over grain boundary scattering is reduced. In addition, the stability of these films is high, such that the measured resistivity only drifts by a 0.1 to 0.2% over several days, possibly due to oxidation. This stability avoids concerns over time-dependant grain growth which is present in many Cu experiments. The surface smoothness is these Cu films is also very good, essentially at the signal-to-noise limit of the AFM.

The use of a layer on top of the Cu film, instead of underneath, precludes any microstructural dependence of the Cu film on the material chosen. Obviously, in any real application of the Cu films this would not be feasible. The use of planar, unpatterned films is both an advantage and a disadvantage. Geometrically, it makes analysis of the results more straightforward. However, it does not begin to answer questions about structures fabricated at the same sub-100nm scale, which will need to be addressed for practical applications in interconnects.

The key issue for this set of experiments is whether the electron-surface scattering process in Cu can be altered experimentally, ideally to make the scattering more specular and hence reduce resistivity increases in metal interconnects as the dimensions approach the electron mean free

path. In this experiment, however, it is still necessary to decouple surface scattering issues from other phenomena, such as grain boundary scattering and surface roughness.

At a Cu film thickness of 40-45 nm, the average resistivity of the bare, epitaxial Cu films was 2.9 micro-ohm-cm, 70% above the bulk value. For these films, measurements of the grain size indicated an average lateral dimension for the Cu grains of 200-220 nm. Using Eqn. (2), (with R = 0.3) this accounts for a 40% increase in resistivity. The surface roughness measured by AFM was 0.14 nm, which suggests a minor geometrical contribution, if any, to the resistivity.

Taking these two parameters into account, and assuming the remaining resistivity increase is due to surface scattering from both the top and bottom of the film leads to a value from Eqn (3) of p = 0.12. When Ta or Pt is deposited on the Cu surface, this value for p drops to closer to 0, although the current formalism is too vague to take this argument much farther. The value of p = 0.12 is consistent, though, with the increase in resistivity of 10% or so which is seen with the Pt or Ta overlayers, which are thought to maximize the level of electron scattering, resulting in $p \approx 0$. The relaxation of the Ta-coated Cu resistivity back to the uncovered level as the Ta oxidizes is also consistent with a reduction in the electron scattering caused by the complex Ta Fermi surface which is eliminated as the Ta coverts into Ta_2O_5.

CONCLUSION

The resistivity of Cu has been shown to be sensitive to a range of effects in the thickness range near the electron mean free path, including electron-surface scattering, grain boundary scattering and surface roughness. The presence of other metals on the Cu surface generally leads to an increase in the resistivity of the Cu, although this increase may relax with time as the metal oxidizes. This increase is thought to be due to increased electron scattering from the more-complex Fermi surface of the overlayer. In the case of Al overlayers, preliminary results suggest a slight reduction in resistivity following oxidation of the Al.

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Figure 1. Calculated Cu resistivity for film thicknesses in the range of the electron mean free path for the case of elastic scattering (p =1) and for diffuse scattering (p=0). The interconnect nodes are shown as dotted lines.

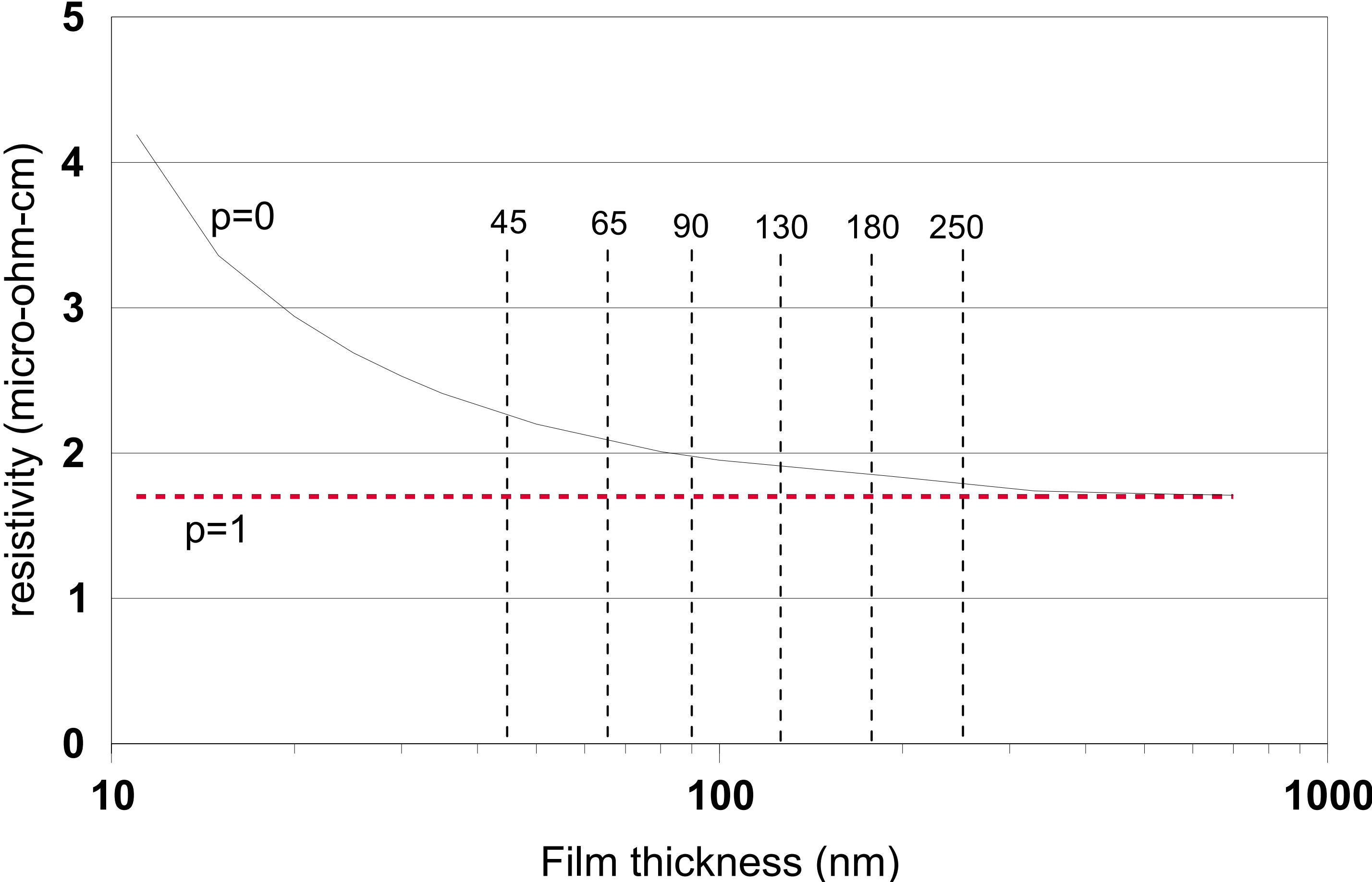


Figure 2. Calculated Cu resistivity due to grain boundary scattering. The interconnect nodes are shown as dotted lines.

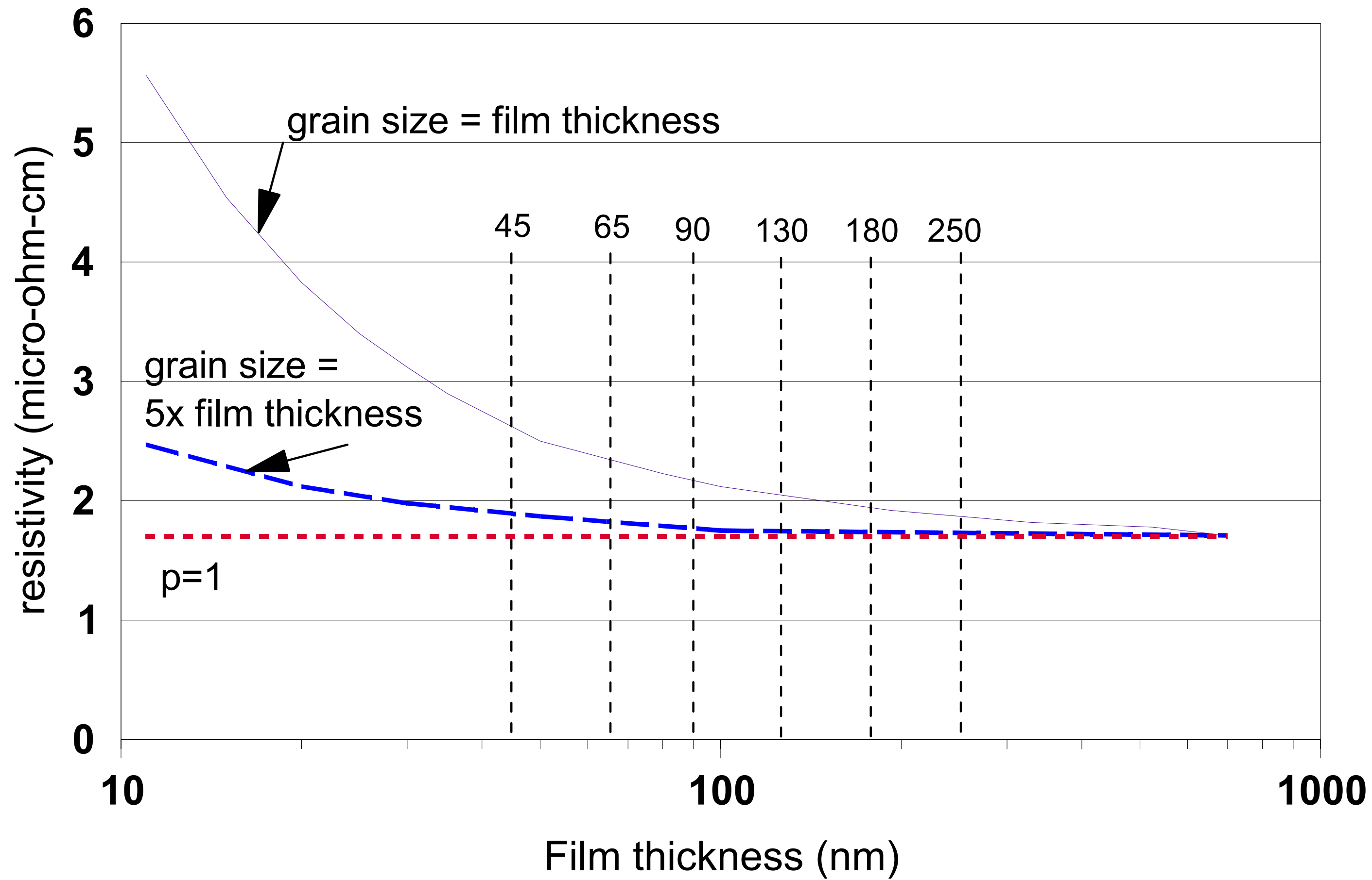


Figure 3. Sketch of electron motion approaching a rough surface.

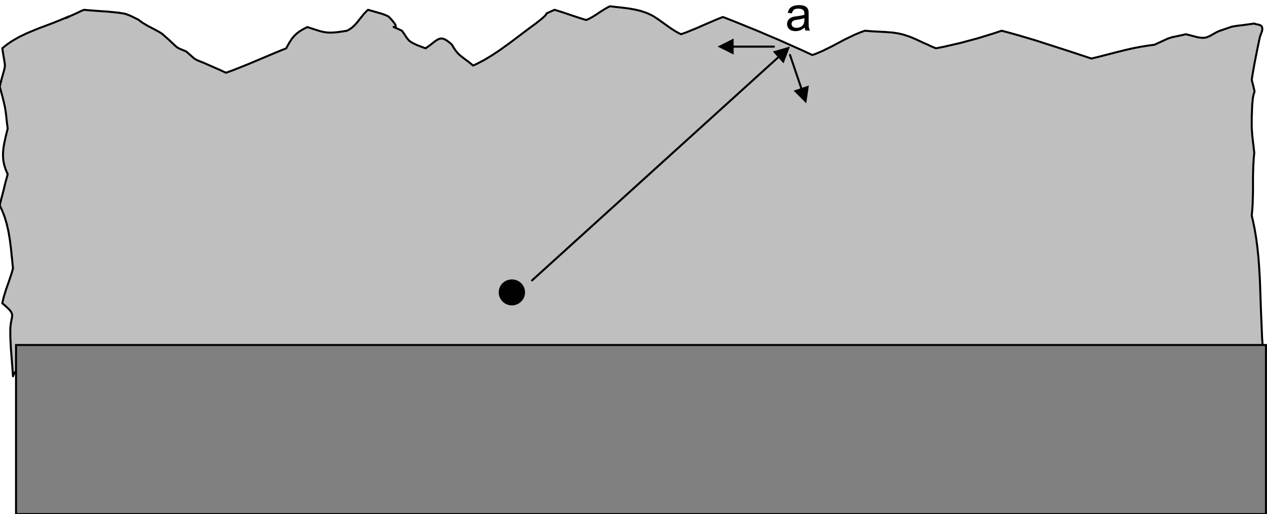


Figure 4. Sketch of electron trajectories predicted from the Montel Carlo model for films with (upper) a smooth upper surface, and (lower) a sinusoidal upper surface with a wavelength of 20 nm.

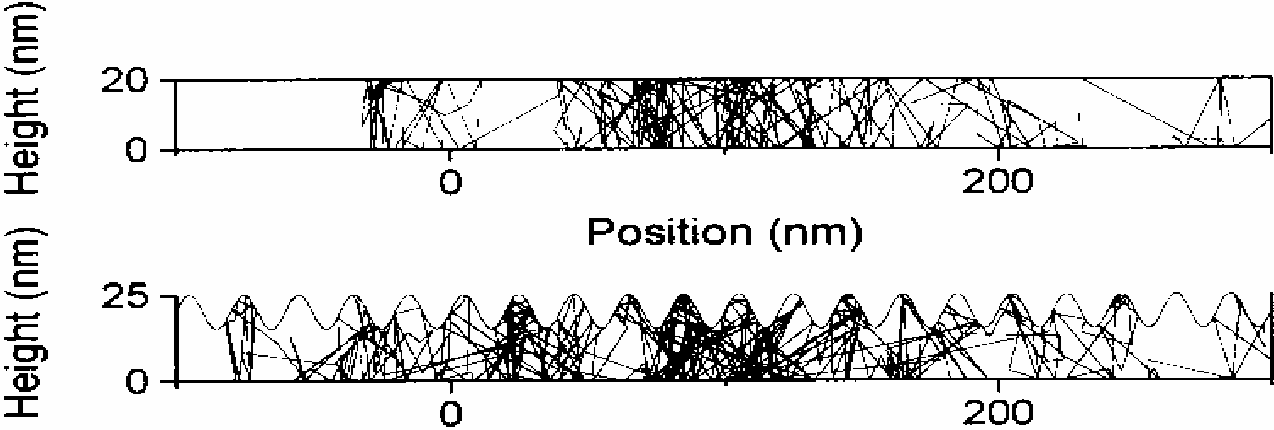
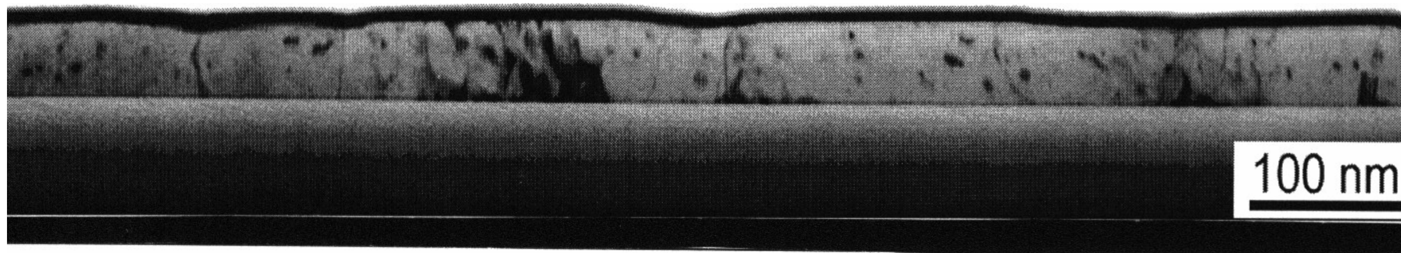
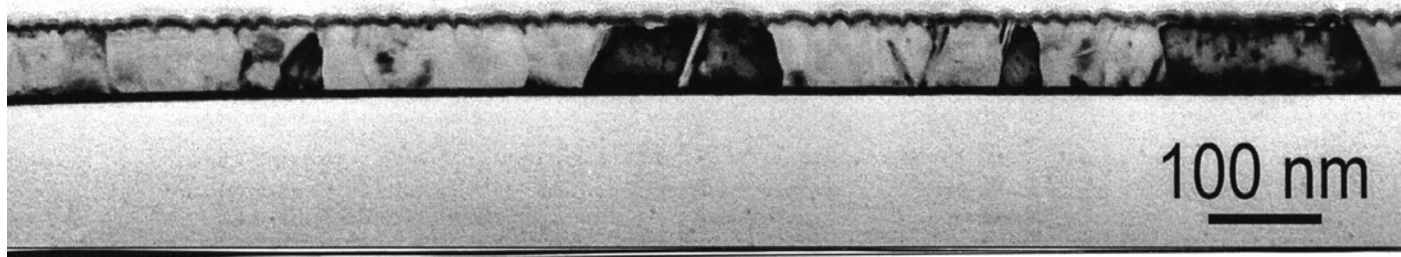


Figure 5 TEM cross-sections of Cu films: (top) 60 nm epitaxial Cu, (middle) 60 nm Cu deposited at 25C, (bottom) 80 nm Cu deposited at 25C, annealed at 400C.





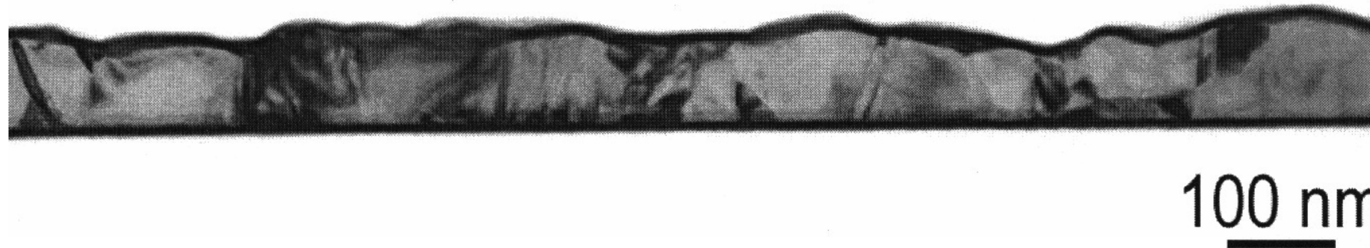


Figure 6 Cu electrical resistivity predicted by the Monte Carlo model (6) for a 20nm and 60 nm thick Cu film with a surface roughness period of 20 nm as a function of the amplitude of the surface roughness.

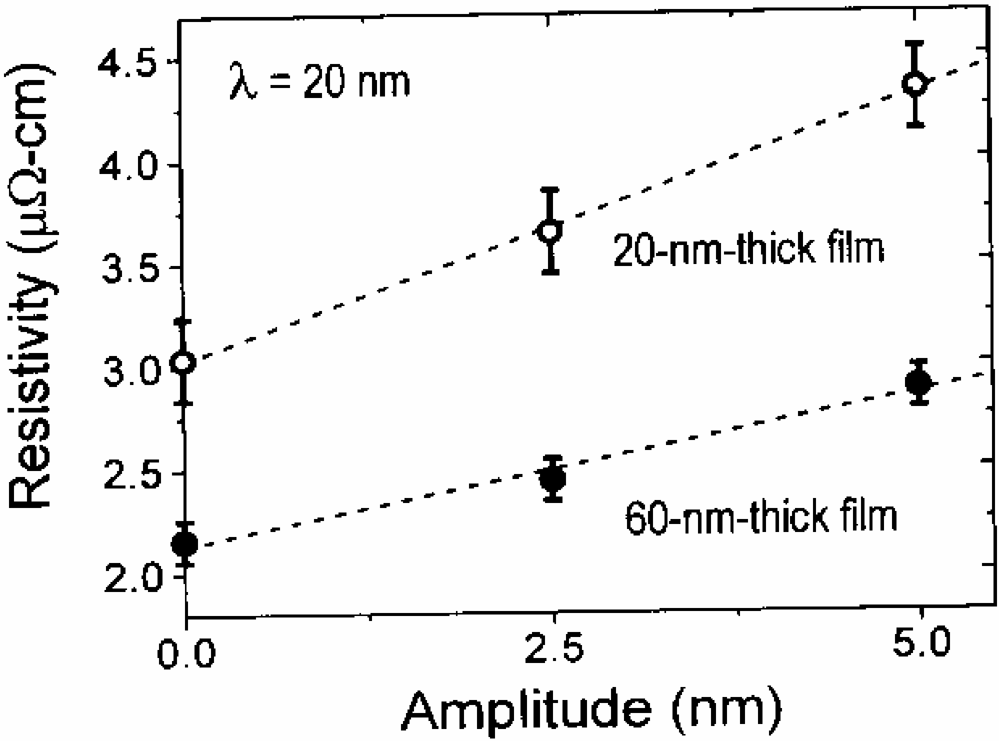


Figure 7. Sheet resistance of 100 nm Cu films deposited by Ar sputtering at 1 mTorr as a function of oxygen pressure introduced into the chamber during deposition. The Cu deposition rate was 25 nm/min.

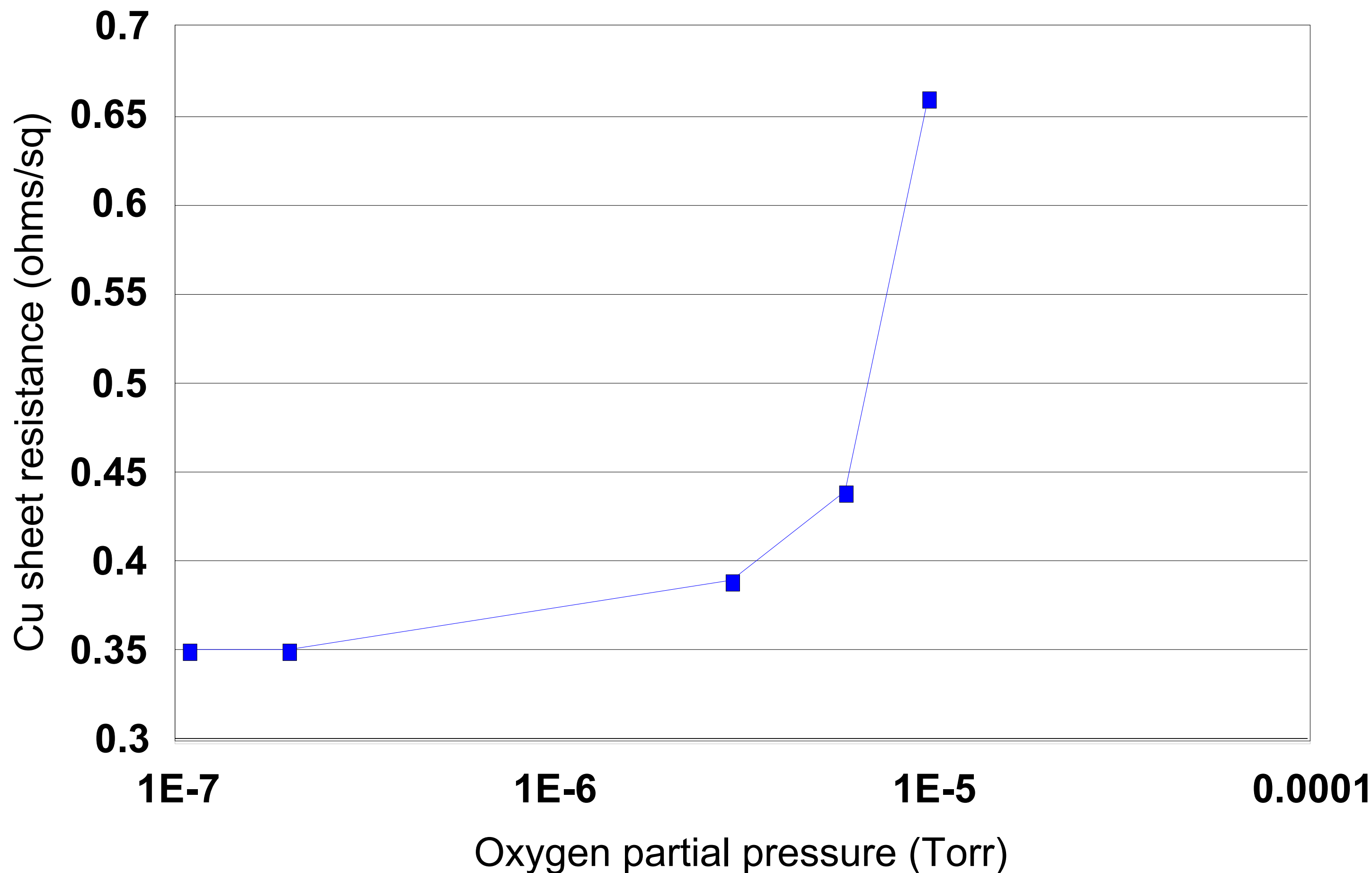


Figure 8. Electrical resistivity of Cu films as a function of film thickness for films deposited on SiO_2 (with a 2 nm Ta adhesion layer) following annealing at 400C for one hour in nitrogen and hydrogen (forming gas).

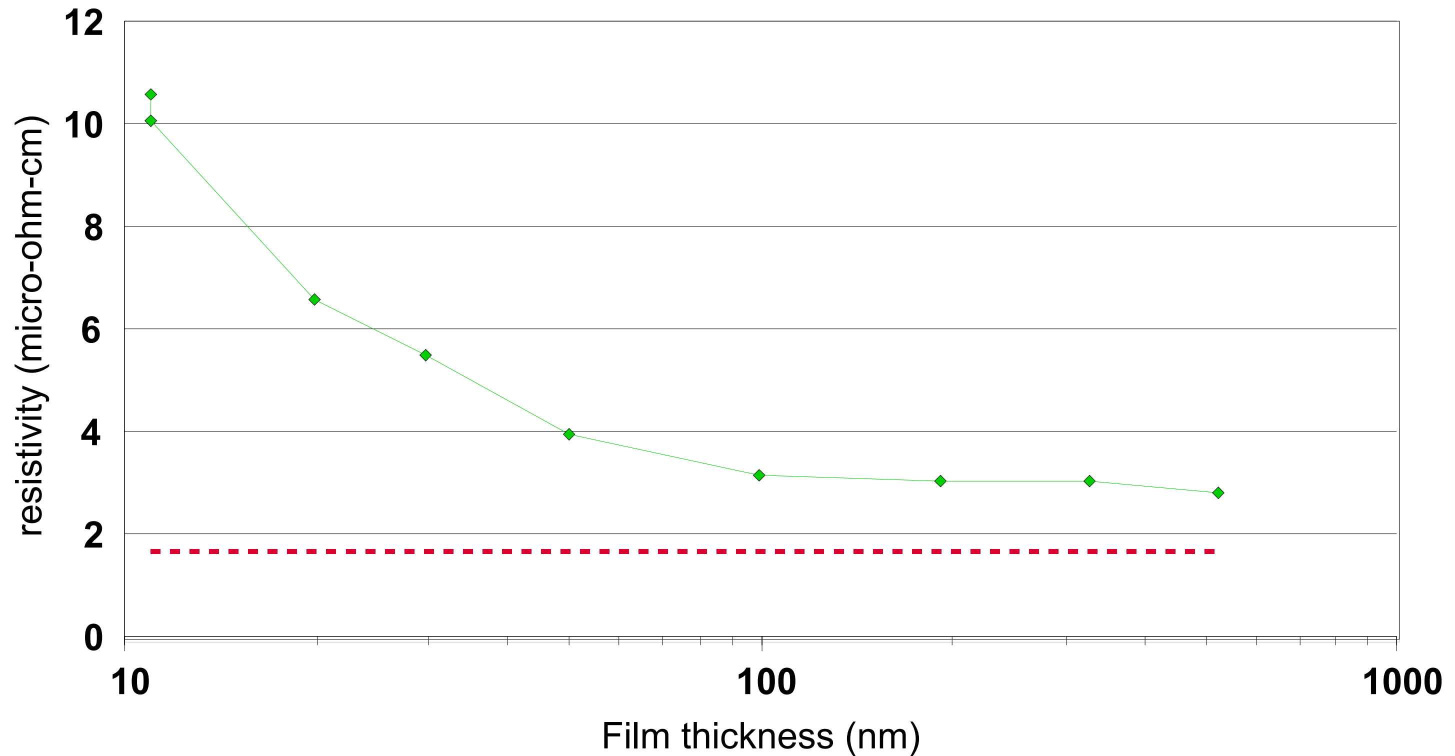
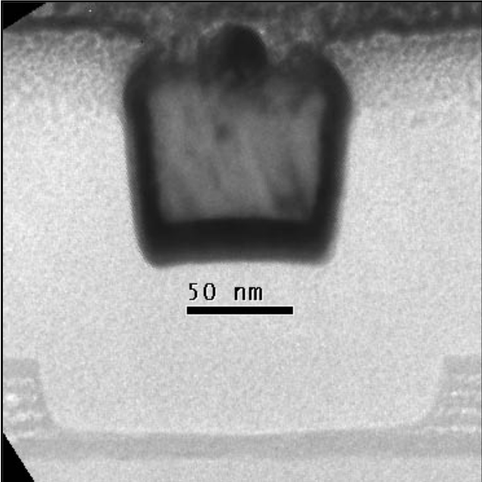
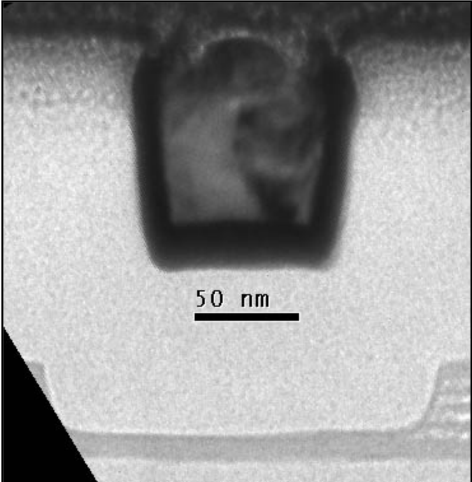
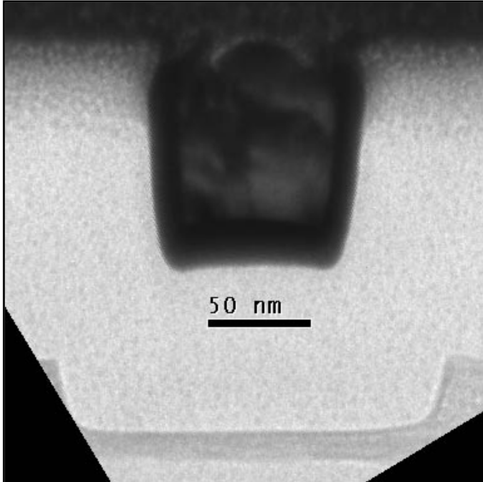


Figure 9. FIB images of 65 nm wide Cu lines: top photos are cross-sections, bottom photo is along line







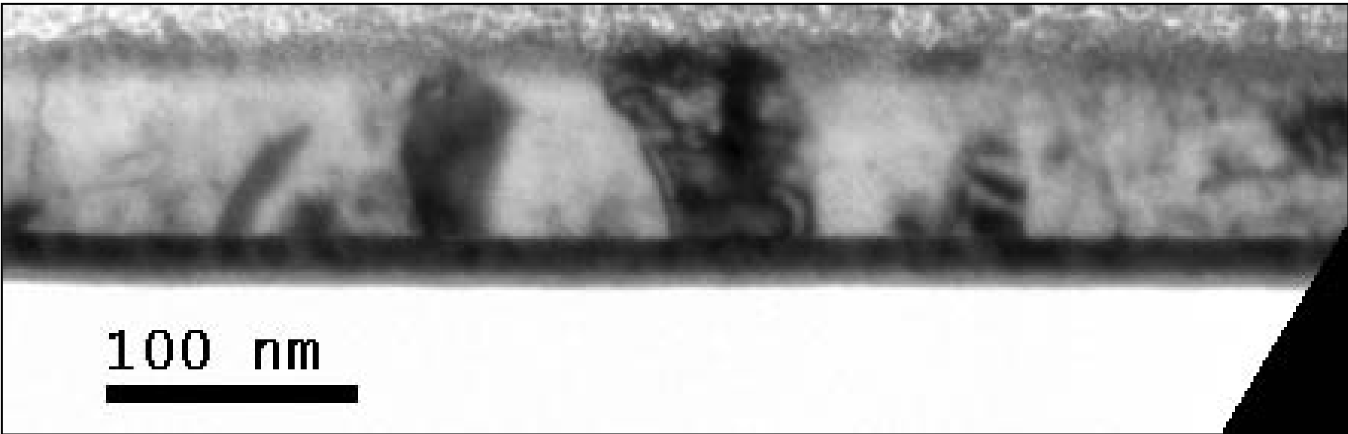
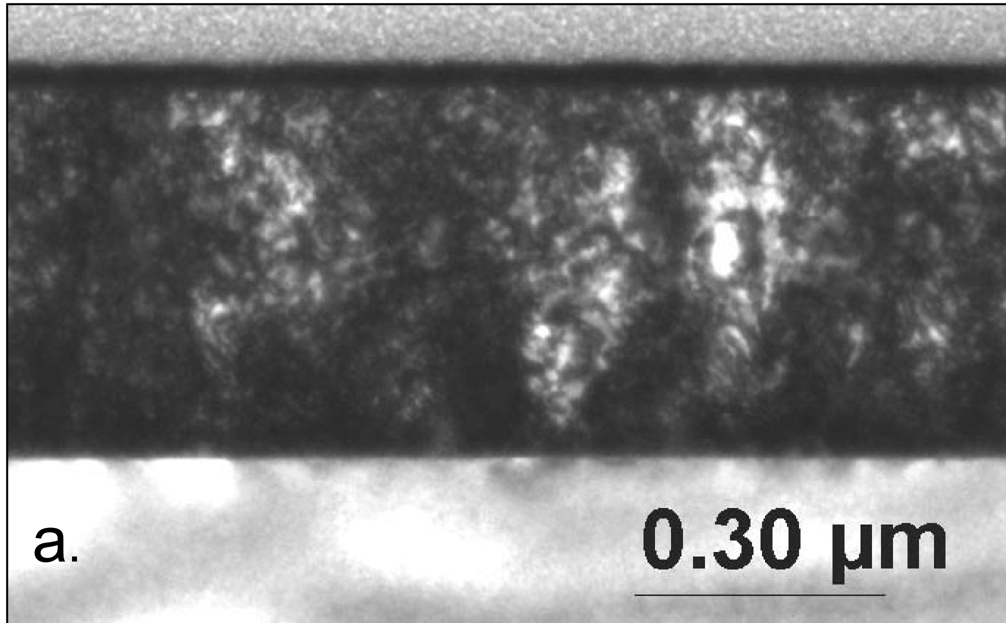


Figure 10 (a) TEM cross section and (b) electron diffraction trace of Cu(100) film deposited on HF-cleaned Si(100).



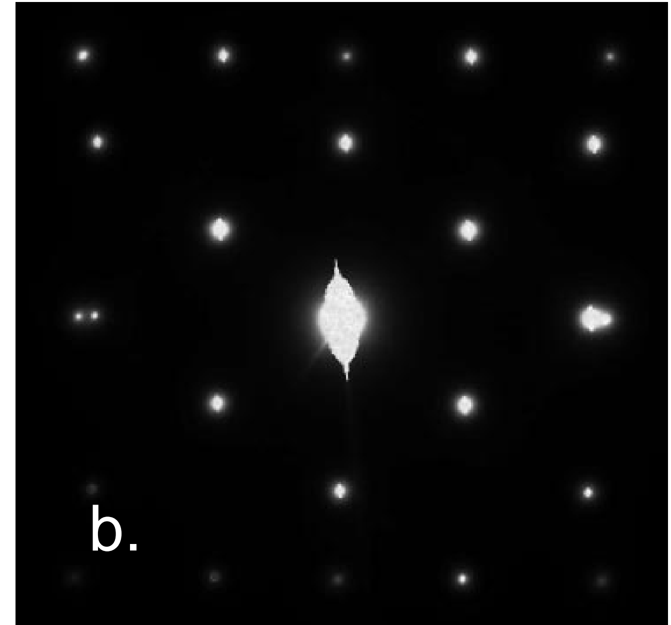


Figure 11. Electrical resistivity as a function of film thickness for Cu films deposited On SiO_2 (post annealed) and near epitaxial Cu(100) films deposited on HF-cleaned Si(100).

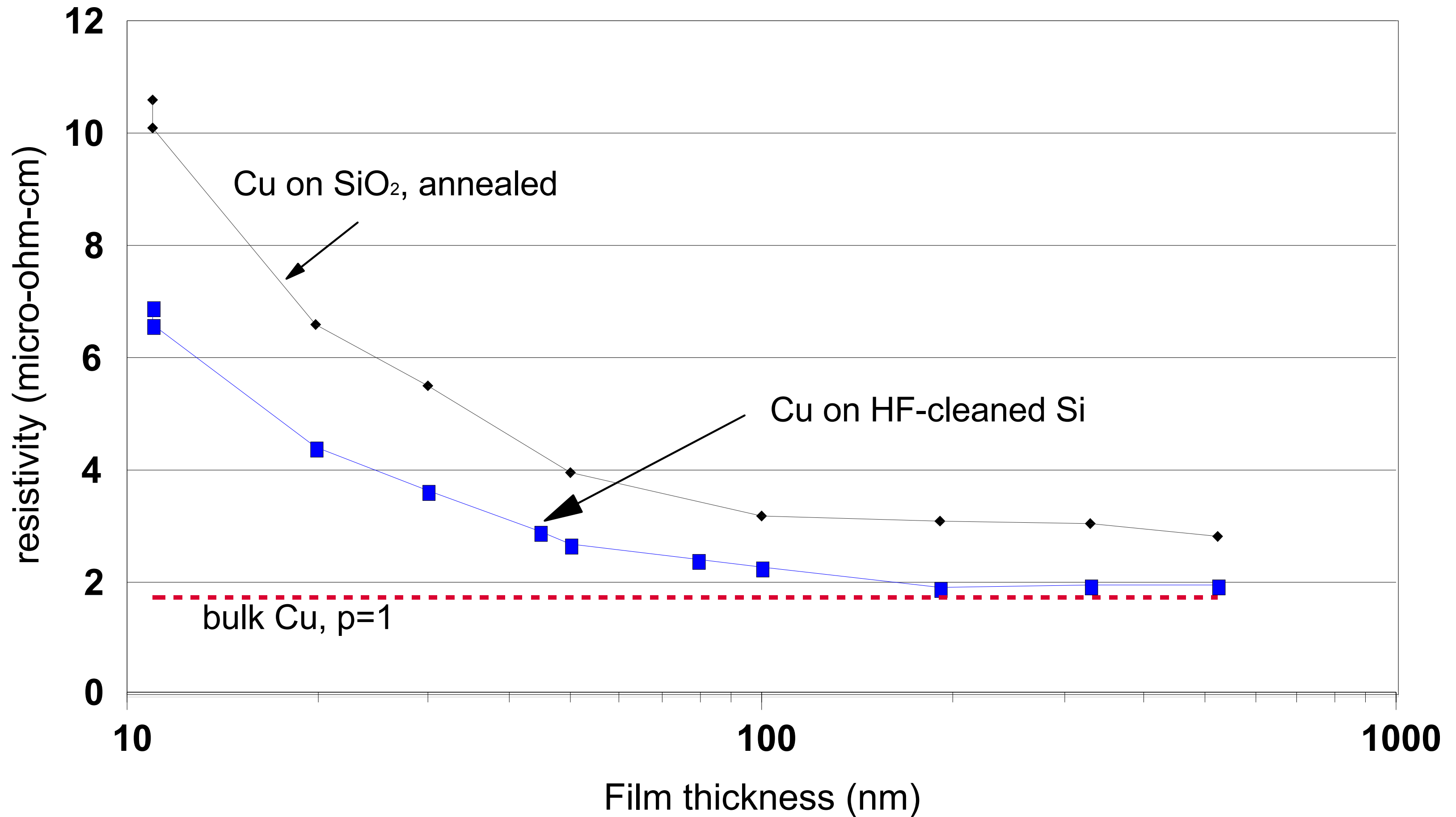


Figure 12. Sheet resistance of 45 nm Cu film as a function of Ta overlayer thickness

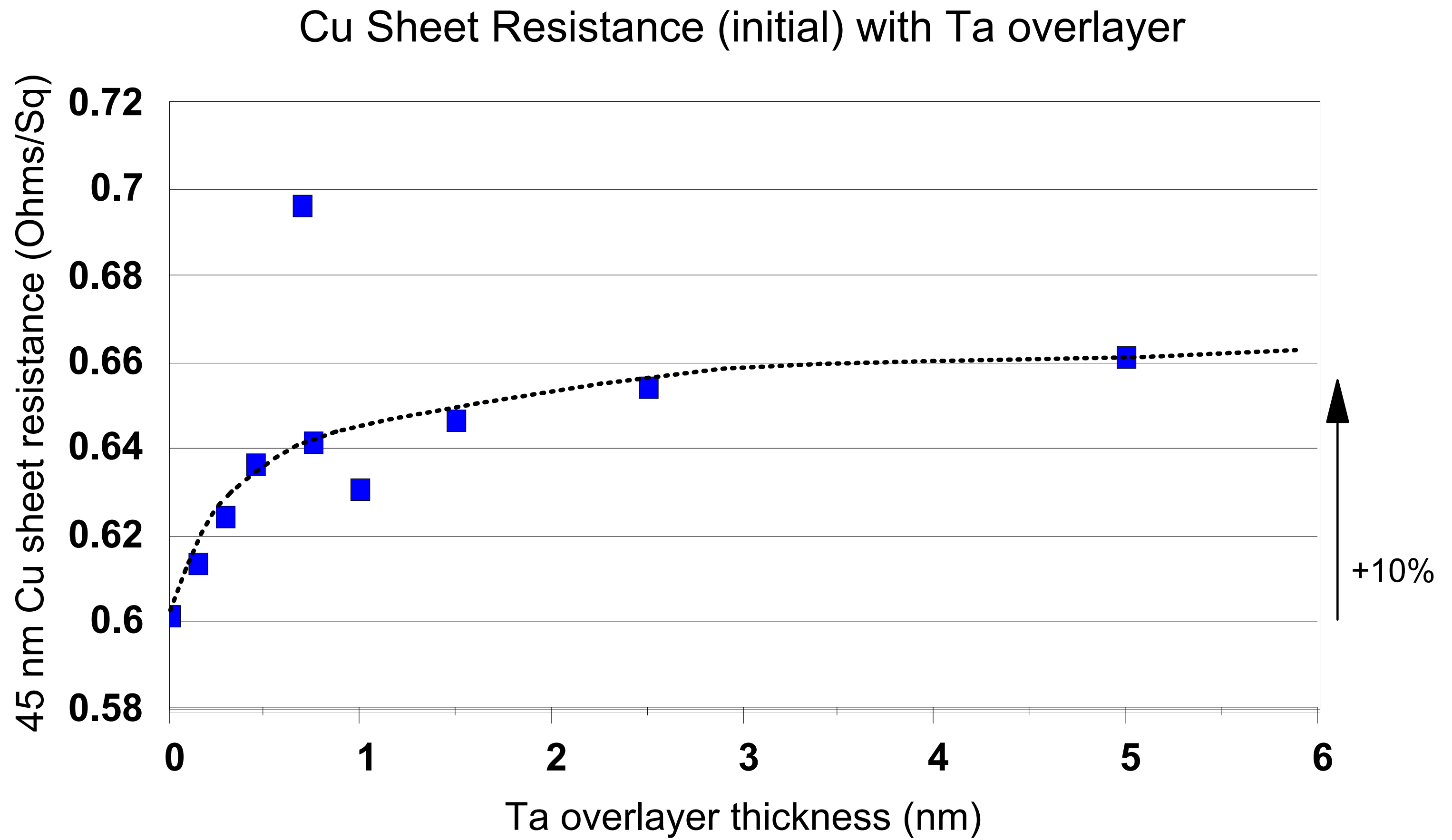


Figure 13. Sheet resistance of 45 nm Cu films as a function of time for Cu films with Ta overlayers.

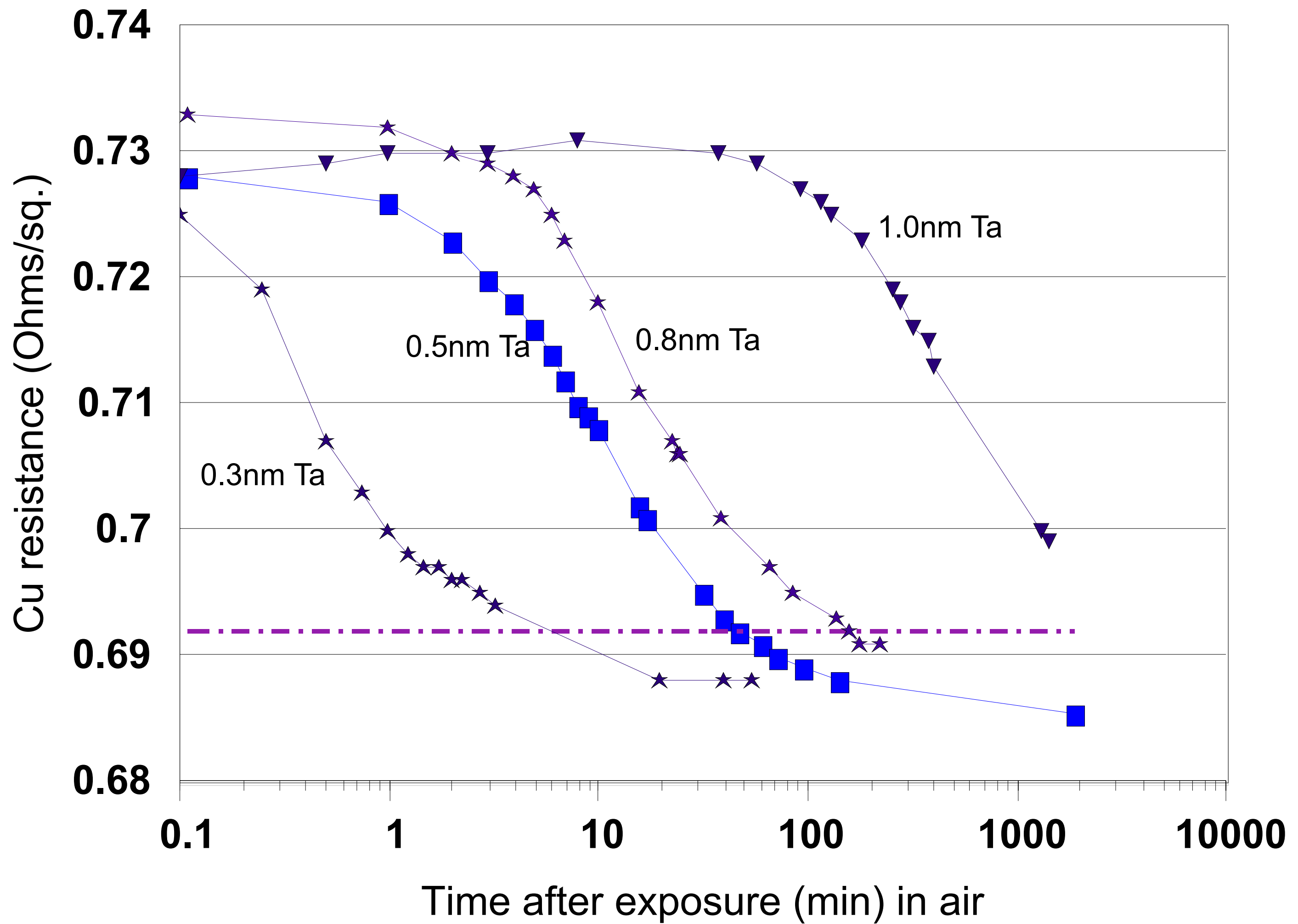


Figure 14. Sheet resistance of Cu films with Pt overlayers

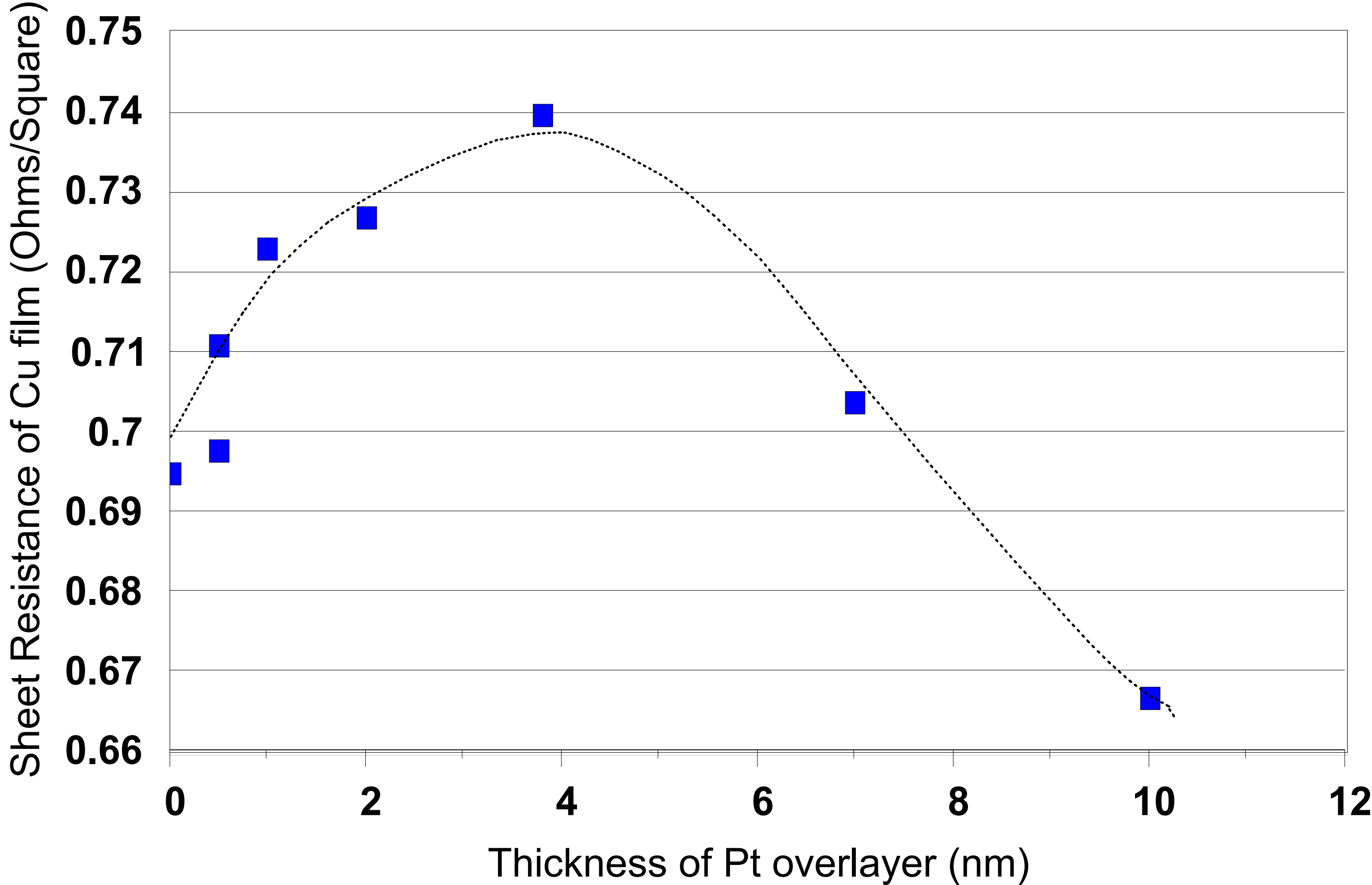


Figure 15. Sheet resistance of 40 nm Cu films as a function of exposure time in air for various thickness Al overlayers.

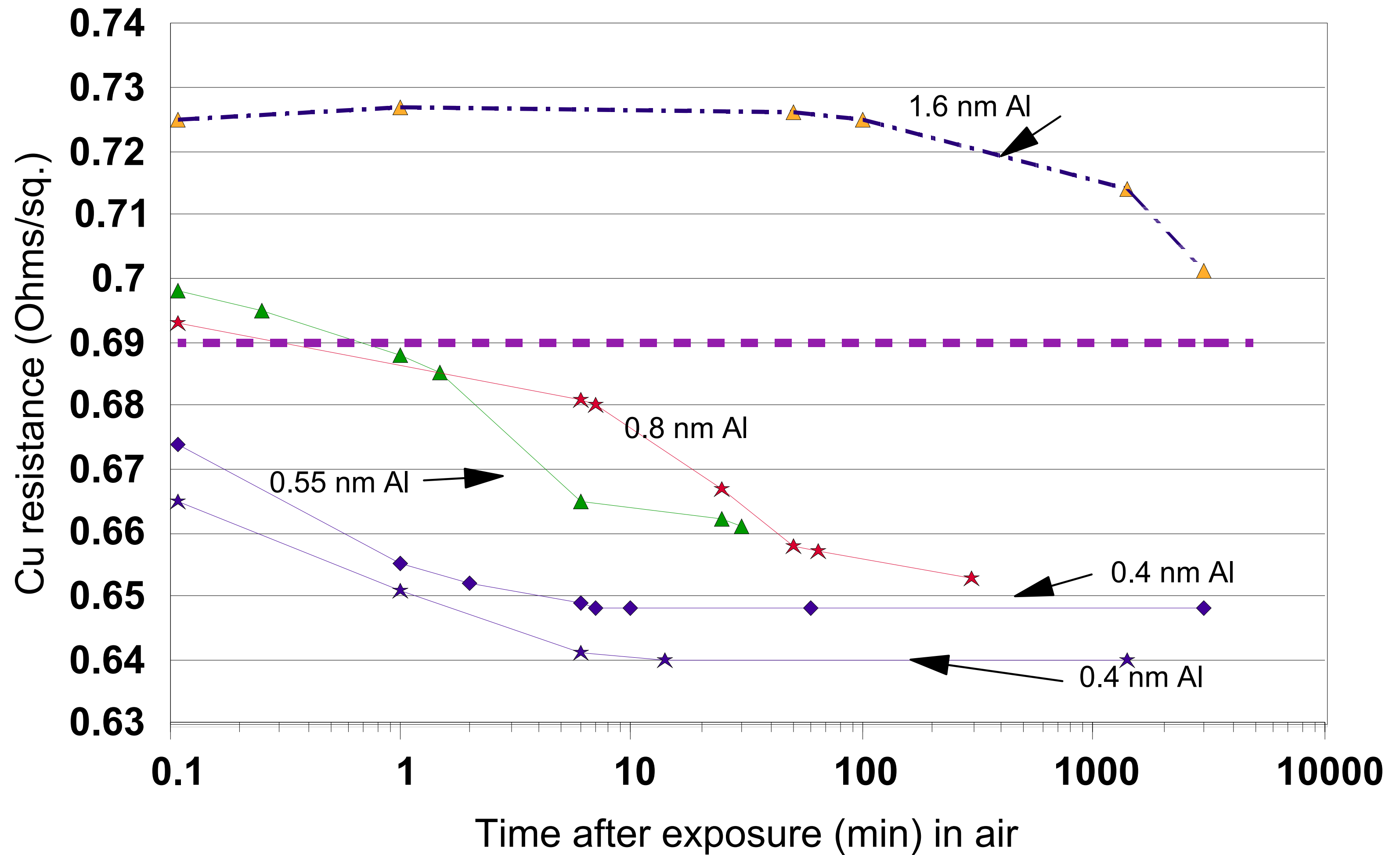


Figure 16. Cu film resistivity as a function of film thickness for Cu films deposited on 1 nm Au underlayer (at 250C) and for Cu on SiO_2, post-annealed to 400C.