RC23018 (W0311-164) November 24, 2003
Physics

IBM Research Report

Reliability of MOS Devices with Tungsten Gates

F. Palumbo, S. Lombardo
CNR-IMM
Sezione di Catania
Stradale Primosole, 50
95121 Catania
Italy

J. H. Stathis, V. Narayanan, R. McFeely, J. J. Yurkas
IBM Research Division
Thomas J. Watson Research Center
P.O. Box 218
Yorktown Heights, NY 10598

Research Division
Almaden - Austin - Beijing - Haifa - India - T. J. Watson - Tokyo - Zurich

LIMITED DISTRIBUTION NOTICE: This report has been submitted for publication outside of IBM and will probably be copyrighted if accepted for publication. It has been issued as a Research Report for early dissemination of its contents. In view of the transfer of copyright to the outside publisher, its distribution outside of IBM prior to publication should be limited to peer communications and specific requests. After outside publication, requests should be filled only by reprints or legally obtained copies of the article (e.g., payment of royalties). Copies may be requested from IBM T. J. Watson Research Center , P. O. Box 218, Yorktown Heights, NY 10598 USA (email: reports@us.ibm.com). Some reports are available on the internet at http://domino.watson.ibm.com/library/CyberDig.nsf/home.

Reliability of MOS devices with tungsten gates

F. Palumbo [(a)], S. Lombardo [(a), 1], J. H. Stathis [(b)],
V. Narayanan [(b)], R. McFeely [(b)], and J. J. Yurkas [(b)]

[(a)] CNR-IMM, Sezione di Catania, ITALY
[(b)] IBM T.J. Watson Research Center, Yorktown, NY; USA

Metal gates are considered a promising approach to increase transistor transconductance and to reduce gate resistance [1]. Tungsten gates, in particular, being a midgap work-function material are considered particularly useful in the case of short channel fully depleted SOI CMOS circuits. To introduce W as gate material, however, major technological challenges have to be faced and solved. Also, concerns related to the reliability of these new MOS stacks have to be taken into consideration. Indeed, the study of the reliability of metal gates with SiO_2 is in itself particularly interesting from the point of view of the basic understanding of the dielectric breakdown (BD) phenomenon. In this paper we present first results on this subject.

The samples are MOS capacitors with standard SiO_2 of 2, 3 and 4 nm of thickness on n-Si and with gate materials of either tungsten or p^+poly-Si. The latter are used as control. In all cases, the accelerated oxide testing consisted of constant voltage stresses in accumulation conditions. Stress-induced leakage current (SILC) measurements were performed to evaluate the status of the oxide. As a function of the injected charge Q_{inj}, the SILC level is evaluated as $(J-J_0)/J_0 = \Delta J/J_0$, where J and J_0 are the gate current after stress and on the virgin sample, respectively.

Poly-Si and W gates on 2 nm oxides show very similar degradation kinetics (Fig.1). This is quite surprising since one would expect that anode hole injection and/or hydrogen release should be different by changing the anode material, and this should be reflected in the wear-out kinetics [2]. We find, on the contrary, the same behaviour for W and p+ poly-Si anodes. Also $\Delta J/J_0$ at BD (i.e. the defect concentration at BD, N_{BD}), reported in Fig. 2, is essentially the same for p^+poly-Si and W gates. This confirms that also with W gates the measurement of SILC is a good methodology for the evaluation of the defect concentration in the oxide, and that BD takes place when the defect concentration (i.e., the SILC level) reaches a critical value. It is confirmed that this value does not depend on the anode, being simply related to the oxide thickness [3, 4].

The fact that (a) N_{BD}, as expected by the current understanding, is the same for W and poly-Si gates, and that (b) P_{gen} (i.e. $d\Delta J/J_0$ / dQ_{inj}), surprisingly, is also very similar in the two cases (Fig. 1) should imply that the charge to BD, Q_{BD}, should be the same for the two gate materials too. This is because $Q_{BD} = N_{BD} / P_{gen}$ [2]. Indeed,. Fig. 3 shows similar result of Q_{BD} for 2 nm p+ poly-Si and W gates.

The other investigated aspect was the BD transient. Its measurement was performed as described in [5]. The evolution of the BD transient is quantified by using the slope of the current during the BD (dI_{BD}/dt), as reported in [6]. We find that W and poly-Si behave very differently (Fig. 4). W gates show a very rapid BD runaway in the whole investigated voltage range, while poly-Si gates show a step decrease on the BD build-up rate. Also in this aspect, the behaviour of the W gate appears quite peculiar. Further work is in progress to try to clarify these aspects.

One of us (F.P.), Ph.D. student of CONICET- DPML at the University of Buenos Aires and now on leave at CNR, gratefully acknowledges economical support of the ICTP-TRIL Programme.

[1] CNR-IMM, Sezione di Catania, Stradale Primosole, 50, 95121 Catania, ITALY. Phone: +39 095 7351056. Fax: +39 095 7139154. E-mail: Salvatore.Lombardo@imm.cnr.it

1. H. S. P. Wong, IBM J. Res. & Dev. 46 No. 2/3, 133 (2002).
2. J. Stathis, IBM J. Res. Dev. 46, No. 2/3, 265 (2002).
3. J. Suñé, I. Placencia, N. Barniol, E. Farrés, F. Martin, X. Aymerich, Thin Solid Films 185, 347 (1990).
4. J. Stathis, J. Appl. Phys. 86(10),5757 (1999).
5. S. Lombardo, F. Crupi, A. La Magna, C. Spinella, A. Terrasi, A. La Mantia and B. Neri, J.Appl.Phys. 84, 472 (1998).
6. B.P. Linder, S. Lombardo, J.H. Stathis, A. Vayshenker and D. Frank. IEEE Trans.Electron Devices. 23, 661 (2002).

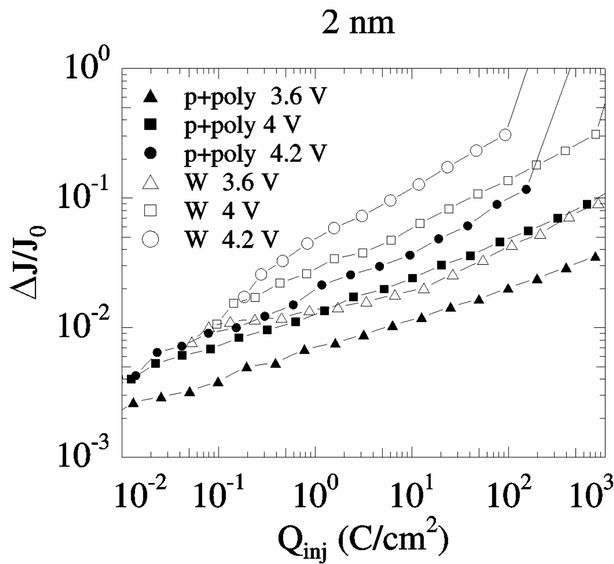

Fig. 1. Behaviour of SILC as a function of the injected charge for W and poly-Si gate MOS capacitors stressed at voltages ranging from 3.6 to 4.2 V. Sense voltage was chosen in order to have the same field in the oxide during sensing, and in particular, it was 2.5 V and 1.8 V, for poly-Si and Wgates, respectively.

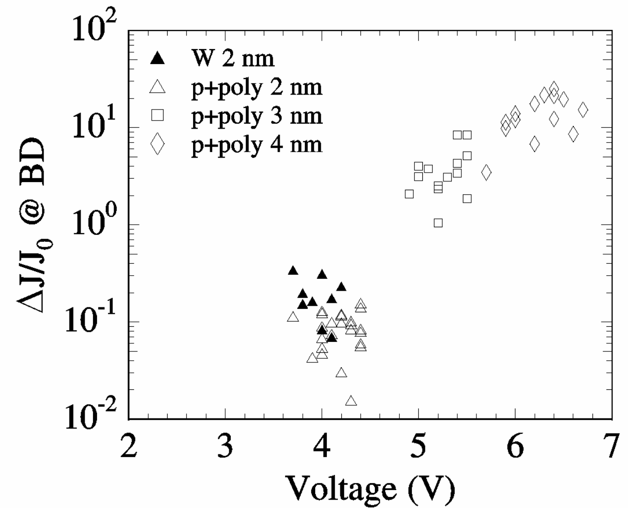

Fig. 2. SILC level at BD, proportional to the defect concentration at BD for poly-Si and W gate MOS devices.

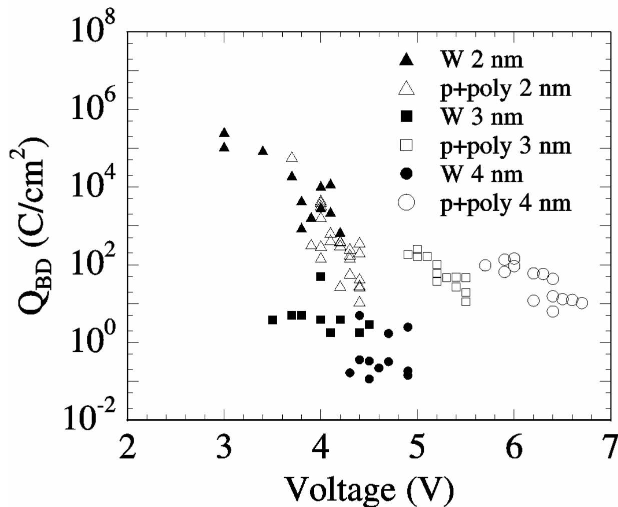

Fig. 3. Charge to breakdown (QBD) as a function of gate voltage during stress for poly-Si and W gate MOS capacitors.

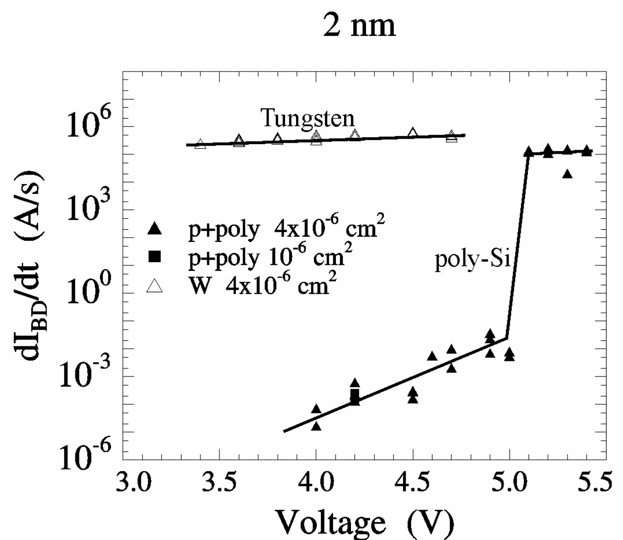

Fig. 4. BD build up rate as a function of gate voltage during stress for poly-Si and W gate MOS capacitors with 2 nm oxides.