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## Charge Trapping in $SiO_2/HfO_2$ Dual Layer Gate Stacks

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# Charge trapping in $SiO_2/HfO_2$ dual layer gate stacks

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**Charge trapping in $SiO_2/HfO_2$ dual layer gate stacks with poly-Si electrodes is reviewed. Results obtained with different measurement techniques are compared and it is shown that pulsed measurement techniques, such as charge pumping (using amplitude sweeps) and the pulsed $I_d$-$V_g$ technique, are useful to quantify the fast transient charging effects in these gate stacks. A trapping model is proposed to explain the observed transient charging behavior.**

## I. Introduction

Many high-k gate dielectrics exhibit excessive charge trapping as compared to scaled $SiO_2$ or oxinitride (SiON) layers, and threshold voltage instabilities remain a major concern for the implementation of high-k materials into the gate stack of future CMOS technologies using standard CMOS processing with poly-Si gates. [1-5]

Conventional techniques based on sense-and stress methods, frequently used for trapping studies in silicon dioxide, have also be sucessfuly applied to high-k gate dielectrics. [4,5]. Some recent studies indicated that the nature of charge trapping in $HfO_2$ containing gate stacks can differ fundamentally from that in SiO2 or SiON layers, requiring alternative characterization techniques to capture the transient aspects of charge trapping. [6-11] Some of these methods are: 1) Capacitance transient measurements with ms time resolution, 2) Pulsed current measurements with µs time resolution, and 3) CP measurements using an amplitude- sweep instead of the more commonly used base level sweep. In this contribution, results obtained by these techniques in $SiO_2/HfO_2$ dual layer gate stacks with poly-Si electrodes will be compared and a simple model [11] to explain the transient phenomena will be discussed.

## II. Experimental

All measurements were done on n-channel FETs fabricated within the SEMATCH/IMEC high-k program either at International SEMATECH [12] or IMEC [13]. An interfacial $SiO_2$ layer was typically formed either by wet-chemical clean or by thermal oxidation prior to the $HfO_2$ (3-5 nm thick) deposition using ALCVD™ or MOCVD. Various Post Deposition Anneals (PDA) were carried out followed by poly-Si deposition and gate activation was done at 1000 $^{O}$C for 1-10 s. Passivation anneals were done in forming gas at temperatures from 400-550 $^{O}$C.[14]

## III. Stress and Sense Experiments

During a constant voltage or current 'stress-and-sense' measurement, the stress is interrupted and charge trapping is measured at a lower voltage. The impact of this interrupt on the measurement results can qualitatively be evaluated with hysteresis measurements.

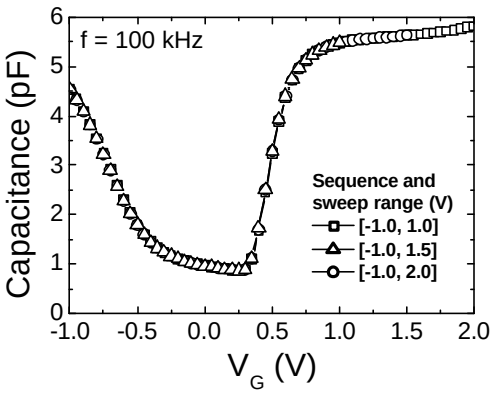


Fig. 1a: Typical repetitive CV up-sweeps measured at a frequency of 100 kHz on a gate stack containing a 5 nm thick $HfO_2$ layer. For measurement sequence and sweep ranges see legend in the figure.) All sweeps started at –1 V.

Typical hystereses measurements for FETs with $HfO_2$ containing gate stacks are shown in Fig. 1a, 1b (Capacitance-Voltage) and in Fig. 2 ($I_d$-$V_g$, drain current-gate voltage), respectively. For clarity, the CV up-sweeps (from negative to positive gate voltage) (Fig. 1a) and CV down-sweeps (Fig. 1b) are plotted separately. The data in Fig. 1a suggest good stability of the gate stack. This is not correct, as demonstrated by the down traces in Fig. 1b, where a substantial $V_t$ instability (~ 200 mV) is observed. It can also be seen that the $V_t$ instability is larger than the $V_{fb}$ instability. This 'stretch-out' is not due to interface-states

[15], as $D_{it}$ remains low during this stress sequence. The same quantitative behavior is observed in Fig. 2, using $I_d$-$V_g$ double-ramp sweeps. All double-ramps were started at $V_g$ = -1.5 V, and the sweep-ranges were increased from 2.5-4.5 V in steps of 0.2 V on the same device.

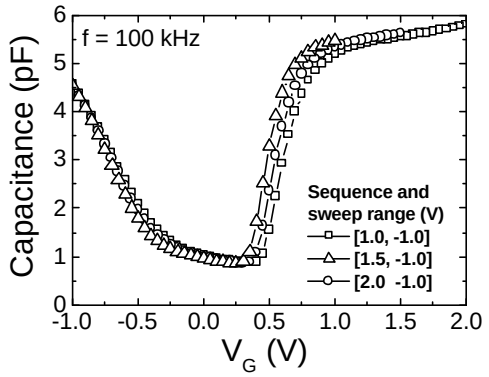


Fig. 1b: Repetitive CV down-sweeps measured at a frequency of 100 kHz on a same gate stack as in Fig. 1a. For measurement sequence and sweep ranges see legend in the figure.

As can be seen, all up-traces are found to be identical, while large shifts (~ 500 mV after a ramp stress to 3 V) are observed on the down-traces. No change in the sub-threshold slope for subsequent up-traces is observed (not shown), excluding $D_{it}$ formation. In Fig. 3, the threshold voltage shift, ? $V_t$, versus maximum gate voltage, $V_{G\_max}$, is summarized for a 4 nm thick $HfO_2$ layer. Shifts are largest for the down traces. About

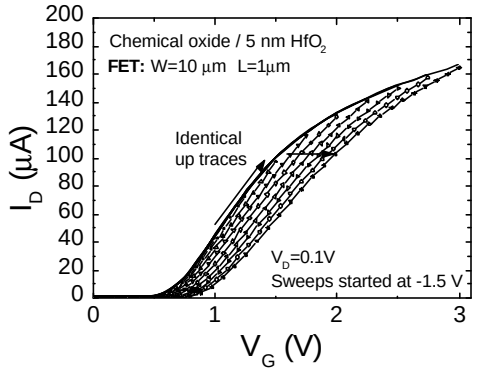


Fig. 2: Sequential $I_D$-$V_G$ dual-ramp measurement for a 5 nm thick $HfO_2$ layer grown on a chemical oxide. Subsequent dual-ramps were all started at –1.5 V and the maximum voltage was continuously increased from 1 to 3 V in steps of 0.2 V.

20 % of the charge is lost after biasing the structure at zero volts (~ 1 sec), as typically done during switching in a 'stress-and-sense' experiment. Interestingly, full charge recovery is observed when the structure is biased at –1 V, constant with the results in Fig. 1 and 2.

These results demonstrate that the magnitude of the charging instability depend on the details of the measurement sequence used in constant voltage (or constant current) 'stress-and-sense' measurements.

The threshold voltage instability is strongly voltage accelerated, as can be seen from the data in Fig. 3. By increasing the maximum gate voltage, $V_{G\_max}$, from 1 V to 2.5 V, the instability increases from ~ 20 mV to ~ 200 mV.

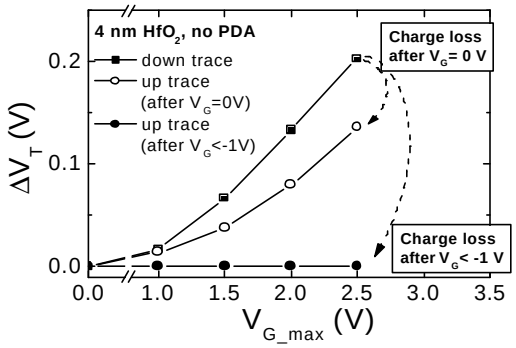


Fig. 3: Dependence of the threshold voltage shift, ? $V_t$ on the $I_D$-$V_G$ dual-ramp measurement range The net shift strongly depends on the lowest voltage value used for the ramp measurement sequence, even for the same maximum gate voltage $V_{G\_max}$.

## IV. Sensing at Stress

Issues with charge loss can be avoided by sensing at the tress condition. Examples of such measurements are shown in Fig. 4 and 5. For the capacitance-time, C-t, measurement in Fig. 4, a pulse was applied to the gate, and the capacitance decay was monitored over time.

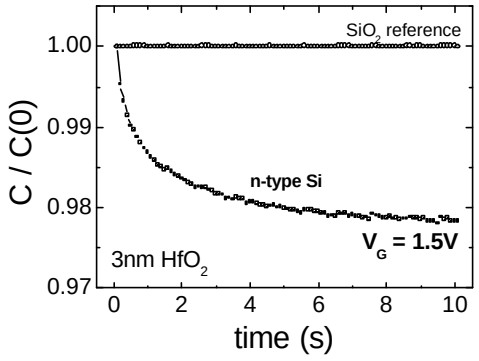


Fig. 4: Capacitance-time transients measured for a 3 nm thick $HfO_2$ layer in the gate stack of an n-FETs in accumulation. N-FET with $SiO_2$ is shown for comparison.

As can be seen, a fast capacitance transient is observed with $HfO_2$ because of the charge induced voltage shifts discussed above. The initial transient is measured to be rather steep, illustrating the need for faster measurement techniques. Accurate absolute extractions of the charge density is only possible, if the capacitance C(0) at t = 0 can be measured correctly, as ?C(V) = C(t) – C(0) is used to calculate the voltage shift ?V = ?C(V) dV/dC.

The constant current measurements (Jg = $10^{-2}$ A/cm$^2$) shown in Fig. 5 also demonstrate the need for faster measurement techniques. As can be seen, for the 5 nm thick control oxide, voltage shifts due to charging are only observed for large amounts of injected charge. This effect is attributed to the slow generation of new defects in the $SiO_2$ layer. [16] In contrast, charge trapping in the $HfO_2/SiO_2$ dual layer stack is considerable (~ 800 mV shifts) and too fast for this technique to provide accurate information on the initial trapping behavior.

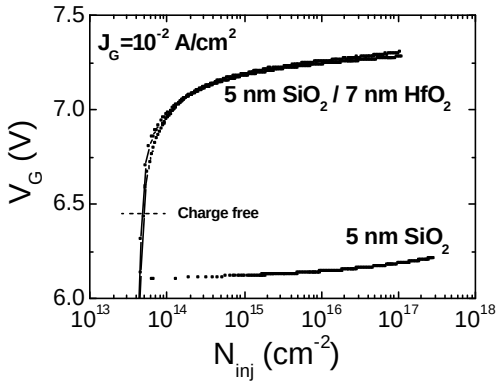


Fig. 5: Constant current stress experiment with 5 nm $SiO_2$ and with a dual layer stack containing 7 nm of $HfO_2$ on top of the 5 nm thick $SiO_2$ layer.

Electron trapping in preexisting defects in the $HfO_2$ layer and/or at the $SiO_2/HfO_2$ interface ('background trapping') is likely responsible for the strong voltage shifts. Recently, it has been demonstrated that trap creation can be directly measured and related to dielectric breakdown by taking advantage of the discussed charging/discharging behavior of the 'background traps'. [17]

## V. PULSED MEASUREMENTS

The transient charging behavior in $HfO_2$ gate stacks can be more comprehensively studied with fast, pulsed measurements. A setup using a dual channel digital storage scope to measure $I_d$-$V_g$ characteristics in the µs time range is illustrated in Fig. 6. An n-channel FET is operated in an inverter circuit with a resistive load, $R_L$. From the two 'voltage–time' traces ($V_G$, $V_D$) the $I_d$-$V_g$ characteristic can be extracted as $I_D = (100mV/V_D)\cdot(100mV - V_D)/R_L$.

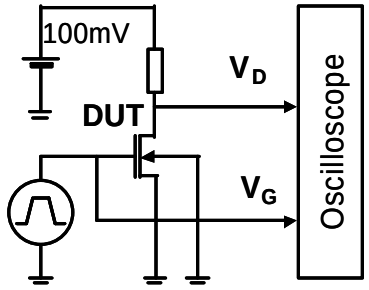


Fig. 6. Schematic of pulsed $I_d$-$V_g$ measurement.

Typical pulsed $I_d$-$V_g$ results are shown in Fig. 7. The initial up-trace and two down-traces (after charging for 100 µs and 500 ms at 2 V) are shown. Also shown by the dashed line is the initial up-trace from Fig. 7, where a 'quasi-DC' ramp was used. With the pulsed technique, essentially parallel $I_d$-$V_g$ curves are measured, suggesting that transient effects can now be largely avoided. Charging during ramp-up is also reduced, as the comparison of the two up-traces illustrates. With a 'quasi-DC' ramp (ramp time > 1 sec), significant charging occurs during ramp-up. The dashed line intercepts the down-trace for the pulsed measurement (500 ms) at its starting point. This shows that charging is near completion within seconds. Finally, the comparison of the two up-traces also shows that charging sets in at fairly low voltages (near $V_t$), consistent with the data in Fig. 3.

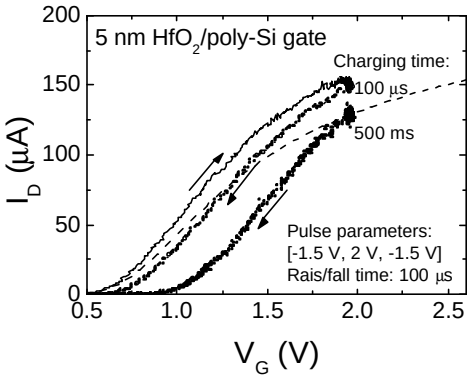


Fig. 7: Typical $I_d$-$V_g$ traces as measured with the pulsed set-up shown in Fig. 6. For comparison, the $I_d$-$V_g$ up-trace (dashed line) from Fig. 2 (slow DC ramp) is shown. The initial up-trace and two down-traces for charging times of 100 µs and 0.5 s (at 2 V) are shown. The fall and rise times were set to 100 µs.

## VI. CHARGE PUMPING

Based on the charging and discharging behavior discussed in section III to V, a variant of the charge pumping (CP) measurement technique can be used, which provides accurate information on charge trapping in the $HfO_2$ layer, in addition to the information obtained on interface states at the $Si/SiO_2$ interface obtained with conventional CP measurements [18], where the base level of the gate pulse is swept from accumulation to inversion (see Fig. 8). This pulse sequence provides poor control over the charge exchange with the high-k layer in $SiO_2/HfO_2$/poly-Si gate stacks. Instead, an amplitude-weep can be use (see Fig. 8) with a sufficiently negative, constant gate bias, $V_{base}$, such that complete discharging of the gate stack occurs during each pulse. Under these 'optimized conditions', at $V_{base}$, all trapped electrons will be emitted from the $HfO_2$ layer to the Si substrate, where they recombine with majority carriers and contribute to the charge pumping current, $I_{CP}$ (measured as a substrate current, $I_{sub}$) (see also Fig. 9).

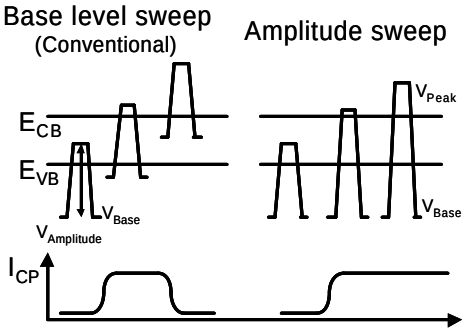


Fig. 8. Schematic of pulse sequences used for interface state measurements with conventional charge pumping (Base level sweep) and for bulk charge measurements in $SiO_2/HfO_2$ dual layer gate stacks (Amplitude sweep).

The schematic in Fig. 9 summarizes the most important contributions to the substrate current, $I_{sub}$, in a CP experiment. In thin oxides, valance band tunneling may dominate over the defect contributions (not shown).

Typical CP curves, $N_{CP} = I_{CP} / (f \cdot q \cdot A)$, measured on an n-channel FET with a 5 nm thick $HfO_2$ layer, are shown in Fig. 10. As can be seen, the measured charge per cycle rapidly increases with the peak voltage, $V_{peak}$, and with the charging time. In absence of bulk trapping, as for $SiO_2$ layers, the CP current stays essentially constant at the level corresponding to the fast interface states (dashed line in Fig. 11) independent of the charging time, t, or frequency. A small dependence on the fall and rise time does exist for fast interface states. [18] The strong increase of

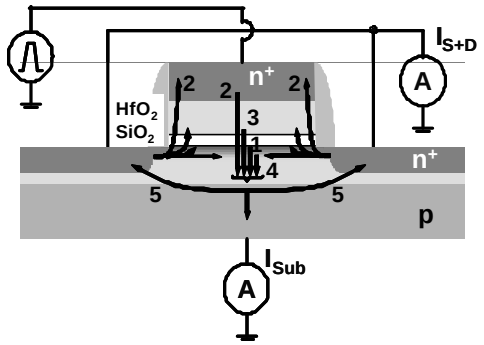


Fig. 9. Possible current contributions in a CP measurement with alternative gate dielectrics. Beside the recombination current due to interface states (1), the gate current contribution (2), charging and discharging of bulk defects (3), recombination of inversion carriers (4) [19] and losses due to minority carrier diffusion (5) (important for electron emission from the $HfO_2$ layer) need to be considered.

the charge per cycle, $N_{cp}$, towards higher voltages in Fig. 11, is due to the charging and discharging of preexisting defects in the $HfO_2$ layer (near the Si substrate and in the bulk). The results obtained with the amplitude sweep ('optimized' conditions) are in good quantitative agreement with results obtained by the single pulsed $I_D$-$V_G$ technique discussed above, if a second order effect related to the channel length is considered [8], as discussed below.

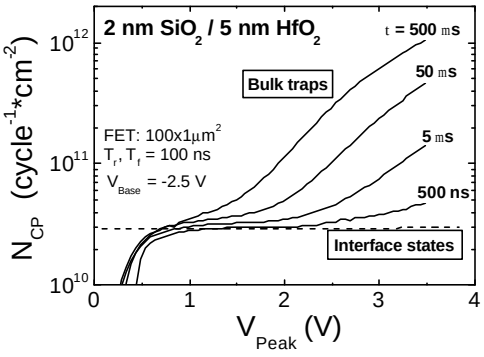


Fig. 10. Charge per cycle and $cm^2$, $N_{CP}$, versus charging time. Fall and raise times, Tf, = Tr = 100 ns and a base voltage, Vbase = - 2.5 V (optimized conditions) were used. The channel length was 1 µm. Curves for four different charging times are shown. The interfacial $SiO_2$ was 2 nm thick.

As shown in Fig. 12, $N_{cp}$ depends on the channel length. For these measurements amplitude sweeps with low frequencies and long rise ($t_r$) and fall ($t_f$) times were used to eliminate the previously identified geometrical component (contributions from inversion charge to the substrate current) [19]. In contrast to the fast

interface states, which recombine at the Si surface, electrons from the $HfO_2$ layer are emitted back into the Si substrate as minority carriers and they have to recombine in the Si bulk in order to contribute to the substrate current. For short channel devices, a significant fraction of the emitted oxide charge may be collected at the S/D junctions before recombination occurs (see schematic in Fig. 9). As can be seen from the data in Fig. 12, about 50 % of the charge is lost to the junctions for a channel length of 1 µm. The presence of this effect clearly shows that the increased $N_{CP}$ values at large $V_{max}$ and long t in Fig. 11 are related to charge trapping (emission) into (from) defects at the $HfO_2/SiO_2$ interface and/or in the bulk of the $HfO_2$ layer.

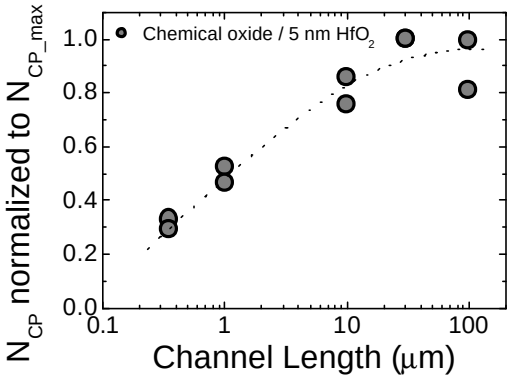


Fig.11: Normalized $N_{CP}$ as a function of channel length. The contribution from fast interface states, $N_{it}$, was measured independently, using conventional CP and subtracted from the total charge pumping current [8].

## VII. DEFECT BAND MODEL

The defect band model sketched in Fig. 13 can be used to explain the essential aspects of the presented experimental data. As can be seen from the center panel of Fig. 13, a defect band is postulated in the $HfO_2$ layer. Placing the defect band in energy above the Si conduction band allows for efficient charging (Fig. 12 left panel) and discharging (Fig. 12 right panel) of the bulk defects by applying positive or negative gate bias, respectively. The energy shift of the defect band (with respect to the Fermi level in the Si substrate) with varying gate bias is 'amplified' due the large difference in the dielectric constants between the $SiO_2$ interfacial layer and the $HfO_2$ film: $dE = 1/q\ V_g\ (t_{SIO2}/EOT_{stack})$, where q is the electron charge, $t_{SIO2}$ is the interfacial layer thickness and $EOT_{stack}$ is the electrical thickness of the gate stack. For positive gate bias, the defect band moves below the Fermi level in the Si substrate. The band can be filled by tunneling into the shaded area in Fig. 13, and possibly be subsequently transport through the defect band. For negative gate bias, the states in the shaded area will empty by tunneling. Bulk states may be transported to the shaded area before tunneling. These features of the model explain the observed polarity dependence. Some issues remain with respect to charge trapping under negative gate bias, as de-trapping has to dominate. The asymmetry in the gate current density may be of importance to fully understand the strong asymmetry with polarity. In any case, the rapid charging and discharging of the defect makes the proposed amplitude sweep particularly useful to study the impact of charge trapping inside the gate stack on the device parameters.

It is interesting to note that an oxygen related defect band has been identified approximately 1.2 V below the $HfO_2$ conduction band edge. [20] This would place the bottom of the oxygen relate defect band approximately 0.4 V above the Si conduction band, using a band offset of 1.5 V between the Si and the $HfO_2$ conduction bands [15], and well within the range required in the proposed model. Oxygen vacancies have been proposed as electron traps in other high-k gate dielectrics, and a similar defect band model has been used to explain charge transport. [21]

The vacancies have to be mostly neutral initially, as no strong $V_t$ and $V_{fb}$ shifts with increasing oxide thickness are observed for as fabricated stacks. [13]. The dependence of charge trapping on post high-k deposition annealing temperature and ambient are often reported to be weak. This suggests that the oxygen vacancy concentration is largely determined by the gate activation anneal and can not be significantly reduced by pre-gate processing, provided the oxygen vacancies are indeed the responsible defects. Comparable results are obtained for $HfO_2$ films deposited by different techniques (PVD [22], CVD, MOCVD), suggesting that impurities (Carbon or Chlorine) are not the cause for the observed charge trapping.

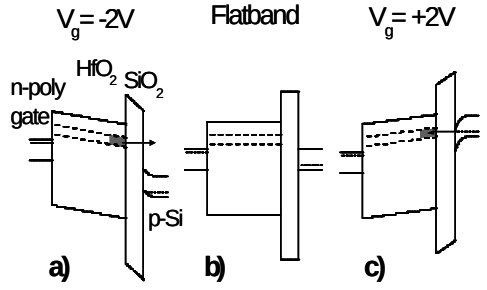


Fig. 12: Defect band model used to explain the trapping behavior in $HfO_2/SiO_2$ dual layer gate stacks (b). Defects can be filled under positive bias (a) and emptied under negative bias (c).

## VIII. CONCLUSIONS

Recent charge trapping studies in $SiO_2/HfO_2$ dual layer gate stacks with poly-Si electrodes have been reviewed. It was shown that strong transient charging effects require the use of pulsed measurement techniques to fully capture the instabilities in these gate stacks. Besides pulsed measurements using a storage scope for data collection, a variant of the CP technique (amplitude sweep) was shown to be particularly useful to study the charging instabilities in these stacks.

Based on the experimental results, a band of defect was proposed to exist in $HfO_2$. The defects are located in energy above the conduction band edge of Si. It is proposed that the defect band originates from oxygen vacancies in the $HfO_2$ layer. The relatively weak dependence on processing conditions suggests that the oxygen vacancy concentration in poly-Si gated devices is largely determined by the gate processing (poly-Si deposition and activation anneal). This would imply that gate stacks containing $HfO_2$ are inherently unstable if used in a standard CMOS process. It might be expected, that better stability can be obtained with Hf-silicates or with metal gated $HfO_2$ devices.

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