RC23165 (W0403-157) March 26, 2004
Materials Science

IBM Research Report

Strained Si-on-Insulator Fabricated from Elastically-Relaxed Si/SiGe Structures

P. M. Mooney, G. M. Cohen, H. Chen*, J. O. Chu, N. Klymko*
IBM Research Division
Thomas J. Watson Research Center
P.O. Box 218
Yorktown Heights, NY 10598

*IBM Microelectronics Division
Hopewell Junction, NY 12533

Research Division
Almaden - Austin - Beijing - Haifa - India - T. J. Watson - Tokyo - Zurich

Strained Si-on-Insulator Fabricated from Elastically-Relaxed Si/SiGe Structures

P.M. Mooney [1], G.M. Cohen [1], H. Chen [2], J.O. Chu [1], and N. Klymko [2]
[1] IBM T.J. Watson Research Center, Yorktown Heights, NY 10598
[2] IBM Microelectronics Division, Hopewell Junction, NY 12533

ABSTRACT

Blanket pseudomorphic $Si_{0.8}Ge_{0.2}$/Si layer structures grown by Rapid thermal Chemical Vapor Deposition (RTCVD) on SOI substrates were etched to form 5μm × 5μm slabs, supported by a single pedestal at the center. Symmetric tri-layer slabs, 20nm Si/236nm $Si_{0.8}Ge_{0.2}$/20nm Si supported by a SiO_2 pedestal are flat and x-ray diffraction measurements of the strain and the thickness of the layers confirmed that the strain is shared between the Si and SiGe layers according to the ratio of the thickness of the SiGe and Si layers. These tri-layer structures were then *firmly attached* to the substrate using a filling material. A thermal oxide layer was grown on the upper and lower surface of the free-standing structures and then polycrystalline Si was deposited to fill the space between the free-standing structure and the Si substrate, thus attaching the bottom strained Si layer to the substrate. The polycrystalline Si was subsequently removed by reactive ion etching except from under the Si/SiGe/Si slab. The top SiO_2 and Si layers as well as the SiGe layer were then removed selectively by wet etching. Raman spectroscopy measurements show that the strain in the attached strained Si-on-insulator layer is $\varepsilon = 0.0067$.

INTRODUCTION

The higher carrier mobility in Si under biaxial tensile strain of ~1% results in enhanced performance of field-effect transistors (FETs) fabricated in strained Si compared to devices of similar dimension fabricated in bulk Si(001) [1-5]. Strained Si layers for devices are typically achieved by growing a pseudomorphic Si layer epitaxially on a strain-relaxed SiGe buffer layer [1]. Strained-Si-on-insulator substrates have been fabricated using wafer bonding methods to transfer a thin strain-relaxed SiGe layer to form SiGe on insulator substrates on which a strained Si layer is subsequently grown epitaxially [2,3] or by a thermal mixing method [4]. Transfer of a strained Si layer by wafer bonding to form strained-Si-directly-on-insulator wafers has also been demonstrated [5,6]. With the latter structure the processing disadvantages when SiGe is present are eliminated.

A serious drawback for all of these strained Si structures is the presence of defects that relieve the lattice mismatch strain in the SiGe buffer layer. The usual defects are 60^o misfit dislocations that terminate in threading arms that run up to the wafer surface, thus passing through the active regions of the devices. Additionally, if the strained Si layer exceeds the critical thickness for dislocation glide, misfit dislocations may form at the interface between the strained Si layer and the SiGe buffer layer either during the growth of the strained Si layer or during subsequent device fabrication processes that are performed at higher temperatures.

An alternative approach is to achieve strained Si structures for device applications by means of elastic strain relaxation, i.e., without the introduction of misfit dislocations. In one implementation, a pseudomorphic SiGe/Si layer stack is transferred by wafer bonding onto a borophosphorosilicate (BPSG) glass rather than to SiO_2. After patterning the bonded wafer, the strain in the pseudomorphic SiGe layer relaxes elastically during annealing at high temperature

and as a result the Si layers are under tensile strain. The SiGe film is etched leaving a strained-Si-directly-on-insulator [7]. The main drawback of this method is that any subsequent processing has to be carried out at a lower temperature than that of the BPSG glass reflow temperature or otherwise the strained silicon film will relax. Additionally, all of the methods for making strained Si-directly-on-insulator require non-conventional wafer bonding due to the use of materials other than Si and SiO_2.

Another method is based on elastic strain relaxation during epitaxial growth of a lattice-mismatched layer on a small free-standing substrate. This concept was first demonstrated for 13 μm-diameter $In_{0.15}Ga_{0.85}As/In_{0.4}Ga_{0.6}As$ quantum well structures, supported at the center by an $Al_{0.6}Ga_{0.4}As$ pedestal, where the wavelength of the emitted light from the quantum well showed that the relatively thick $In_{0.15}Ga_{0.85}As$ cladding layers are strain-relaxed [8]. More recently it was reported that SiGe could be grown epitaxially on 5 μm × 5 μm Si slabs, supported at the center by a 0.7 μm-diameter SiO_2 pedestal [9,10]. The strain is shared between the SiGe and Si layers according to the ratio of the layer thickness as predicted by a force balance model [9]. AFM images of the surface clearly show that there are no misfit dislocations, even when the thickness of the SiGe layer exceeds the critical thickness for misfit dislocation formation on an area of the wafers that was not patterned [10].

Here we present a method to utilize elastically-relaxed SiGe/Si structures for the fabrication of strained Si directly on insulator (SSDOI) wafers for strained Si devices. Pseudomorphic SiGe and Si layers were first grown on an SOI substrate to form a symmetric tri-layer structure. The wafer was patterned to form Si/SiGe/Si slabs and the buried oxide layer was etched to form a supporting SiO_2 pedestal. The free-standing Si/SiGe/Si structure relaxed elastically at room temperature according to the layer thickness ratio, consistent with the force balance model [9]. An oxide layer was then grown and polycrystalline Si was deposited to fill the gap between the Si/SiGe/Si structure and the Si substrate, thus attaching the elastically relaxed structure to the Si substrate. The polycrystalline Si layer on top of the Si/SiGe/Si structure was removed, as were the upper Si layer and the SiGe layer, leaving the lower stained Si layer behind. We show that the filling material preserves the strain state of the Si layer as it was on the free-standing Si/SiGe/Si structures.

EXPERIMENTAL DETAILS AND RESULTS

The structures were evaluated after each major fabrication step using scanning electron microscopy (SEM) and high-resolution x-ray diffraction (XRD). The starting wafers were commercially bonded SOI substrates with a 55 nm thick Si-on-insulator (SOI) layer and 145 nm thick buried oxide (BOX). The SOI layer was thinned down to 20 nm and a metastable pseudomorphic $Si_{0.8}Ge_{0.2}$ layer (236 nm) and a Si (20 nm) cap layer were grown on the SOI layer by rapid thermal chemical vapor deposition (RTCVD). A low-temperature oxide, serving as a hard mask, was deposited on the Si/SiGe/Si film stack and patterned by optical lithography and reactive ion etching (RIE). The photoresist was stripped and hydrogen bromide (HBr) based chemistry was used to etch the Si/SiGe/Si film not protected by the hard mask down to the buried oxide (Fig. 1a). A 10:1 diluted hydrofluoric (HF) acid etch was used to remove the buried oxide. The etching was timed to form a free-standing Si/SiGe/Si slab which is supported by a single narrow SiO_2 pedestal (Fig 1b).

Fig. 2 shows an SEM image of an array of free-standing $Si/Si_{0.8}Ge_{0.2}/Si$ slabs supported by the SiO_2 pedestal as shown in Fig. 1(b). Note that the pedestal is wider at the top than at the

base due to a faster oxide etch rate at the bonding interface, which is the BOX/silicon-substrate interface. The x-ray diffraction map for this structure is shown in Fig. 3. The compressive strain in the $Si_{0.8}Ge_{0.2}$ layer is reduced by 83%. When the Si/SiGe/Si slab is released from the BOX, the lattice mismatch strain between the SiGe and Si layers remains constant indicating that no defects are formed. Thus the mismatch strain is transferred to the Si layers as a tensile strain of 0.0069. Fig. 4 is a plot showing the data point for this sample plotted with the data and the force balance model from Ref. 10. The plotted data further confirm that the relaxation is purely elastic and is independent of the growth method used for the SiGe and Si films, and also independent of whether relaxation occurs during growth at 550 ^{o}C or at room temperature by etching.

Next the S/SiGe/Si slab was attached firmly to the substrate. This was achieved by thermal growth of a thin oxide on the Si/SiGe/Si surfaces, and then blanket deposition of a conformal polycrystalline Si film that fills the gap between the slab and the silicon substrate (Fig. 5(a)). The polycrystalline Si on top of the structure was selectively etched by reactive ion etching (RIE) using HBr based chemistry. The polycrystalline Si between the Si/SiGe/Si slab and the substrate is not etched, since it is shadowed by the slab (Fig. 5(b)). The exposed thin thermal oxide was removed by etching in a bath of 100:1 diluted HF. Then the top silicon film was removed selectively with respect to the SiGe layer by etching with tetramethylammonium hydroxide (TMAH) 25 wt. % at room temperature and, finally, the SiGe film was removed selectively with respect to the bottom strained-silicon layer by etching in a bath of aged 1 HF:2 H_2O_2:3 CH_3COOH (Fig. 6).

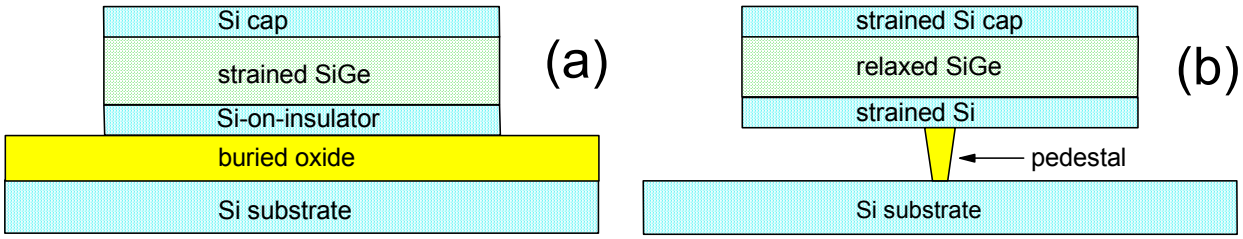

Fig. 1. Processing steps to create free-standing Si/SiGe/Si structures: (a) Pattern the Si/SiGe/Si film stack into isolated regions by etching down to the buried oxide and then (b) release the film stack by etching the BOX to form a free-standing Si/SiGe/Si slab supported by a single SiO_2 pedestal.

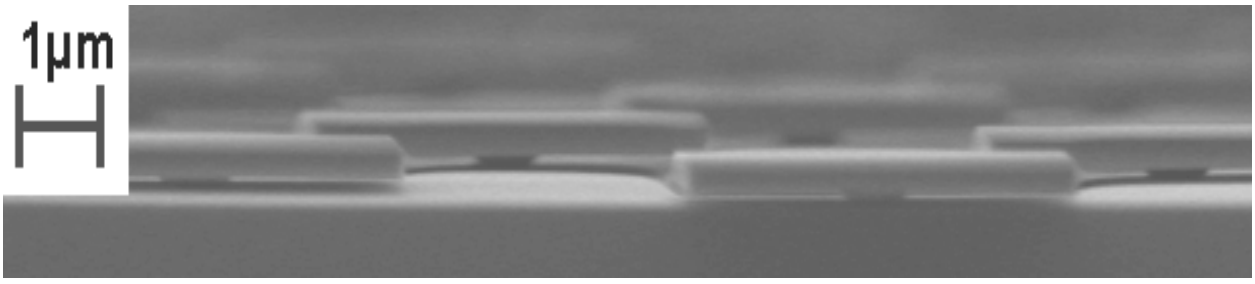

Fig. 2. SEM image of the free-standing Si/SiGe/Si slabs supported by an SiO_2 pedestal, shown schematically in Fig. 1(b).

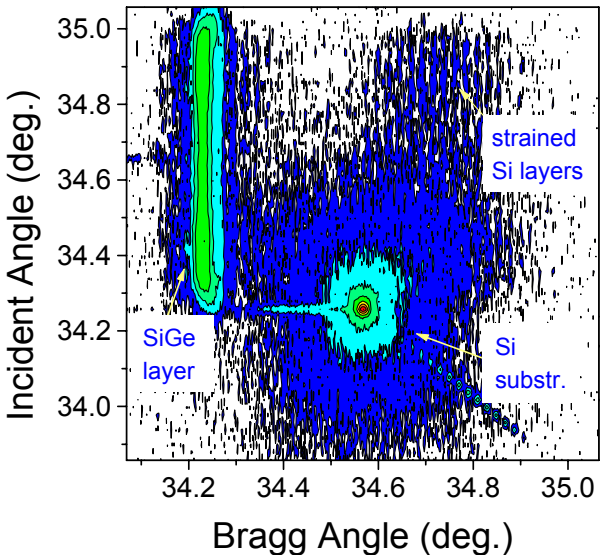

Fig. 3. Triple axis x-ray diffraction map of the etched structure. The $Si_{0.8}Ge_{0.2}$ layer is 83% relaxed and the Si layers have a biaxial tensile strain of 0.0069.

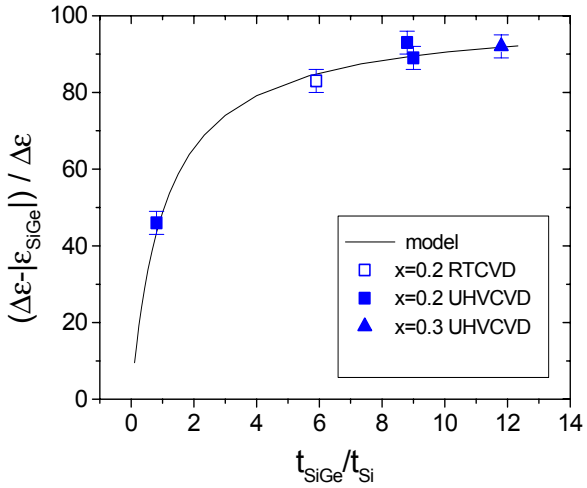

Fig. 4. Strain relaxation of the $Si_{1-x}Ge_x$ layer in symmetric tri-layer free-standing Si/SiGe/Si features (open symbol) with data and model from Ref. 10.

Fig. 6 shows the drawing and SEM image of the strained-Si-on-insulator structures. SEM cross sectional images of the structures reveals a partial seam in the polycrystalline Si filling. While the seam does not seem to affect the strain in sample we have tested, further work is underway to obtain a seamless fill. The SEM also shows the polycrystalline Si sidewalls on either side of the strained silicon region, and the SiO_2 pedestal at the center of the region. Fig. 7 shows Raman spectroscopy data for the strained Si layer in the final structure. The strain in the bottom silicon film is retained even after the SiGe layer is removed, since the silicon film is rigidly attached to the substrate by the polycrystalline Si filling. The measured strain is 0.0067, in good agreement with the strain measured by XRD before removal of the SiGe layer. To test

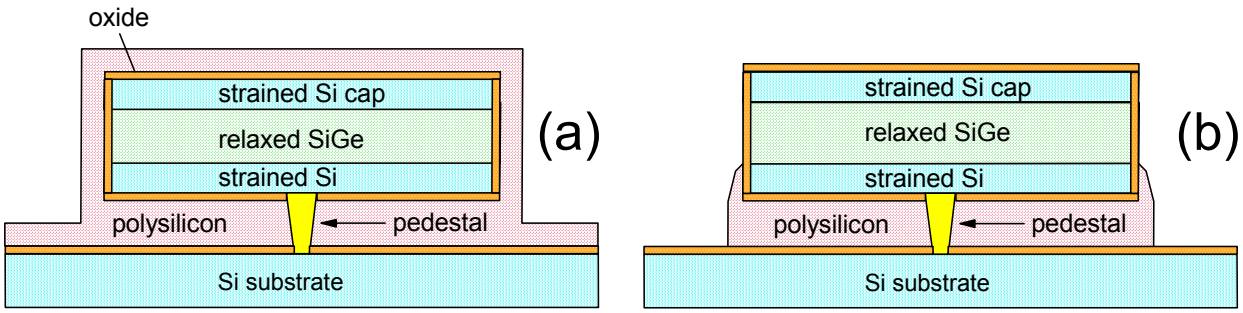

Fig. 5. Processing steps for attaching the strained silicon film to the substrate: (a) Deposit an insulating material on the Si/SiGe/Si slab and substrate or grow a thin thermal oxide. Reattach firmly the Si/SiGe/Si slab to the substrate using a filling material. (b) Etch the filler material except from where it is shadowed by the Si/SiGe/Si slab.

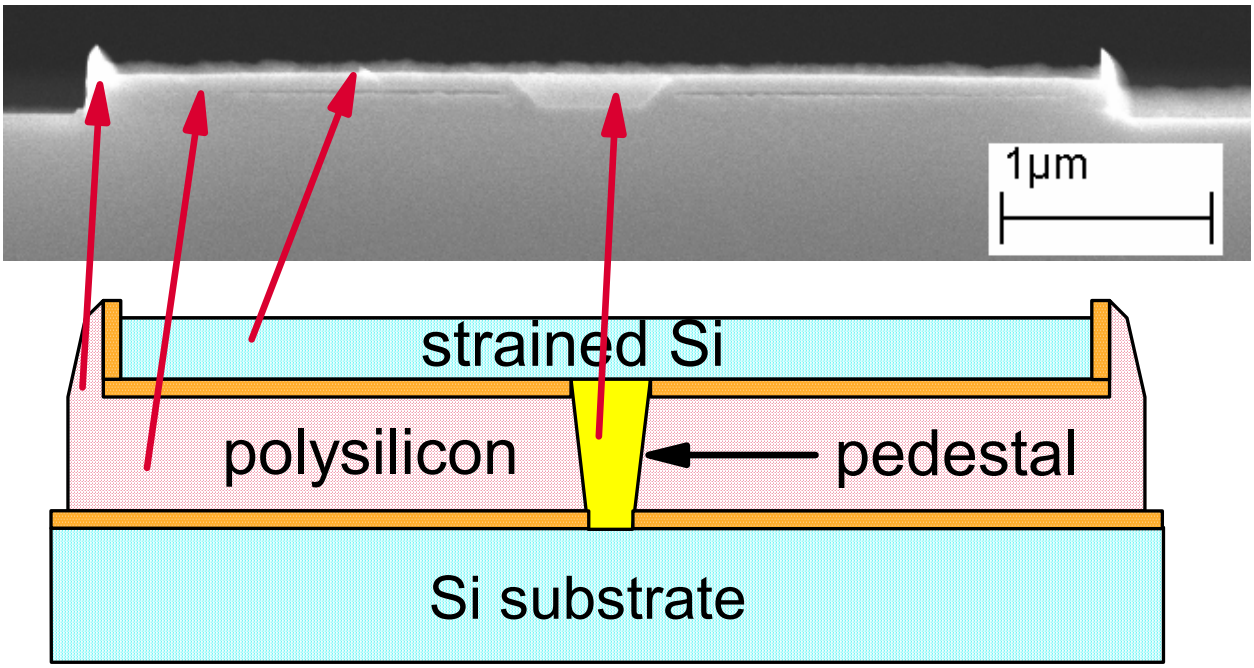

Fig. 6. SEM image and drawing of the structure after removal of the upper SiO_2, Si and SiGe layers.

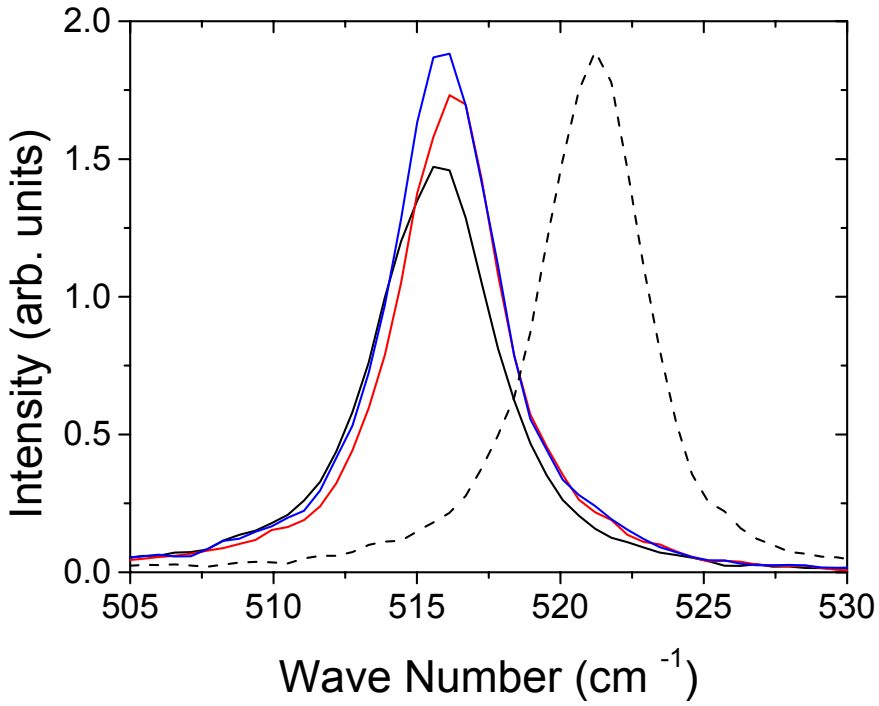

Fig. 7. Si-Si mode for bulk Si (dashed curve) and for the strained Si layer attached to bulk Si using with polycrystalline Si (solid curves). In order of increasing intensity the strained Si samples are as-fabricated, heated to 1070 ^{o}C and heated to 1000 ^{o}C.

the thermal stability of the strained Si structures, a sample was ramped up to 1000 ^{o}C at a rate of 50 ^{o}C/sec and held there for 5 sec and another was ramped up to 1070 ^{o}C at a rate of 100 ^{o}C/sec with no hold, both in N_2 ambient. The average strain measured on four different features on each of these samples is 0.0063 and 0.0061 respectively, 6% and 9% lower than that measured in the as-fabricated sample. The scatter in the strain of the four different features on the same sample is <1%. This slight strain relaxation may occur because of the voids at the seam of the filling material as seen in Fig. 6.

SUMMARY AND CONCLUSIONS

We have shown that symmetric Si/SiGe/Si slabs supported at the center by an SiO_2 pedestal, formed by etching epitaxial layers grown on a commercially bonded SOI substrate, relax elastically as predicted by a force balance model. More importantly, we have also shown that these slabs can be *firmly attached* to a Si substrate using polycrystalline Si as a filling material. After removing the upper Si layer and the SiGe layer, the strain in the remaining Si layer is the same, within measurement error, as it was in the free-standing structures prior to thermal oxidation and deposition of the polycrystalline Si. This work points the way to the use of these elastically-relaxed SiGe/Si structures with low defect density for the fabrication of strained Si CMOS devices.

REFERENCES

1. K. Rim, J. Chu, H. Chen, K.A. Jenkins, T. Kanarsky, K. Lee, A. Mocuta, H. Zhu, R. Roy, J, Newbury, J. Ott, K. Petrarca, P. Mooney, D. Lacey, S. Koester, K. Chan, D. Boyd, M. Ieong, and H.-S. Wong, *Symp. on VLSI Tech*., p.98 (2002).
2. Lijuan Huang, J.O. Chu, S.A. Goma, C.P. D'Emic, S.J. Koester, D.F. Canaperi, P.M. Mooney, S.A Cordes, J.L. Speidell, R.M. Anderson and H.-S.P. Wong, IEEE Trans. Electron. Devices **49**, 1566 (2002).
3. Zhi-uan Cheng, M.T. Currie, C.W. Leitz, G. Taraschi, E.A. Fitzgerald, J.L. Hoyt and D.A. Antoniadas, IEEE Electron. Device Lett. **22**, 321 (2001).
4. B.H. Lee, A. Mocuta, S. Bedell, H. Chen, D. Sadana, K. Rim, P. O'Neil, R. Mo, K. Chan, C. Cabral, C. Lavoie, D. Mocuta, A. Chakravarti, R.M. Mitchell, J. Mezzapelle, F. Jamin, M. Sendelbach, H. Kermel, M. Gribelyuk, A. Domenicucci, K.A. Jenkins, S. Narasimha, S.H. Ku, M. Ieong, W. Haensch and J. Welser, *IEDM Technical Digest*, p. 946 (2002).
5. K. Rim, K. Chan, L. Shi, D. Boyd, J. Ott, N. Klymko, F. Cardone, L. Tai, S. Koester, M. Cobb, D. Canaperi, B. To, E. Duch, I. Babich, R. Carruthers, P. Saunders. G. Walker, Y. Zhang, M. Steen and M. Ieong, *IEDM Technical Digest*, p. 49 (2003).
6. T.S. Drake, C. Ni Chleirigh, M.L. Lee. A.J. Pitera, E.A. Fitzgerald, D.A. Antoniadis, D.H. Anjum, J. Li, R. Hull, N. Klymko and J.L. Hoyt, Appl. Phys. Lett. **83**, 875 (2003).
7. Haizhou Yin, K.D. Hobart, Rebecca L. Peterson, F.J. Kub, S.R. Shieh, T.S. Duffy and J.C. Sturm, *IEDM Technical Digest*, p. 53 (2003).
8. A.M. Jones, J.L. Jewell, J.C. Mabon, E.E. Reuter, S.G. Bishop, S.D. Roh and J.J. Coleman, Appl. Phys. Lett. **74**, 1000 (1999).
9. P.M. Mooney, G.M. Cohen and J.O. Chu and C.E. Murray, Appl. Phys. Lett. **84**, 1093 (2004).
10. G.M. Cohen, P.M. Mooney and J.O. Chu, Mat. Res. Soc. Symp. Proc. **768**, 9 (2003)