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FinFET SRAM for High-Performance Low-Power Applications

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Abstract

SRAM behavior of FinFET technology is investigated and compared with 90 nm node planar partially-depleted silicon-on-insulator (PD-SOI) technology. Unique FinFET circuit behavior in SRAM applications, resulting from the near-ideal device characteristics, is demonstrated by full cell cross section simulation for the first time, and shows high performance and low active and standby power. SRAM stability is in detail analyzed as compared to PD-SOI.

Introduction

Double-gate FinFET is a very promising candidate to extend scaling beyond the limit for conventional MOSFETs, with the simplest fabrication process offered by symmetric double-gate technologies [1]. Both logic and SRAM FinFET technologies have been previously demonstrated in [2-3].

The FinFET applicability for SRAM in a full cell design however has not been previously studied. In this paper, we examine key SRAM issues with FinFET technology, regarding performance, power, and stability.

The reference point for this study is a 90 nm node PD-SOI planar technology with extremely scaled oxide (~1 nm) and low supply voltage (~1 V) for SRAM analysis. The planar SOI technology is similar to [4]. The FinFET technology in this study is designed with comparable channel length and digital logic performance. Figure 1 shows the FinFET channel design fabricated in a substrate with a buried oxide. The FinFET silicon is 10 nm wide (T_{fin}).

The double-gate technology advantage allows the gate oxide to be less aggressive (~1.5 nm), which results in lower gate-leakage power. Selected technology parameters from the PD-SOI and the FinFET SRAM devices used in this study are compared in Table 1.

Metric	NFET	PFET
Ion [uA/um]	-90	0
Ioff [nA/um]	-30	-30
Vtlin [mV]	-145	-120
DIBL [mV]	-130	-130

Table 1: Transistor design parameters showing the offset between the FinFET devices and the planar SOI devices. A negative value means the FinFET is lower.

The FinFET performance advantage derives from the reduced threshold (Vt) possible in a dual gate device (enabled by better subtheshold swing). As Table 1 shows, the FinFET devices have lower linear threshold voltages and drain-induced barrier lowering (DIBL) because the wrap-around FinFET gate exerts more control of the channel charge as compared with the planar single gate[5] and due to the elimination of floating body effects. This Vt reduction compensates performance for the difference in NFET Ion. Such attributes are ideal for SRAMs.

Device Models

We use the IBM circuit simulator PowerSpice[6] to study FinFET SRAM behavior. The planar PD-SOI technology is modeled using the Compact Model Council (CMC)-standard compact model [7] BSIMPD from the University of California, Berkeley [8]. This model is incorporated into a subcircuit that includes the BSIMPD model and current sources to model the gate-to-source and gate-to-drain leakage present in scaled SOI technologies.

The FinFET compact models used in this study are assembled using a modified version of planar PD-SOI compact model. This approach captures important first-order FinFET features such as low subthreshold slope, reduced drain-induced barrier lowering (DIBL), reduced junction capacitance, and suppressed body factor while automatically including SOI features such as source/drain isolation from the substrate and self-heating.

Due to the thin fin thickness T_{fin}, the fin bodies are fully depleted under typical doping conditions. Full depletion implies that the mobile majority charge in the body will be zero, and to first order, in strong inversion, the body potential is constant [9]. Therefore the body charges including the body-to-diffusion junction capacitance terms are zeroed out through model parameter changes. Diode and impact ionization effects are also shut off due to full depletion together with the assumption that impact ionization effects will be low because of the scaled power supply voltage. For numerical considerations the floating body is tied to the source node through a resistor R_{numer} since in this approximation it has little influence on the overall result. Note that because the body is fully depleted and the body does not move, the SOI history effect is negligible. The schematic of the modified model is given in Figure 2.

Finally while the fin thickness is narrow enough to experience double-gate inversion charge control, it is assumed to be insufficiently narrow to significantly influence charge transport properties between the source and drain; the same mobility model formulation is used as the planar PD-SOI technology. Using this formulation the FinFET models are calibrated to the targets in Table 1. The

improved subthreshold characteristics of the model are demonstrated in Figure 3.

Width Quantization

The width of the FinFETs is quantized in multiples of 2 x H_{fin} based on the process technology. For scaled technologies the effect of fin quantization can be large and the SRAM cell response can be very sensitive to it. In this study the fin count was chosen to approximate the widths used in the comparison planar technology and also corresponds to the fin packing density possible in the original PD-SOI planar cell design. An exact match in widths is not possible, and the percentage change is given in Table 2. More details on the effects of width quantization are given in the subsequent section.

FET Type	Fin count	Change in Width
Pull-up	1	13.1%
Pull-down	2	-3%
Pass-gate	1	5%

Table 2: Quantization effect on SRAM cell

Performance

The simulated SRAM cross section is shown in Figure 4 and a plan view of the cell in Figure 5. Since the fin height is quantized it is important to study the quantization effect on performance. Two planar SOI cells with Regular Vt (RVT) and High Vt (HVT, Vt offset ~ 80 mV) devices are compared with the quantized FinFET cell topology. To measure the read performance, a sense amp is used (not shown here but is common to both analyses). The combined quantization effect on cell and sense amp is analyzed using circuit delays (see Figure 6). The read delays measured from the wordline rise through the cell to the sense amp output are shown in Figure 7. The read delays improve significantly for the FinFET structure as the cell pass-gate strength increases due to quantization, thereby slightly changing the beta ratio of the cell. Since the FinFETs are fully depleted, the device junction capacitance is negligible, giving additional delay improvement. Combined with lower FinFET DIBL, the delays improve substantially compared to both the RVT and HVT cells. The HVT cell creates a different beta ratio compared to the RVT, and resistance to pull-down "0" increases (due to slow down of pass-gate and pull-down devices).

For write delays, however, the comparison point changes (Figure 8). The write delays for FinFET are higher than the RVT SOI cell. The write delays are measured from 50% bitline switch point to the 50% switch point of the flipping of the opposite cell node. Thus this is a true representation of the cell delay. Due to width quantization, the Pfet strength (whose width is smaller to start with) increases, making the write ("0" to "1") operation more difficult. For the RVT cell, the pass-gate and pull-down Nfets become stronger, while for the HVT cell the pass-gate and pull-down stacks gets weaker. Thus the strength of the pass-gate and pull-down transistors affect the write delays.

Power

Figure 9 shows power comparison for FinFET and PD-SOI for read and write operations. As can be seen the active power shows marked difference between the FinFET cell vs. PD-SOI cell. The FinFET cell has much lower active power. Since FinFET devices are fully depleted the device junction capacitance is negligible compared to PD-SOI devices, the active power is reduced.

The half-select power (when bit lines are held at Vdd) is slightly lower for FinFET cell (Figure 10). As the FinFET is fully depleted, Vt changes due to floating body effects are eliminated, compared to PD-SOI. This reduced Vt variation results in reduced leakage during the half-cell select operation.

Similar analysis is helpful in explaining the difference between the two for standby power (Figure 11). The slope for leakage power is much smaller for FinFET cell while it is much sharper for PD-SOI. This is due to the lower FinFET Ioff and DIBL.

Stability

Figure 12 shows read-disturb stability for the FinFET and PD-SOI cells. The stability depends on process-induced Vt fluctuations, and on length and width variation of the cell devices. As the magnitude of the Vt scatter increases, the maximum stable voltage (Vmax, the voltage at which cell does not flip) needs to be lowered for "Half-select or read stability". A similar analysis holds for write-ability. In addition when the device drive strength increases, the Nfet devices get stronger which allows the cell to flip with bitlines precharged to Vdd. For the RVT SOI cell similar Vt scatter makes the cell more unstable. As a result the maximum stable voltage decreases. Figure 13 illustrates the minimum voltage (Vmin) for stability as a function of scatter. The FinFET shows a lower value until the sensitivity of its lower threshold voltages is realized.

Summary

FinFET-based SRAM cells were analyzed using compact model simulations. The circuit performance of a FinFET SRAM has been compared with conventional planar PD-SOI and shown to exhibit reduced delays. Standby power was shown to be smaller than the PD SOI cell and the effect of quantization on stability was explored and demonstrated to be acceptable.

References

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[2] Rainey, B. A., et al., "Demonstration of FinFET CMOS Circuits," *Device Research Conference 2002 Proceedings*, pg. 47.
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[7] Compact Model Council web page, http://www.eigroup.org/cmc/soi/default.htm
[8] *BSIMPD MOSFET Model User's Manual*, http://www-device.eecs.berkeley.edu/bsim3soi/get2.html
[9] Su, P., et al., "On the Body-Source Built-In Potential Lowering of SOI MOSFET's", *IEEE Electron Device Letters*, Vol. 24, No. 2, pg. 90.

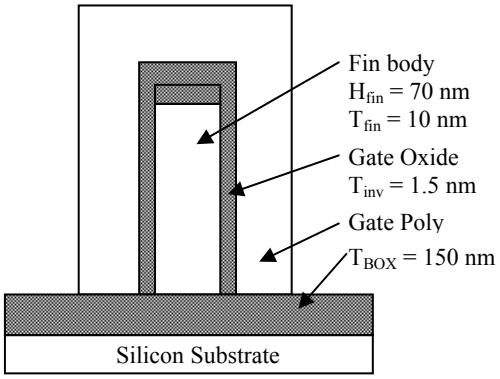

Figure 1 - Structural details of the Nfet and Pfet FinFETs (Source/drain direction into the page).

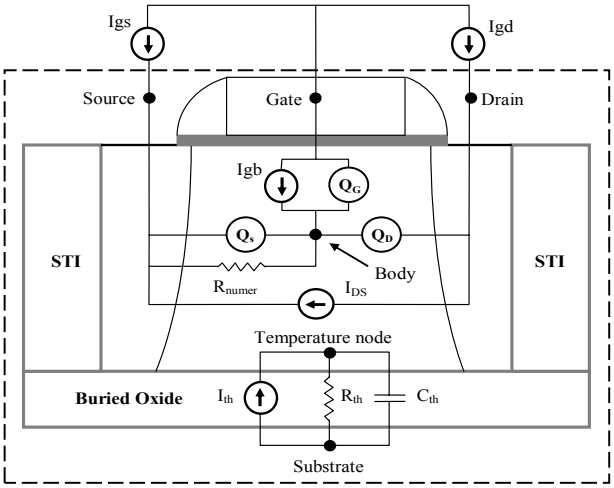

Figure 2 - View of the FinFET taken along the MOS channel showing the electrical elements of the FinFET compact model. The FinFET gate wraps around the fin body behind and in front of the MOS channel (into and out of the page).

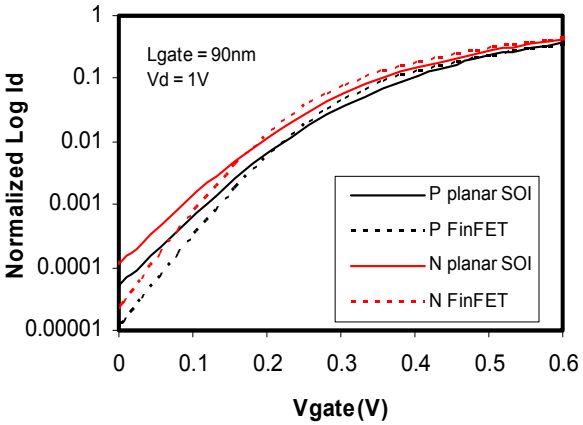

Figure 3 - Planar SOI and FinFET I-V plot. The FinFETs show steeper subthreshold slopes due to the fully-depleted channel.

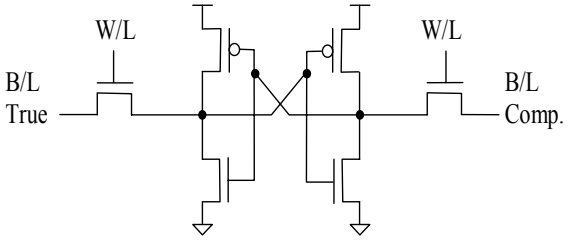

Figure 4 - SRAM cell schematic. In this study, one or more FinFETs replace each planar SOI device.

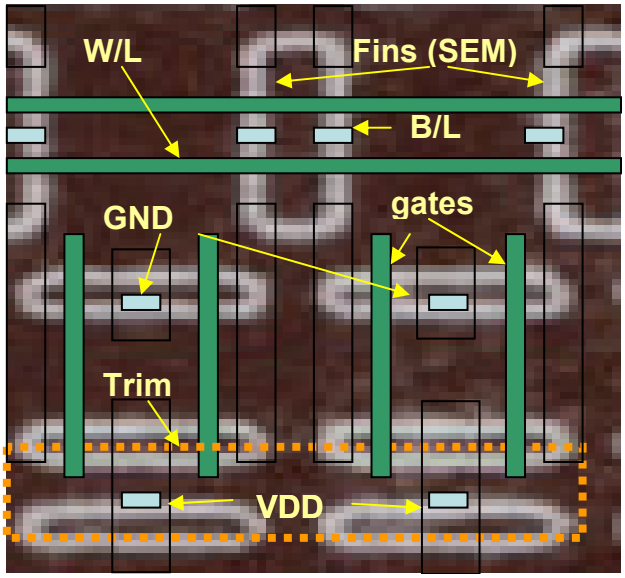

Figure 5 - SEM of fin pattern in silicon is shown with gate, trim, and via levels superimposed. Trim level is used to remove undesired fin sections. Interconnect for the cell is not shown.

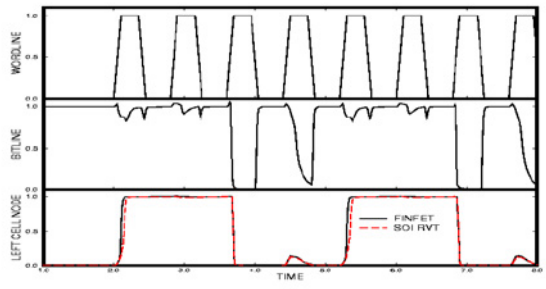

Figure 6 - Typical write operation of the SRAM cell showing the faster FinFET cell node rise time.

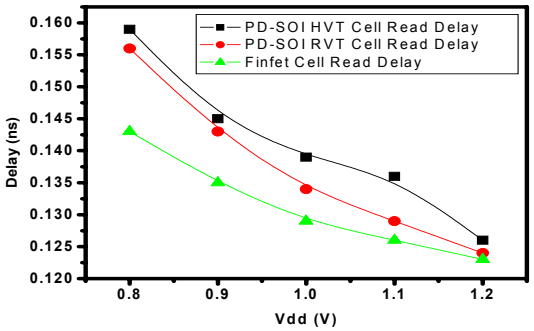

Figure 7 - Read propagation delays through the SRAM cell for FinFET and two planar SOI Vt's.

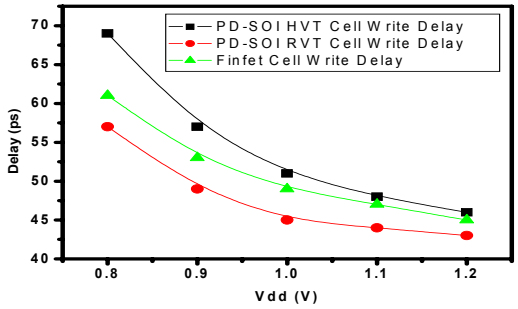

Figure 8 - SRAM cell write delays. Note that GIDL in the FinFETs is insignificant due to the relatively thicker gate oxide.

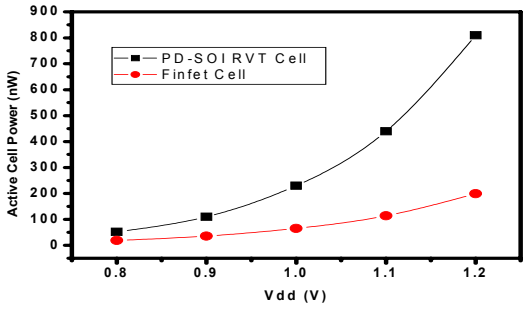

Figure 9 - Dynamic power is reduced because of FinFET fully-depleted characteristics and because transistor design target differences.

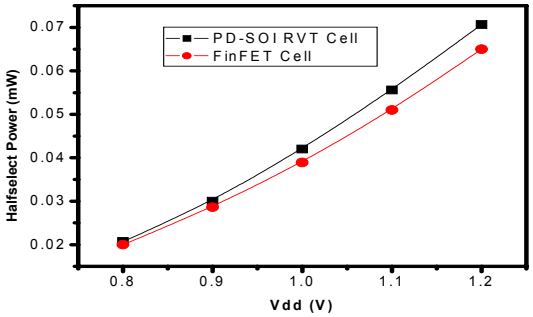

Figure 10 - Dynamic power in the half-select mode is lower due to reduced floating body effects.

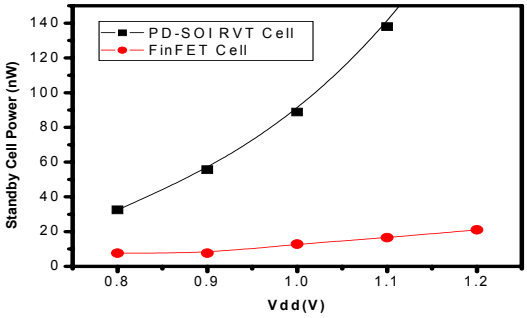

Figure 11 - Standby power used by the SRAM cell is dominated by Ioff which lower in FinFETcell.

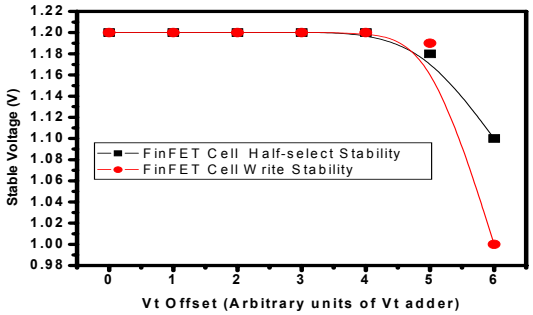

Figure 12 - Vmax analysis shows FinFET cell strength to approximately 5 Vt adder units for the pull-up and pass-gate.

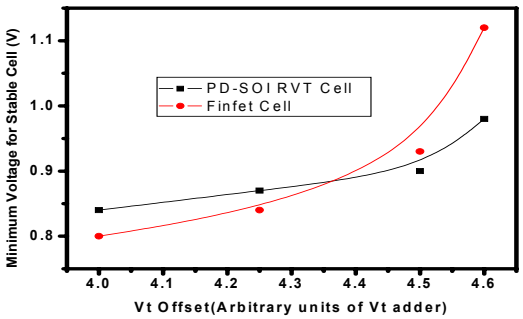

Figure 13 - Crossover of Vmin occurs due to lower relative Vt and drive current in the FinFET cell.