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High-Performance SiGe MODFET Technology

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ABSTRACT

An overview of SiGe modulation-doped field-effect transistor (MODFET) technology is provided. The layer structures and mobility enhancements for both p- and n-channel modulation-doped quantum wells are described and compared to mobilities in Si/SiO_2 inversion layers. Next, previous results on high-performance n- and p-MODFETs fabricated at IBM and elsewhere are reviewed, followed by recent results on laterally-scaled Si/SiGe n-MODFETs with gate lengths as small as 70 nm. We conclude with a discussion of the materials issues for the future vertical and lateral scaling of SiGe MODFETs.

INTRODUCTION

SiGe-based heterostructure bipolar transistors (HBTs) have been the enabling factor in establishing Si-based technology as a viable contender in the rf communications marketplace. While SiGe HBTs are an established commercial technology [1], the steady progress made on SiGe modulation-doped field-effect transistors (MODFETs) in recent years, indicates that these devices hold promise to further expand the capabilities of Si technology for rf and microwave communications applications.

SiGe MODFETs are based upon the principle of using strain to provide carrier confinement and enhanced mobility to improve FET performance. The most common technique for creating these strained layers is to start with a low-defect-density relaxed $Si_{1-x}Ge_x$ buffer layer (grown on a Si substrate) that can then be used as a template for subsequent strained-layer growth [2]. Strained Si layers grown on relaxed SiGe are under biaxial tensile strain, which splits the six-fold conduction-band degeneracy, reducing the in-plane electron effective mass as well as the inter-valley scattering rate [3]. The strain splitting also leads to a staggered band alignment, with the formation of a potential well for electrons [4]. Similarly, a thin $Si_{1-y}Ge_y$ layer grown on $Si_{1-x}Ge_x$ ($y > x$) will be under biaxial compressive strain, leading to splitting in the valence band, reducing inter-band scattering and improving the hole mobility [5]. The band offset created by the strain also produces a confining potential for holes [4]. SiGe MODFETs specifically utilize this carrier confinement to implement the well-known III-V technique of modulation doping [6], whereby the quantum well is separated from dopants in one or both of the barrier regions by a thin undoped spacer layer. This technique efficiently populates the quantum well with minimal additional ionized impurity scattering, and eliminates the adverse effects of surface roughness scattering that occur in surface-channel MOSFETs. In the following section, a description of Si/SiGe/Ge modulation-doped quantum wells and the mobility enhancement that can be obtained in these layer structures is provided.

MOBILITY ENHANCEMENT

Hole mobility

All of the SiGe p-MODFET layer structures produced at IBM have been grown by ultra-high-vacuum chemical vapor deposition (UHV-CVD). Fig. 1 shows a plot of the hole Hall mobility vs. sheet carrier concentration, n_s, for various SiGe p-MODFET structures grown at IBM compared with the hole drift mobility for a Si/SiO_2 inversion layer on a lightly-doped n-Si substrate. The plot shows that the highest mobilities occur as the Ge concentration approaches 100% due to reduced alloy scattering and the lower valence-band effective mass [5]. The hole mobility enhancement compared to Si/SiO_2 inversion layers is about ~ 5-6 for $Si_{0.3}Ge_{0.7}/Si_{0.7}Ge_{0.3}$ [7] and $Si_{0.2}Ge_{0.8}/Si_{0.7}Ge_{0.3}$ quantum wells [8], and > 10 for $Ge/Si_{0.4}Ge_{0.6}$ quantum wells [9]. MBE-grown Ge-channel heterostructures reported by Daimler Chrysler produced similar mobility enhancements [10]. The highest sheet concentrations that have been reported in p-MODFET layer structures are still less 4×10^{12} cm^{-2}, while much higher sheet concentrations ($> 10^{13}$ cm^{-2}) can be achieved in Si/SiO_2 inversion layers.

Electron mobility

Similar to the p-MODFET results described above, all of the n-MODFET layer structures utilized by IBM have been grown by UHV-CVD. Fig. 2 shows a plot of the Si/SiGe n-MODFET Hall mobility, as a function of carrier concentration for various layer structures with different nominal Ge concentrations in the SiGe barriers layers. Early layer structures grown at IBM were optimized for low-temperature mobility, and therefore had thick spacer layers and low carrier concentration [11]. Typical layer structures had barrier-layer Ge concentrations of 25%, and as-measured room-temperature mobility of 2300 cm^2/Vs at $n_s = 4.5 \times 10^{11}$ cm^{-2}. $Si/Si_{0.75}Ge_{0.25}$ layer structures targeted for FET applications have utilized somewhat thinner spacer layers to increase the carrier concentration and reduce the surface-to-channel separation, d_{QW}. A wide variety of these layer structures have been grown with n_s ranging from 1×10^{12} cm^{-2} to 5×10^{12} cm^{-2}. As shown in Fig. 2, at densities around 1×10^{12} cm^{-2}, these layers produce mobilities as high as 2000 cm^2/Vs, but the mobility decreases to about 1000 cm^2/Vs for

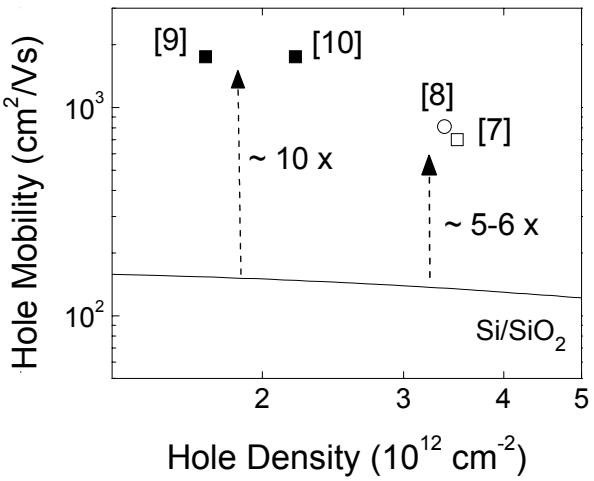

Figure 1. Plot of hole mobility vs. sheet density for various p-MODFET layer structures compared with Si/SiO_2 inversion layers.

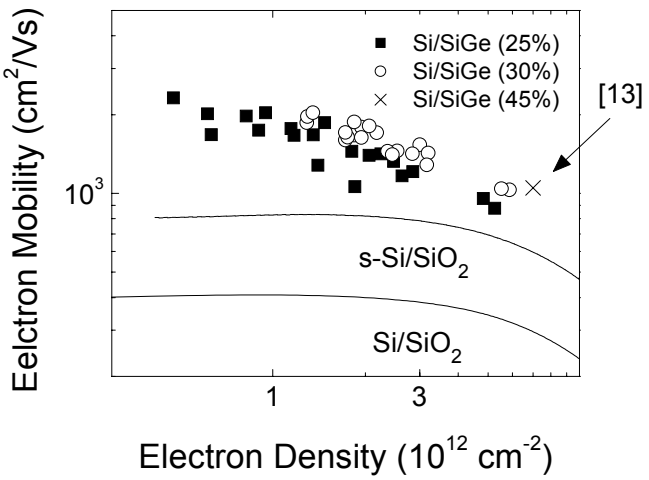

Figure 2. Plot of electron mobility vs. sheet density for various n-MODFET layer structures compared with bulk Si and $Si/Si_{0.7}Ge_{0.3}$ surface-channel MOSFETs.

$n_s = 5 \times 10^{12}$ cm^{-2}. In our more recent device work, quantum wells with barrier Ge concentration of 30% have been utilized [12]. From Fig. 2 it is clear that these layers have improved mobility vs. density characteristics compared to 25% layers. For instance, at $n_s \sim 2 \times 10^{12}$ cm^{-2}, the average mobility using 30% barrier layers is 1800 cm^2/Vs, compared to an average value of only 1600 cm^2/Vs for 25% barriers at the same density. Fig. 2 also shows the results of $Si/Si_{0.55}Ge_{0.45}$ quantum wells grown by MBE at Daimler Chrysler [13]. In addition to the high Ge content, these layer structures utilized top- and bottom-side modulation doping to produce extremely-high sheet densities of 7×10^{12} cm^{-2}, while maintaining a mobility of 1050 cm^2/Vs.

The improvement in the mobility vs. density characteristics with higher Ge concentration is consistent with the analysis of Sugii *et al*. [14]. This work showed that while high mobilities can be obtained for low Ge concentration, the mobility is quickly degraded at higher densities due to population of the parasitic supply layer. The higher barrier-layer Ge concentration increases the band offset, enabling the quantum well to hold more electrons before the parallel path is populated. It is interesting to note that this requirement is different than for strained Si surface-channel MOSFETs. In those devices, the mobility advantage saturates at ~20% [15], since confinement is not necessary for mobility enhancement. Finally, Fig. 2 shows that the mobility enhancement of Si/SiGe MODFET layer structures compared to Si/SiO_2 inversion layers ranges between 3 and 5, and is about 4 at $n_s = 2 \times 10^{12}$ cm^{-2} for $Si/Si_{0.7}Ge_{0.3}$ layer structures. This mobility is also about twice that of strained $Si/Si_{0.7}Ge_{0.3}$ surface-channel MOSFETs at the same density.

MODFET DEVICE RESULTS

p-MODFETs

In recent years, IBM and other groups have made a number of demonstrations of high-performance SiGe p-MODFETs. For instance, Arafa *et al*. reported 0.1 μm gate-length $Si_{0.3}Ge_{0.7}$-channel p-MODFETs with $f_T = 70$ GHz [7]. $Si_{0.2}Ge_{0.8}$-channel p-MODFETs on sapphire substrates have also been fabricated [8] and a diagram of one such device is shown in

Fig. 3(a). These devices had f_T and f_{max} values of 50 GHz and 116 GHz, respectively (Fig. 3(b)), and minimum noise figures, F_{min}, of 0.6 dB (2.5 dB) at 3 GHz (20 GHz). We have also demonstrated the operation of Ge-channel p-MODFETs on $Si_{0.4}Ge_{0.6}$ relaxed buffer layers [9] and a cross-sectional diagram of one such device is shown in Fig. 4(a). These devices produced peak g_m values of 488 mS/mm (687 mS/mm) at room temperature (77 K). As shown in Fig. 4(b), g_m saturated at extremely low bias voltages of V_{ds} ~ 0.3 V (~ 0.15 V) at room temperature (77 K). This is most likely a result of the extremely-high mobility in these structures. More recently, Daimler Chrysler has reported 0.1 μm Ge-channel p-MODFETs with f_T = 52 GHz and f_{max} = 135 GHz, and de-embedded F_{min} values of 0.5 dB at 2.5 GHz and 2.1 dB at 12 GHz [16]. A common characteristic of all the MODFETs described above is that they are Schottky-gated devices. Insulating-gate SiGe p-MODFETs using jet-vapor-deposited SiN_x gates have also been reported by Lu *et al*. [17]. These devices had reduced gate leakage, and improved linearity compared to Schottky gated devices, but also suffered from lower g_m.

n-MODFETs

Since SiGe MODFETs are mainly targeted for rf communications applications, n-channel MODFETs emerge as a better candidate than p-MODFETs due to the higher mobility and higher saturation velocity in the former devices. It has been shown previously that long-channel Si/SiGe n-MODFETs have considerable performance enhancement compared to Si MOSFETs with similar gate dimensions. For instance, Ismail *et al*. fabricated 0.5 μm gate-length devices with g_m = 422 mS/mm [18], as well as 0.4 μm gate-length $Si/Si_{0.7}Ge_{0.3}$ n-MODFETs with f_T = 40 GHz and f_{max} = 56 GHz [19]. More recently, we have demonstrated 62 GHz f_T n-MODFETs with L_g = 0.2 μm and source-to-drain spacing, L_{ds}, of 0.5 μm. Daimler Chrysler also reported a series of results on Si/SiGe n-MODFETs with gate-lengths of 0.25 μm [21], 0.15 μm [22] and 0.1 μm [23], with the latter results including n-MODFETs with f_{max} as high as 188 GHz.

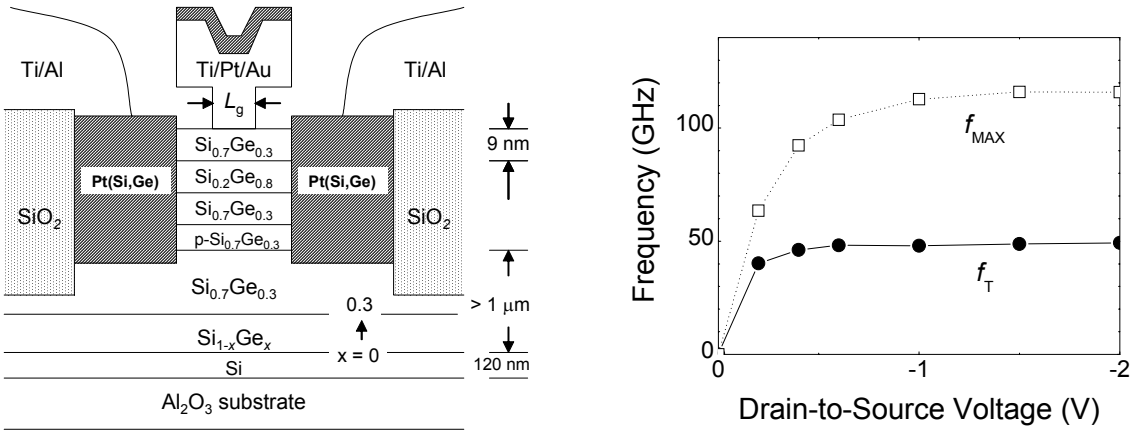

Figure 3. (a) Cross-sectional diagram of a $Si_{0.2}Ge_{0.8}$-channel p-MODFET fabricated on a silicon-on-sapphire substrate. (b) Plot of f_T and f_{max} vs. drain-to-source voltage for the device shown in (a) with L_g = 0.1 μm [8].

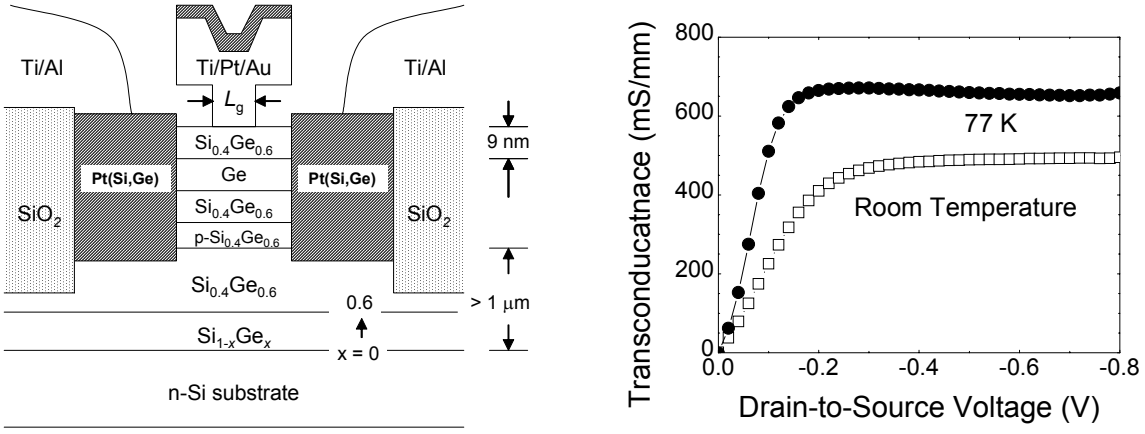

Figure 4. (a) Cross-sectional diagram of a Ge-channel p-MODFET fabricated on a $Si_{0.4}Ge_{0.6}$ relaxed buffer layer [9]. (b) Plot of transconductance vs. drain-to-source voltage for device in (a) with L_g = 0.1 μm at room temperature and 77 K.

Despite the impressive performance demonstrations on long-channel n-MODFETs, Si MOSFET performance has overtaken that of SiGe MODFETs due to the aggressive scaling that has occurred in the industry over the last several years. In fact, MOSFETs with gate lengths as small as 6 nm have been reported [24], while it has only been recently that sub-100 nm gate-length SiGe MODFETs have been reported. These reports include $Si/Si_{0.55}Ge_{0.45}$ n-MODFETs with L_g = 90 nm and f_T = 90 GHz [25] from Daimler Chrysler and $Si/Si_{0.7}Ge_{0.3}$ n-MODFETs with gate lengths as small as 70 nm fabricated at IBM [12]. A cross section of one device from [12] is shown in Fig. 5(a). This device utilized a $Si/Si_{0.7}Ge_{0.3}$ layer structure with Hall mobility of 1800 cm^2/Vs and $n_s = 2.1 \times 10^{12}$ cm^{-2}, and had L_{ds} of only 300 nm. Devices with L_g = 70 nm had f_T and f_{max} of 80 GHz and 175 GHz, respectively, while 80 nm gate-length devices produced values of f_T = 70 GHz and f_{max} = 194 GHz [12].

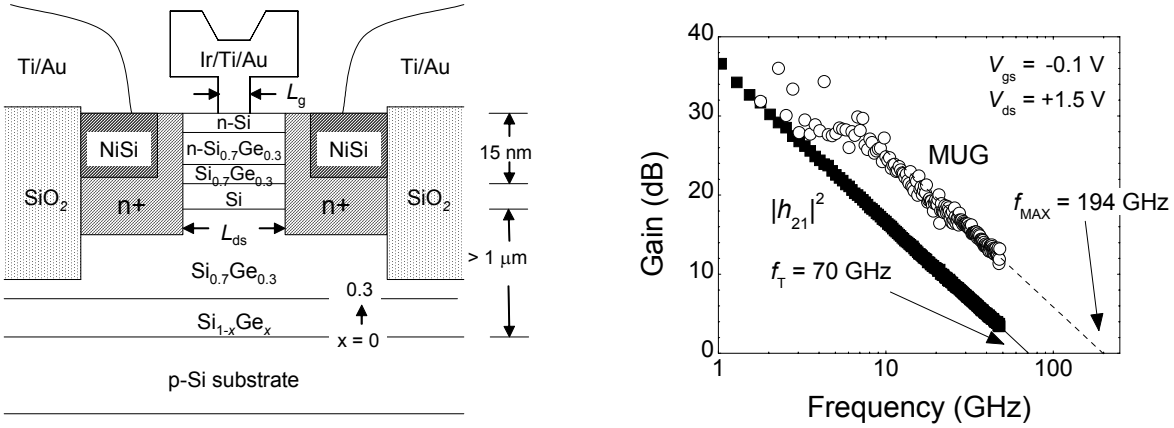

Figure 5. (a) Cross-sectional diagram of a $Si/Si_{0.7}Ge_{0.3}$ n-MODFET. (b) Plot of $|h_{21}|^2$ and MUG vs. frequency for the device shown in (a) with L_g = 80 nm and L_{ds} = 300 nm [12].

MATERIALS ISSUES FOR MODFET SCALING

Despite the impressive rf performance of the Si/SiGe n-MODFETs described above, several device design improvements are needed to achieve better performance at current gate lengths, as well as allow effective scaling to smaller lateral dimensions. First of all, the layer structure needs to be vertically scaled. The layer structures in [12] had quantum well depth, d_{QW}, of 15 nm, which was already reduced from our previous value of 25 nm in [19]. However, for sub-70 nm gate lengths, much shallower quantum well structures are needed. We have recently produced MODFET layer structures with 10 nm deep quantum wells, utilizing a reduced-temperature growth method for the phosphorous-doped supply layer [26]. The Hall mobility vs. temperature characteristics are shown below in Fig. 6, along with results from a 15 nm-deep quantum well with roughly the same carrier density. The 10-nm deep quantum wells displayed nearly identical room-temperature mobility (1750 cm^2/Vs) compared to layers with d_{QW} = 15 nm (1790 cm^2/Vs). The low-temperature results also show no mobility degradation despite the closer proximity of the quantum well to the surface and the doped supply layer. Further scaling of the quantum well layer structure eventually will require delta-doping, which can readily be achieved using MBE, but is difficult using UHV-CVD. Bottom-doping side doping, as is used in p-MODFETs, could allow aggressive vertical scaling, but results in poorer subthreshold characteristics. Eventually, gate leakage current will become a limiting factor for $d_{QW} \sim 5$ nm, and a gate insulator will be needed for further vertical scaling.

The main challenge to lateral MODFET scaling is improving the control of the body potential to improve off-state leakage and reduce short-channel effects. Therefore p-well doping must be utilized, but standard ion implantation through the quantum well cannot be used because the resulting ionized impurity scattering drastically reduces the mobility. Therefore, we have developed a technique where the relaxed buffer layer is implanted with p-well doping, and then the modulation-doped layer structure is grown on top. A cross-sectional TEM of one such layer structure is shown in Fig. 7(a). The layer structure was fabricated as follows. First a relaxed $Si_{0.7}Ge_{0.3}$ graded buffer layer was grown using the usual step-grading technique. Then boron was implanted using a series of implants to produce a roughly constant boron concentration of 10^{17} cm^{-3}. Then the dopants were activated using rapid thermal annealing. Finally, the sample was cleaned and the remaining MODFET layer structure was regrown using UHV-CVD. The distance between the quantum well and the growth interface was kept as small as possible to maximize the effectiveness of the p-well doping.

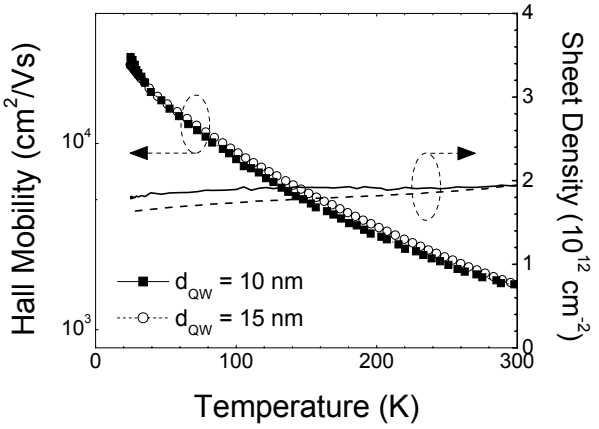

Figure 6. Results of temperature-dependent van der Pauw measurements for $Si/Si_{0.7}Ge_{0.3}$ modulation-doped layer structures with quantum well depths of 10 nm and 15 nm.

To determine the effect of the p-well doping on the electron transport, we performed an experiment where half of an 8" wafer was implanted with boron, while the other half received no implant. Then a MODFET layer structure was regrown on the entire wafer and van der Pauw measurements were performed on both sides. The results are shown in Fig. 7(b). (The room-temperature results on the implant wafer are obscured by the fact that the Hall voltage from both holes in the SiGe buffer layer and electrons in the quantum well tend to cancel each other, leading to an anomalously high electron density and low mobility. However, at low temperatures the contacts to the p-well freeze out, and an accurate comparison of the samples with and without p-well doping can be made.) The results show that the mobility is only minimally affected by the proximity of the quantum well to the p-well doping. However, the p-well doping does deplete the quantum well electrons; for the layer structure shown in Fig. 7(a), where the p-well doping was separated from the quantum well by 25 nm, the carrier density is reduced by ~ 7 x 10^{11} cm^{-2} compared to the sample with no p-well doping. This depletion sets an upper limit on the amount of p-well doping that can be used to control short-channel effects without resorting to a fully self-aligned geometry.

Due to the limitations of p-well doping for MODFETs, it is clear that another method of controlling short-channel effects is needed. From our numerical simulation analysis, the most promising avenue for MODFET scaling to $L_g \leq 50$ nm is to utilize a buried insulating layer. The main materials challenge to realizing SiGe MODFETs on a buried insulator is the ability to produce a high-Ge content (30%) SiGe-on-insulator (SGOI) substrate, and then grow the MODFET layer on top, while minimizing the thickness of the entire structure. We have recently made progress in this direction and the initial results are shown below.

Fig. 8(a) shows a cross-sectional TEM of a SiGe MODFET layer structure grown on a thin SGOI substrate. The SGOI layer has a nominal Ge concentration of 30% and was fabricated using wafer bonding and thinned by chem-mechanical polishing (CMP). The initial thickness after wafer splitting was ~ 300 nm, and the final thickness after CMP thinning was 50 $\pm$ 20 nm, with the large thickness variation being due to CMP non-uniformity. The layer structure was then implanted with boron and annealed to activate the dopants. Then the wafer was cleaned and a MODFET layer structure grown on top. The quantum well was separated from the growth

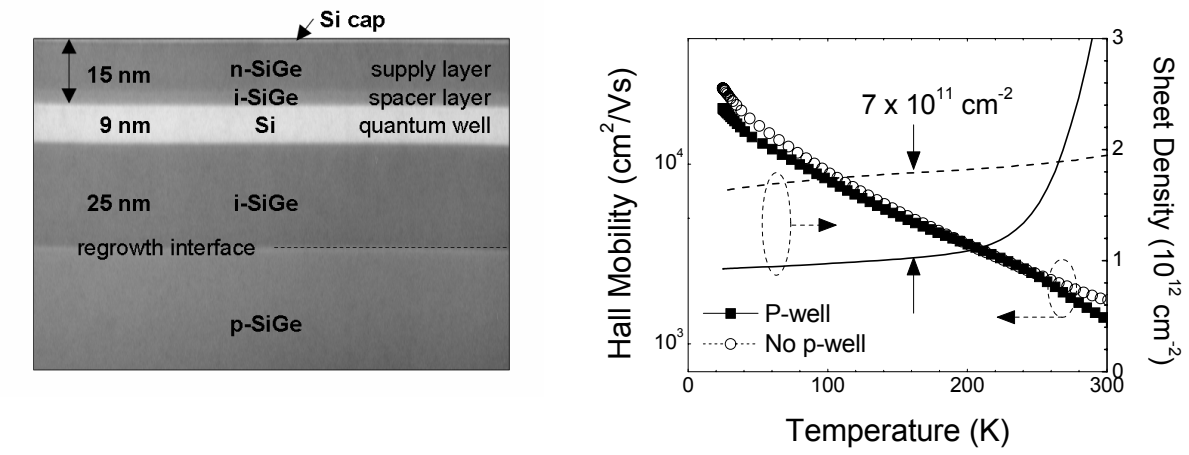

Figure 7. (a) Cross-sectional TEM micrograph showing a MODFET layer structure regrown on a p-type-implanted SiGe buffer layer. (b) Comparison of electron density and mobility for p-MODFET layer structures regrown on buffer layer with and without p-well doping.

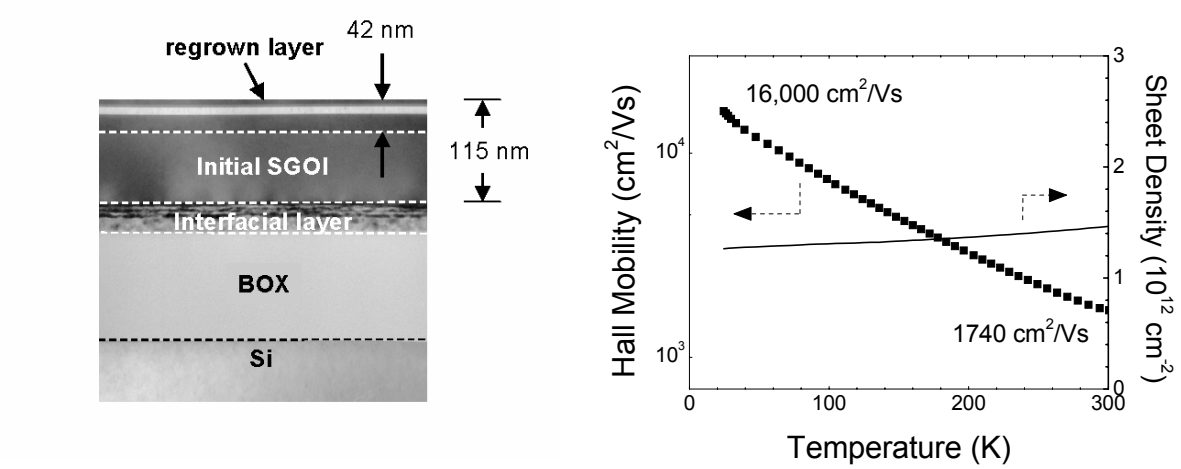

Figure 8. (a) Cross-sectional TEM micrograph of a thin SGOI MODFET layer structure. (b) Hall mobility and sheet density vs. temperature for same layer structure as in (a).

interface by < 20 nm, and the total thickness of the SGOI layer after regrowth was 115 nm. This value is considerably less than SGOI MODFET layer structures reported previously [27]. The results of van der Pauw measurements on these layers are shown in Fig. 8(b). The measured Hall mobility was 1740 cm^2/Vs at room temperature with a corresponding sheet density of 1.5 x 10^{11} cm^{-2}. The mobility at 25 K was 16,000 cm^2/Vs. The ability to reduce the SGOI thickness was limited due to an interfacial layer that formed due to intermixing of the SiGe with the underlying buried oxide layer. We have recently made improvements in the SGOI substrates, and similar room-temperature mobilities have been obtained on SGOI MODFET layers with total thickness of only 74 nm [28].

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