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I. The SOI Advantage

Silicon-on-insulator (SOI) technology has matured over the past 15 years to become production-worthy for advanced CMOS manufacturing [1], for applications ranging from high-end servers like IBM's PowerPC and AMD's Opteron to ultra-low-power systems like Seiko and Oki's chips for watches. Conventional silicon VLSI processing is based on bulk silicon substrates. When CMOS transistors are built into a thin silicon film on the order of 0.1μm on top of an insulating silicon dioxide layer, the source and drain junction capacitance is greatly reduced. As a result, SOI CMOS circuits switch faster and use less power than conventional bulk CMOS. The power-delay advantage obtained from substrate material innovation has become particularly important as conventional CMOS scaling reaches its limit.

BiCMOS is the preferred technology platform for many wireless and communication applications which need both RF/analog functions from bipolar transistors and low-power digital functions from CMOS transistors. From a mixed-signal system perspective, SOI is attractive due to the insulating nature of the substrate, which can provide RF noise isolation between digital and RF/analog components, particularly when a thick insulator or high resistivity substrate is used [2], or when substrate engineering is applied [3]. The reduction of substrate loss also enables fully-integrated high quality-factor passive elements for communication systems [2].

The challenge for SOI BiCMOS integration arises from a fundamental device architectural difference between bipolar and CMOS. Unlike CMOS transistors where current flows in a superficial silicon layer from source to drain, in high-speed vertical bipolar transistors including all SiGe HBTs, electrons flow vertically from the emitter on the top to the collector on the bottom. In order to have low resistance access to the collector from a contact electrode on the top, a sub-collector layer on the order of 1-2μm thick with heavy doping is needed underneath the collector, which makes it too thick to build on thin silicon film SOI. Past approaches to SOI BiCMOS integration either used a thick silicon layer on a bonded SOI substrate to accommodate the vertical bipolar transistors or used lateral bipolar transistors on thin silicon film SOI. In the thick SOI case, the CMOS transistors have the same source and drain junction capacitances as those on a conventional bulk substrate and thus have no power-delay advantage. Digital BiCMOS technology on 1-1.5μm silicon film SOI was developed for soft-error immune processors [4, 5]. More recently, a SiGe HBT/CMOS technology on 1μm silicon film SOI was developed for RF and mixed signal applications, featuring integrated high-Q inductors [2]. For such thick-silicon SOI BiCMOS, deep trenches are employed to isolation the bipolar transistors from the bulk-like CMOS devices. The lateral SOI bipolar has limited speed due to base width control and is not compatible with SiGe epitaxy. It is noteworthy that process innovations to minimize the base width and base resistance have kept improving the speed of lateral SOI bipolar transistors over the years [6-8]. With f_T up to 20GHz, it still can not compete with vertical bipolar transistors (not to mention SiGe HBTs) in terms of performance, but it may provide a low cost solution for mobile wireless communications due to a simpler and more CMOS-compatible manufacturing process [7].

Recently, a novel vertical bipolar transistor suitable for integration on CMOS-compatible SOI was proposed and npn transistors with SiGe base were demonstrated on 0.12μm SOI [9-12].

The remainder of this chapter is dedicated to the concept, manufacturing process, electrical characteristics and future prospects of this new transistor.

II. Vertical Bipolar Transistors on Thin SOI

High-performance vertical bipolar transistors consist of an n+ emitter region, a p-type base region and an n-type collector region stacked atop one another. The base and emitter regions can be built on top of the SOI substrate by epitaxial growth of a silicon-germanium base layer followed by LPCVD deposition of a polysilicon emitter film, like in most SiGe HBT's. Thus the silicon film of the SOI substrate needs to accommodate only the collector part. In conventional vertical bipolar, typically a thick n+ type subcollector region and an n+ reachthrough region are used to bring the collector contact to the silicon surface in order to minimize collector series resistance. The subcollector is placed deep enough to leave a quasi-neutral region of n-collector between the subcollector and collector space-charge region (or depletion region), such that the collector-base capacitance is not increased. This conventional collector structure would require an SOI substrate with a silicon film thickness (T_{SI}) of at least 1μm, as illustrated in Fig. 3.3.1(a).

The silicon film thickness requirement is greatly relaxed if we omit the thick n+ subcollector layer, as shown in Fig. 3.3.1(b). The lower bound of T_{SI} is determined by the depth of the depleted collector region (W_C). For a collector doping concentration (N_C) of $10^{17}/cm^3$ and a reverse collector-base junction bias of 2V, W_C=0.19μm, which approaches the range of Tsi for SOI CMOS devices. However, the collector current is carried laterally towards the n+ reachthrough in the thin quasi-neutral layer above the buried oxide which is very resistive. The collector series resistance from the quasi-neutral layer is inversely proportional to $N_C \cdot (T_{SI}-W_C)$ and can be more than 10^3 times higher than that of a heavily doped 1μm-thick subcollector layer.

A more radical reduction of T_{SI} to below collector depletion thickness W_C leads to a new vertical bipolar transistor, as shown in Fig. 3.3.1(c). The collector underneath the base and above the buried oxide is fully depleted. The fully-depleted collector not only eliminates the resistive quasi-neutral layer but also results in a reduced base-collector junction capacitance (C_{CB}) due to its serial connection with a small capacitance from the thick buried oxide layer. To minimize collector series resistance, the n+ reachthrough should be placed as close as possible to the depleted collector region. However, it's desirable to leave a narrow quasi-neutral region in-between such that the proximity of n+ reachthrough does not limit C_{CB} or the breakdown voltage of the device.

The new device structure in Fig. 3.3.1(c) is similar to bending the vertical collector structure in Fig. 3.3.1(a) by 90 degrees such that most of the vertical collector stack including the lower part of collector depletion region, the quasi-neutral collector region and the n+ subcollector region rest on the side of the upper part of collector depletion region. Under forward active mode, electrons injected from the emitter, instead of flowing vertically down towards the subcollector layer as in a typical vertical bipolar transistor, are guided by the two-dimensional electric field in the collector depletion region and make a turn towards the n+ reachthrough on the side, see dotted lines indicating electron transit path in Fig. 3.3.1(c).

The new device concept overcomes the T_{SI} limit for integrating SiGe HBT with SOI CMOS. For a given T_{SI} which is usually dictated by CMOS scaling requirement, there is an upper limit to the collector doping concentration that satisfies $W_C<T_{SI}$. To maximize the high-frequency performance of the HBT, an N_C near this limit can be used to delay the onset of base push-out, or Kirk effect.

III. Voltage Pinning in a Fully-Depleted Collector

In this section, a simple one-dimensional theory is used to analyze the onset condition of full collector depletion, as a function of the physical structure (T_{SI}, N_C) and bias conditions (V_B, V_C and V_S for base, collector and SOI substrate respectively). The unique characteristic of collector voltage pinning and its consequence on bipolar device operation will be highlighted.

For simplicity, consider part of the SiGe HBT structure, with base, collector, n+ reach-through and SOI substrate, as illustrated in Fig. 3.3.2 (a). Due to the symmetry, along the central cut line, the electric field is vertical and the potential distribution can be solved exactly using one-dimensional Poisson's equation. The problem is simply a p/n diode in series with a MOS capacitor. Figure 3.3.2 (b) illustrates the band diagram along the cut line for the case where both the p/n diode and MOS capacitor are reverse-biased ($V_B<V_C$, $V_S<V_C$), with two distinct depletion regions of width y_1 and y_2 respectively ($y_1+y_2 < T_{SI}$). Figure 3.3.2 (c) illustrates the electric field distribution along the same cut line. The voltage in the collector quasi-neutral region follows V_C of the n+ reach-though regions. Increase of collector voltage widens both depletion regions and at certain critical voltage V_C', the two depletion regions merge. Increase of collector voltage beyond V_C' no longer influences the vertical field. The potential well along the center line has a fixed depth determined by V_C'. This is referred to as collector voltage pinning. Away from the center line, the additional voltage V_C-V_C' increases the lateral field.

The critical collector voltage can be solved analytically using depletion approximations for both the p/n diode and the MOS capacitor. For the base/collector diode, assuming one-sided abrupt junction, depletion width y_1 is described by:

$$V_C - V_B + V_{BI} = \frac{q}{2\varepsilon_S} N_C y_1^2 \ , \qquad (1)$$

where V_{BI} is the diode built-in potential. For the MOS capacitor, the depletion width y_2 near the buried oxide is described by:

$$V_S - V_C - \phi_{MS} = V_{OX} + V_{SI} = -\frac{qN_C y_2}{C_{OX}} - \frac{q}{2\varepsilon_S} N_C y_2^2 \ , \qquad (2)$$

where ϕ_{MS} is the work function difference between the p+ substrate of SOI and the n-collector, V_{OX} and V_{SI} are the potentials dropped across the buried oxide and the collector depletion region (y_2) respectively. The critical collector voltage V_C' that fully depletes the collector, i.e., $y_1+y_2=T_{SI}$, can be solved based on equations (1) and (2):

$$V_C^{'} = V_B - V_{BI} + \frac{q}{2\varepsilon_S} N_C \cdot (y_1^{'})^2 \le V_{CM}^{'} = V_B - V_{BI} + \frac{q}{2\varepsilon_S} N_C \cdot T_{SI}^2 \ , \qquad (3)$$

where y_1' is the value of y_1 at the onset of full depletion:

$$y_1^{'} = T_{SI} \cdot \left(\frac{1/C_{OX} + 1/(2C_S) - (V_B - V_S + \phi_{MS} - V_{BI})/qN_C T_{SI}}{1/C_{OX} + 1/C_S} \right) \ , \qquad (4)$$

$C_S=\varepsilon_S/T_{SI}$ and $C_{OX}==\varepsilon_{OX}/T_{BOX}$. For thick buried oxide ($C_{OX} \ll C_S$) and low substrate biases ($V_S \approx V_B$), the depletion region due to the MOS capacitor is narrow and $y_1' \approx T_{SI}$. In general, when the MOS capacitor is under flatband condition and the collector is fully depleted from the p/n diode ($y_1'=T_{SI}$), the critical collector voltage reaches the maximum value of V_{CM}'. More negative substrate bias induces a depletion region near the buried oxide, which has the effect of lowering the critical collector voltage via a smaller y_1'. In the other direction, under more positive substrate bias, the MOS capacitor is under surface accumulation condition, i.e., electrons accumulate near the buried oxide interface. The accumulation layer is linked to the n+ reach-through regions and acquires the collector potential V_C. This breaks the collector voltage pinning. The vertical potential drop again follows the collector voltage. The accumulation layer acts like an ultra-thin subcollector which is shown to significantly enhance the speed of the SOI SiGe HBTs in section V. We call this novel structure with depleted collector directly on accumulated back surface the accumulation-subcollector transistor.

For any SOI bipolar structure, there are four distinct types of collector depending on the bias condition: I) fully-depleted collector; II) partially depleted collector with depleted back surface; III) partially depleted collector with accumulated back surface and IV) depleted collector on accumulated back surface, (accumulation subcollector). The bias condition that defines the collector type is shown in Fig. 3.3.3 for an SOI bipolar device with T_{SI}=120nm, T_{BOX}=140nm, N_C=1.5×10^{17}/cm^3, which is used in the experiment described in section IV. The boundary between regions I and II is described by Equation (3). The single point that borders all four regions corresponds to the condition that y_1'=T_{SI} in Equation (4). It's noteworthy that in the fully-depleted collector region, reduced vertical potential drop due to the negative substrate bias can lead to effective forward biasing of the B-C junction (V_C'<V_B) for an apparent reverse bias condition (V_C>V_B), as shown by the shaded area. This region gives rise to collector saturation and should be avoided in circuit applications.

There is a well-known trade-off between the speed (f_T) and the breakdown voltage (BV_{CEO}) of a traditional bipolar transistor, from the vertical scaling of the collector depletion layer [13]. The voltage swing of a high speed device is constrained by the breakdown voltage. We can design an SOI bipolar device such that the collector voltage is pinned at a value below the BV_{CEO} of a bulk device with the same collector doping. The SOI device is expected to have improved BV_{CEO} as well as Early voltage V_A. Avalanche multiplication and breakdown is sensitive to the maximum electric field (E_{MAX}) near the B-C junction interface. In a bulk device, E_{MAX} increases with collector voltage as a function of $\sqrt{V_C - V_B + V_{BI}}$, whereas in the fully-depleted collector device, it's pinned at (qN_C/ε_S) ·y_1', independent of collector voltage. Thus avalanche effect progresses more slowly with increasing collector voltage in a fully-depleted collector device than a bulk device. Avalanche breakdown is delayed to higher collector voltage in the SOI device where the lateral field becomes large enough to raise E_{MAX}. The depletion

width on the base side is determined by E_{MAX}, which does not change with collector voltage in the fully-depleted collector device. Therefore the modulation of quasi-neutral base width by the collector voltage is much weaker than that of a bulk device, which results in a higher V_A.

In an accumulation-subcollector device [region IV in Fig. 3.3.3], the B-C junction reverse bias is dropped over T_{SI} whereas in a bulk device the same reverse bias is dropped over a larger distance, or $W_C > T_{SI}$ if collector doping concentrations are the same. This means higher E_{MAX} and somewhat degraded BV_{CEO} and V_A in an accumulation-subcollector device. The difference in the maximum field is:

$$E_{MAX}^{SOI} - E_{MAX}^{Bulk} = \frac{qN_C}{\varepsilon_S} \cdot \frac{W_D - T_{SI}}{T_{SI}} \quad . \tag{5}$$

IV. Making SiGe HBTs on Thin SOI Substrate

Figure 3.3.4 shows process flow diagrams for building npn SiGe HBTs on SOI substrate. The silicon film thickness for SOI CMOS has been scaled down from about 0.2μm to below 0.1μm, along with channel length scaling. The new SiGe HBT is expected to be scalable to thinner SOI substrate as will be discussed in section VI. In the experiment, we used the same SOI substrate that is used for a 130nm SOI CMOS technology [14], which has a silicon thickness of 0.12μm and a buried oxide thickness of 0.14μm. After shallow-trench isolation, a phosphorus implant is introduced to define the collector doping concentration in the silicon area. It can be a blanket implant in a bipolar-only process, or a masked implant in a BiCMOS flow. Both a uniform doping profile and a low-high retrograde doping profile were exercised. Then a mask is used for a high dose phosphorus implant that defines a n+ reach-through region surrounding the n-type collector in the middle. The mask dimension determines the length of the n-collector, L_C, which was varied in the experiment to evaluate its effect on collector resistance and breakdown behaviors.

Next, a dielectric stack, followed by a heavily doped p+ polysilicon layer, is deposited over the wafer. The p+ polysilicon will provide low resistance contact to the base and the dielectric stack is served as an insulator between the p+ polysilicon and the collector. The thickness of the insulator should be optimized as it contributes to parasitic collector-base capacitance. The parasitic C_{CB} could dominate in a fully-depleted collector device as the collector-base junction capacitance is minimized. The use of a thicker insulator reduces C_{CB} but creates more topography later in the process that can increase the base resistance. Then a window is etched into the polysilicon and insulator to expose the silicon surface for epitaxial growth of the SiGe base layer. The window size, L_B, should be minimized while providing enough room for a defect-free SiGe base region. The SiGe base layer was grown by a non-selective low-temperature epitaxy (LTE) process using UHV/CVD tools. During the LTE process, polysilicon is grown on the sidewalls of the dielectric window which provides the link between the SiGe base layer and the overhanging p+ polysilicon layer.

Next, a second dielectric stack is deposited which will serve as an insulator between the base and the emitter. An emitter window mask is used to etch an opening in the dielectric stack, and a layer of in-situ arsenic-doped polysilicon layer is deposited that becomes the n+ emitter. Due to two-dimensional electric field in the depleted collector region, the electrons coming down through the middle of the emitter window will have a longer lateral drift path in the depleted collector than those from the edge of the emitter window. The speed of the SOI device is expected to degrade at large emitter width. Simulation results suggest that a good rule of thumb is to keep W_E less than Tsi/2. Two more mask levels are then used to pattern an n+ polysilicon emitter region and a p+ polysilicon base region respectively. Cobalt silicide is formed over the p+ base and n+ collector regions to reduce access resistance to the intrinsic base and collector of the device. Finally contacts to the n+ emitter, p+ base and n+ collector reach-through are etched

open. It should be noted that the deep subcollector implantation and drive-in, the n-type epitaxial silicon growth, and the deep-trench isolation process steps associated with fabrication of a conventional vertical bipolar transistor are not needed in fabricating the thin-SOI bipolar.

Figure 3.3.5 shows an SEM micrograph of an SOI SiGe HBT, after contacts to the emitter, base and collector are opened. The mask dimensions of emitter width, LTE window and collector length are 0.16μm, 0.5μm and 1.2μm respectively. The collector doping profile is uniform, with $N_C=1.5\times10^{17}/cm^3$. Devices with smaller L_B and L_C designs and different collector doping profiles were also fabricated.

V. Characteristics of SOI SiGe HBTs

In this section, electrical characteristics of the manufactured thin-SOI SiGe HBTs will be reviewed, with a focus on the breakdown behavior in the depleted collector SOI device as well as the substrate bias effect on both the DC and AC performance.

Figure 3.3.6 shows the Gummel plot and the output I_C-V_{CE} characteristics, with substrate bias, V_{SE} (referenced to the emitter voltage), as a parameter which is varied from -5V to 20V. The Gummel plot shows a peak current gain of over 400. Since the base and emitter process are borrowed from a bulk SiGe technology [15], the current gain is similar to that of the bulk devices. The substrate bias has an effect at emitter-base forward biases higher than 0.9V. The opposite movement in I_B and I_C is a signature of collector saturation effect where the forward biasing of collector-base junction reduces I_C while contributing to more I_B. A positive substrate bias suppresses this saturation effect by increasing the vertical potential drop in the collector that prevents electrons from back injection into the base. The I_C-V_{CE} in part (b) shows almost identical turn-on behaviors under zero and positive substrate biases, whereas under the negative substrate bias, it requires higher collector voltage to turn on the device, another manifestation of

saturation effect. This is consistent with Figure 3.3.4, which predicts an effectively forward biased B-C junction (V_C'-V_B<0) when V_S-V_B<-2V.

As expected from the voltage pinning effect, BV_{CEO} is the highest at 5.5V under zero substrate bias. The reduction of BV_{CEO} at V_{SE}=20V is due to the accumulation subcollector that breaks the voltage pinning and creates a vertical potential drop of V_{CB} across T_{SI}. In contrast, at V_{SE}=5V, avalanche current turns on at the same V_{CE} as the high positive bias case, but the rate of increase with collector voltage is slower. This can be explained by Fig. 3.3.3. Under low positive V_{SE}, as V_{CE} increases, the collector makes a transition from the one with an accumulation subcollector (region IV) to a fully depleted collector (region I). The transition decouples the collector voltage to the maximum electric field at the B-C junction interface and results in a much slower increase of avalanche current with V_{CE}.

For the same collector design, BV_{CEO} depends on the current gain (I_C/I_B) due to the bipolar effect. A more direct examination of avalanche multiplication is through the measurement of the 'M-1' factor [16]. In this measurement, a constant forward emitter current (I_E) is forced through the device while ramping up the collector voltage. The electron-hole pairs generated by impact ionization in the collector depletion region contribute to an increase in the collector current and a corresponding reduction in the base current (ΔI_C=-ΔI_B). The factor 'M-1' is extracted as $|\Delta I_B|/I_E$. Figure 3.3.7 (a) compares the avalanche multiplication in an SOI SiGe HBT to two bulk SiGe HBTs with 90GHz-f_T (open symbols) and 50GHz-f_T (solid symbols) respectively. In bulk devices, avalanche multiplication has the similar exponential dependence on V_{CB}. The 90GHz device has a 'M-1' which is ~6× higher than the 50GHz device due to heavier collector doping concentration as a part of vertical scaling. The SOI device shows a much weaker dependence of 'M-1' on V_{CB} under zero substrate bias, or under positive substrate bias in the high V_{CB} range. This corresponds to bias conditions for a fully-depleted collector. In

the open-base configuration, the increase of collector current due to avalanche effect is multiplied by the current gain β of the bipolar transistor. When β·(M-1)=1, the collector current is doubled from its low V_{CB} value, which can be used as a measure for device breakdown. The flat portion of the 'M-1' data suggests that it's possible to significantly increase the BV_{CEO} of a fully-depleted collector device by reducing the current gain from ~400 in the experimental hardware to about 100. Under positive substrate bias and in the low V_{CB} range, which corresponds to the accumulation sub-collector condition, 'M-1' is nearly the same as the 50GHz bulk device. Under negative substrate bias, the exponential rise of 'M-1' suggests that the lateral field dominates avalanche multiplication in the saturated collector region where there is minimum vertical potential drop in the collector. Figure 3.3.7(b) shows that the SOI devices and the bulk devices have a different 'M-1' vs. f_T trade-off. The peak f_T of the SOI devices can be improved by applying positive substrate biases without much increase of avalanche multiplication, while scaling N_C in a bulk device results in a steeper penalty in 'M-1', or breakdown voltage.

The f_T and f_{MAX} characteristics of a SOI SiGe HBT are shown in Fig. 3.3.8, along with those of a lateral SOI bipolar device as a reference [6]. The SiGe HBT shows a 2.5× to 4.5× improvement in peak f_T, depending on the substrate bias condition. The maximum oscillation frequency, f_{MAX}, on the other hand, is less sensitive to the substrate bias. This is expected from the $f_{MAX} \propto \sqrt{f_T / C_{CB}}$ dependence. As V_{SE} increases, C_{CB} increases as the collector makes a transition from a fully-depleted one to the one with an accumulation subcollector. A 30% increase of f_T is observed for a V_{SE} change from 0V to 5V, while there is minimal change in f_{MAX}. This suggests that C_{CB} increases by ~30% due to the presence of an accumulation back surface. To understand the strong dependence of f_T on V_{SE}, it's instructive to look at the two-dimensional potential distribution in the collector depletion region. Figure 3.3.9 shows

simulated equi-potential contours in the forward active mode with V_{CB}=1V and V_{BE}=0.84V. The potentials V_I are referenced to the vacuum level in the emitter. The boundaries of the collector depletion region is defined approximately by V_I=-4V at the base side and V_I=-2.5V at the n+ reachthrough side. At zero substrate bias (V_{SE}=0V) in part (a), the collector is fully depleted under the base and there is little potential drop along the vertical direction. The arrow indicates the electron drift path along the electric field direction. It's mostly lateral with a length of ~0.5μm. At 20V substrate bias (V_{SE}=20V), the potential at the back interface is fixed at V_I=-2V, the same potential as the n+ reachthrough region. The large substrate bias attracts a majority carrier accumulation layer with an electron concentration of $(V_S-V_C-V_{BI})/qC_{OX}=2.7\times10^{12}$ /cm^2. The accumulation layer serves as an ultra-thin subcollector which provides a low resistance path to the n+ reachthrough. It also helps to reduce the collector series resistance in the reachthrough region. The electron drift path becomes vertical and much shorter, on the order of the SOI film thickness, or 0.1μm. The shortened drift path results in a transit time $\tau_{BC}=W_{dBC}/2v_{SAT}$ reduction of about 2 pico-seconds, which accounts for 80% of the f_T improvements. The remaining improvement comes from the reduction of collector series resistance from the accumulation subcollector.

Similar f_T improvement may be obtained at a much lower substrate bias if the buried oxide is scaled down. For future SOI-CMOS technology, the ability to use a back gate voltage to control the CMOS threshold voltage is desirable for compensating chip-to-chip process variations. This can drive the scaling of buried oxide thickness to below 20nm. On an SOI substrate with relatively thin buried oxide, it would suffice to connect the SOI substrate of the bipolar portion to the highest supply voltage V_{CC} (~3V) for the analog/RF circuits to get the benefit of an accumulation subcollector. Use of n+ substrate instead of p+ substrate would further lower the required substrate bias by about 1V. In lieu of an accumulation subcollector, a

retrograde collector doping profile with low concentration near the base and high concentration near the buried oxide can simulate some of the accumulation subcollector effect, albeit the doping gradient is limited by the diffusion process and is much less ideal. Experimental hardware with a retrograded collector doping profile measured a 60GHz f_T at zero substrate bias [10]. The ECL ring oscillator operation has been demonstrated using SiGe SOI bipolar transistors, with a minimum delay time of 18 pico-seconds per stage for a logic swing of 300mV [10].

VI. Process Optimization, Device Scaling and Complimentary Bipolar

This section will highlight the opportunities for some future work on the SOI SiGe HBTs. First, there are several process development opportunities for enhancing the device speed while maintaining the benefit of high breakdown voltage which includes (1) self-alignment of the LTE window to the n+ reach-through region; (2) minimizing the 'facet' region near the edge of the epitaxial layer such that the LTE window size (L_B) can be reduced for the same emitter width; and (3) self-alignment of the emitter opening to the base layer. All these steps would facilitate closer placement of the n+ reach-through to the center of the device to reduce the lateral drift path in a fully-depleted collector. A buffered region of intermediate doping concentration between the n+ reach-through and the n-collector would also help to reduce the lateral drift path while maintaining the same collector voltage pinning under the base.

For SOI-CMOS, the trend in lateral (lithography dimensions) and vertical (T_{SI}) scaling is expected to continue. We will show that the RF performance of the SOI bipolar device will benefit from this scaling trend as well. Table I shows the effect of scaling on the collector depletion layer drift length W_{dBC} and collector delay time $R_C \cdot C_{CB}$ for three types of collectors: fully-depleted, depleted with accumulation subcollector and partially depleted. Independent lateral and vertical scaling factors, α and β (both <1) respectively, are assumed. A good

guideline is to increase the collector doping concentration (N_C) by $1/\beta^2$, such that the collector depletion width is reduced by the same factor β as T_{SI}. A fully-depleted collector remains fully depleted after scaling, with a shorter lateral drift path determined by the lateral scaling factor α. For the accumulation subcollector and partially-depleted collector devices, in addition to a reduction in the vertical drift path by β, the collector resistance reduction results in a RC delay time reduction of up to a factor of α^2. Thus even the partially depleted device can be an attractive option after significant reduction in RC delay time. Simulation results suggest at 100nm emitter width, 200GHz f_T can be achieved on 55nm SOI substrates using a collector doping concentration of $2.4\times10^{18}/cm^3$. The guideline for N_C scaling will be eventually limited by the base-collector band-to-band tunneling current and the collector breakdown voltage. Though the speed of SOI SiGe HBT will not be as high as the most advanced bulk SiGe HBT, it will be adequate for most of the RF/wireless applications.

Compared to bulk SiGe HBTs, the SOI device features a simpler manufacturing process as deep trench isolation and epitaxial collector are not necessary and the deep sub-collector is omitted. The full dielectric isolation of each transistor by shallow-trench and the SOI substrate provides a lower cost opportunity to make both vertical npn and vertical pnp bipolar transistors on the same chip, see an illustration in Fig. 3.3.10. In bulk technologies, usually only vertical SiGe npn and lateral Si pnp transistors are available, the latter simply as two back-to-back connected p/n diodes which have very low performance. The availability of a high performance vertical SiGe pnp transistor should provide innovation opportunities in analog circuit design for significant performance improvement and power saving.

VII. Summary

We presented a new class of vertical SiGe HBTs that is compatible with SOI-CMOS. The unique feature of collector voltage pinning in thin silicon film was discussed in depth which

gives rise to high breakdown voltage, high Early voltage and low collector capacitance. The SOI device is promising for a better f_T-BV_{CEO} trade-off than that from conventional collector scaling in bulk devices. The fabricated devices show the anticipated strong dependence of DC and RF characteristics on SOI substrate bias. The relatively low speed of a fully-depleted collector device can be significantly enhanced by a positive substrate bias for an accumulation subcollector operation. The new device is expected to scale well with SOI-CMOS and can enable complementary SOI-BiCMOS with the possibility of a high-performance pnp transistor.

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REFERENCES

1. G. G. Shahidi, 'SOI technology for the GHz era,' IBM J. Research and Development, Vol. 46, No. 2/3, pp. 121-131 (2002).
2. K. Washio, E. Ohue, H. Shimamoto, K. Oda, R. Hayami, Y. Kiyota, M. Tanabe, K. Kondo, T. Hashimoto, and T. Harada, 'A 0.2-μm 180GHz f_{MAX} 6.7-ps-ECL SOI/HRS self-aligned SEG SiGe HBT/CMOS technology for microwave and high-speed digital applications,' IEDM Tech. Digest, pp. 741-744 (2000).
3. J.N. Burghartz, M. Bartek, B. Rajaei, P.M. Sarro, A. Polyakov, N.P. Pham, E. Boullard, K.T. Ng, 'Substrate options and add-on process modules for monolithic RF silicon technology,' Proc. BCTM, p. 17-23 (2002).
4. T. Hiramoto, N. Tamba, M. Yoshida, T. Hashimoto, T. Fujiwara, K. Watanabe, M. Usami, T. Ikeda, 'A 27-Ghz double polysilicon bipolar technology on bonded SOI with embedded

58μm^2 CMOS cells for ECL-CMOS SRAM applications,' IEDM Tech. Digest, pp. 39-42 (1992).

5. T. Hashimoto, T. Kikuchi, K. Watanabe, N. Ohashi, T. Saito, H. Yamaguchi, S. Wada, N. Natsuaki, M. Konda, S. Konda, Y. Homma, N. Owada, T. Ikeda, 'A 0.2μm bipolar-CMOS technology on bonded SOI with copper metallization for ultra high-speed processors,' IEDM Tech. Digest, pp. 209-212 (1998).
6. G. G. Shahidi, D.D. Tang, B. Davari, Y. Taur, P. McFarland, K. Jenkins, D. Danner, M. Rodringuez, A. Megdanis, E. Petrillo, M. Polcari and T. H. Ning, 'A novel high-performance lateral bipolar on SOI,' IEDM Tech. Digest, pp. 663-666 (1991).
7. T. Shino, S. Yoshitmi, H., Nii, S. Kawanaka, K. Inoh, T. Yamada, T. Fuse, Y. Katsumata, M. Yoshimi, S. Watanabe, and J. Matsunaga, 'Analysis on high-frequency characteristics of SOI lateral BJTs with self-aligned external base for 2-GHz RF applications,' IEEE Trans. Electron Dev., 49(3), pp. 414-421 (2002).
8. H. Nii, T. Yamada, K. Inoh, T. Shino, S. Kawanaka, M. Yoshomi, Y. Katsumata, 'A novel lateral bipolar transistor with 67-Ghz f_{MAX} on thin-film SOI for RF analog applications,' IEEE Trans. Electron Dev., Vol. 47, pp. 1536-1541 (2000).
9. J. Cai, A. Ajmera, Q. Ouyang, P. Oldiges, M. Steigerwalt, K. Stein, K. Jenkins, G. Shahidi and T. Ning, 'Fully-depleted-collector polysilicon-emitter SiGe-base vertical bipolar transistor on SOI,', Symp. VLSI Tech. Digest, pp. 172-174 (2002).
10. Q. Ouyang, J. Cai, P. Oldiges and J. Johnson, 'A simulation study of thin SOI bipolar transistors with fully or partially depleted collector,' BCTM Tech. Digest, pp. 28-31 (2002).
11. J. Cai, M. Kumar, M. Steigerwalt, H. Ho, K. Schonenberg, K. Stein, H. Chen, K. Jenkins, Q. Ouyang, P. Oldiges, and T. Ning, 'Vertical SiGe-Base Bipolar Transistors on CMOS-Compatible SOI Substrate,' BCTM Tech. Digest, pp. 215-218 (2003).

12. L. Geppert, ‘A better bipolar transistor for wireless ICs,’ IEEE Spectrum, p. 20, December 2003.
13. Y. Taur and T. H. Ning, Fundamentals of Modern VLSI Devices, Ch. 8, Cambridge Univ. Press (1998).
14. P. Smeys, V. McGahay, I. Yang, J. Adkisson, K. Beyer, O. Bula, Z. Chen, B. Chu, J. Culp, S. Das, A. Eckert, L. Hadel, M. Hargrove, J. Herman, L. Lin, R. Mann, E. Meciejewski, S. Narasimha, P. O’Neil, S. Rauch, D. Ryan, J. Toomey, L. Tsou, P. Varekamp, R. Wachnik, T. Wagner, S. Wu, C. Yu, P. Agnello, J. Connolly, C. Davis, R. Ferguson, A. Sekiguchi, L. Su, R. Goldblatt and T.C. Chen, ‘A high-performance 0.13μm SOI CMOS technology with Cu interconnects and low-k BEOL dielectrics,’ Symp. VLSI Tech. Digest, pp.184-186 (2000).
15. G. Freeman, D. Ahlgren, D.R. Greenberg, R. Groves, F. Huang, G. Hugo, B. Jagnnathan, S.J. Jeng, J. Johnson, K. Schonenberg, K. Stein, R. Volant and S. Sabbanna, ‘A 0.18μm 90GHz fT SiGe HBT BiCMOS, ASIC-compatible, copper interconnect technology for RF and microwave applications,’ IEDM Tech. Digest, pp. 569-572 (1999).
16. G. Freeman, J. Rieh, B. Jagannathan, Z. Yang and F. Guarin, ‘Device scaling and application trends for over 200GHz SiGe HBTs,’ Int’l SiGe Technology and Device Meeting (ISTDM) Tech. Digest (2003).

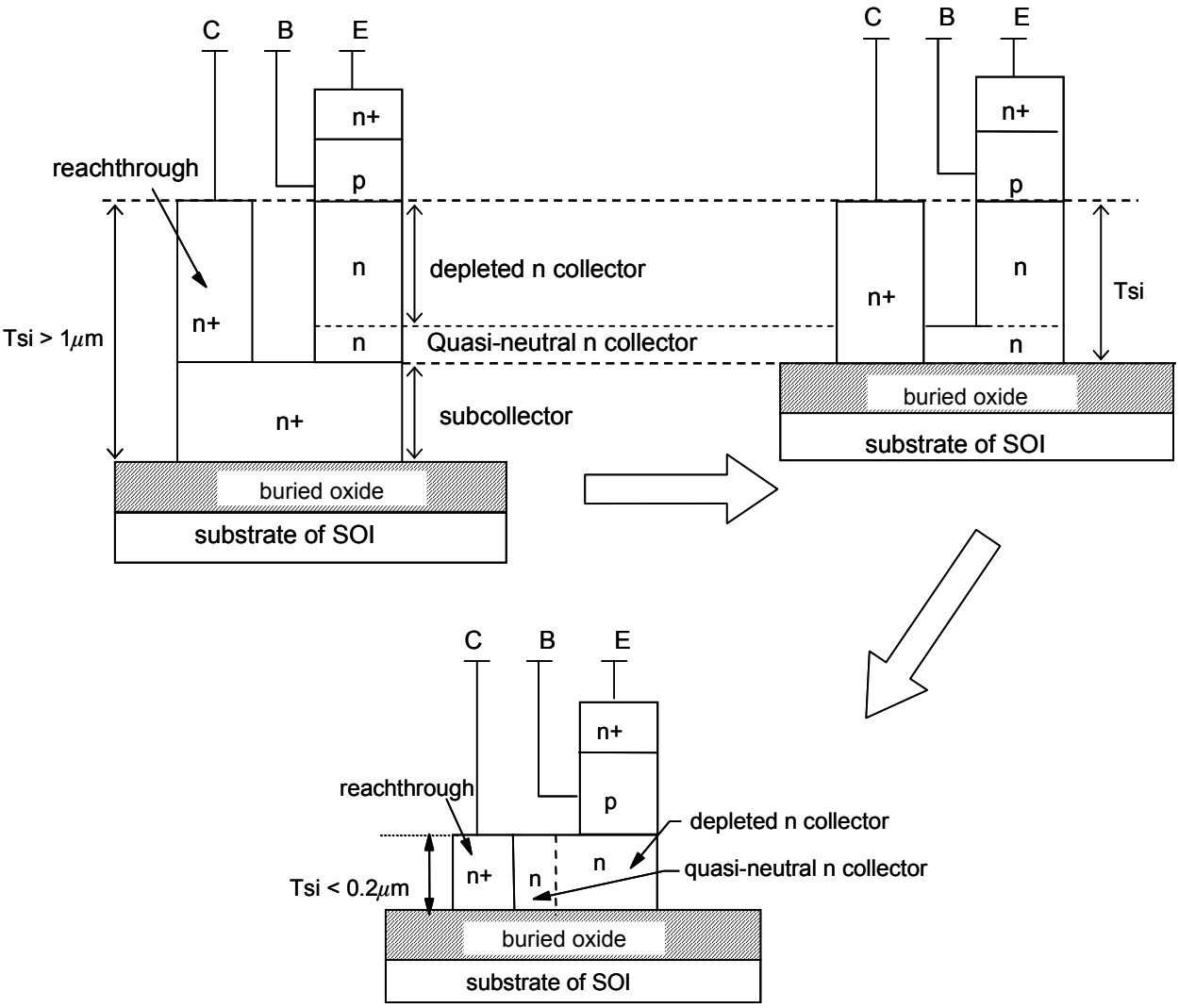


Figure 3.3.1 Schematics of npn bipolar transistors on SOI substrate, showing evolution of collector design that leads to the new transistor. The three cross-sections have the same base and emitter layers but different collector layers: (a) the traditional design with n+ subcollector underneath the n- collector, (b) without n+ subcollector, and (c) fully-depleted n- collector.

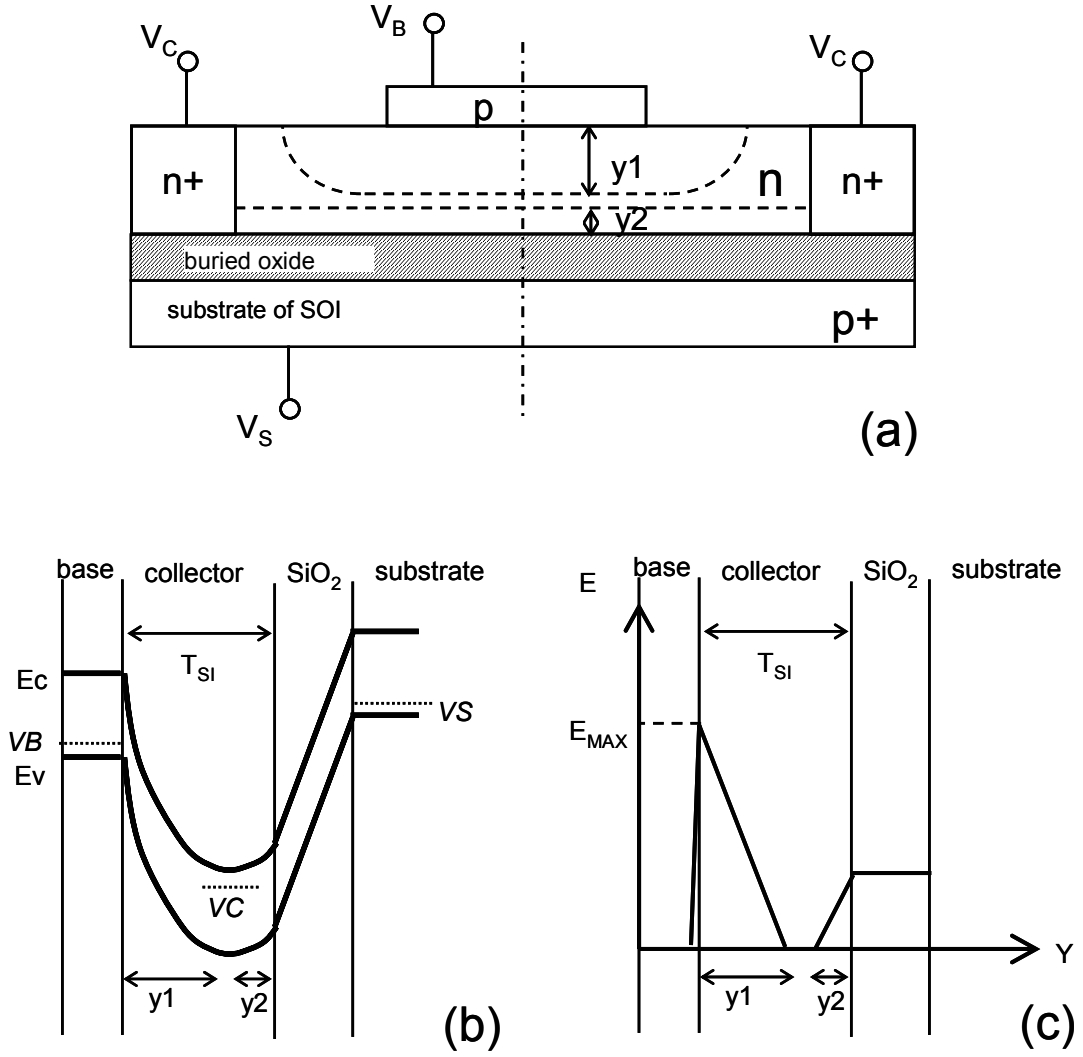


Figure 3.3.2 Analysis of collector potential distributions based on depletion approximation. (a) Schematic cross-section of part of an SOI bipolar transistor with symmetrically placed n+ reachthough regions; (b) energy band diagram along the central cut line; (c) electric field distribution along the same cut line.

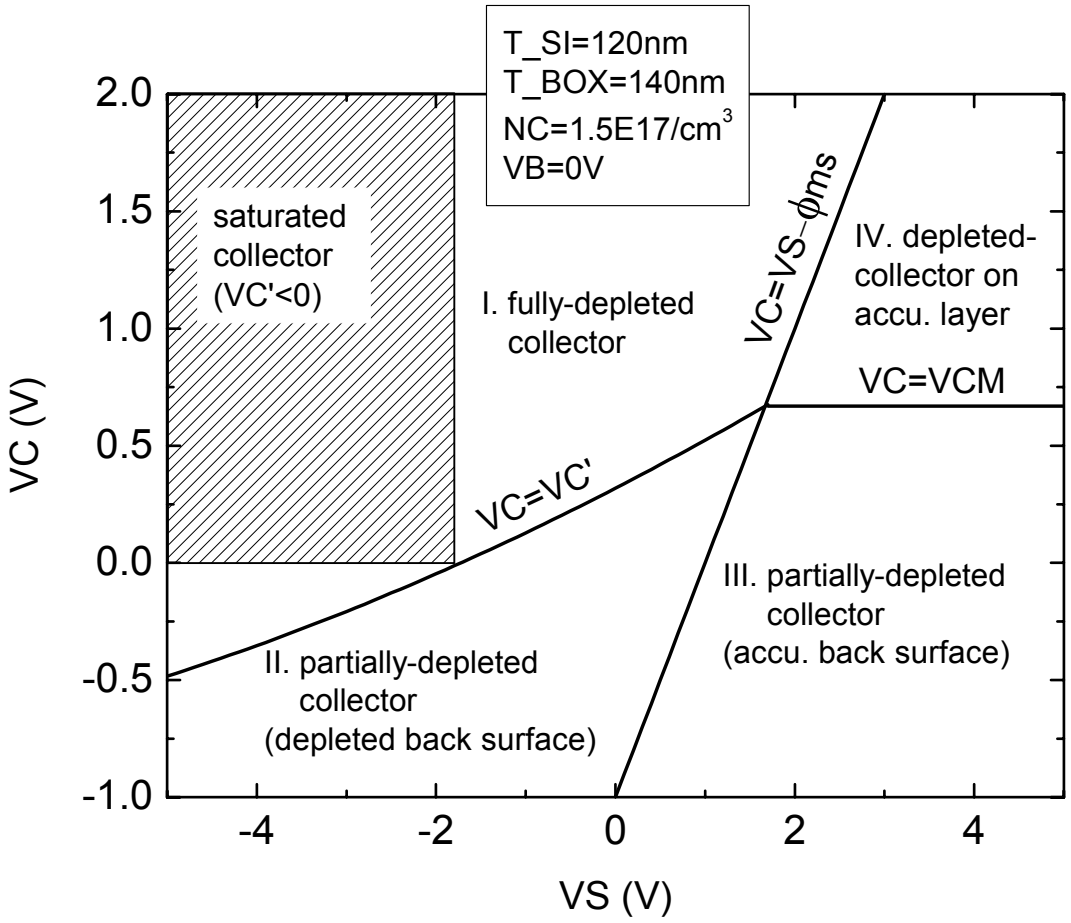


Figure 3.3.3 The collector characteristic of an SOI bipolar transistor is categorized into four types depending on the collector and SOI substrate bias conditions: 1) fully-depleted collector, 2) partially depleted collector with depleted back surface, 3) partially depleted collector with accumulated back surface, and 4) depleted collector with accumulated back interface, or accumulation subcollector.

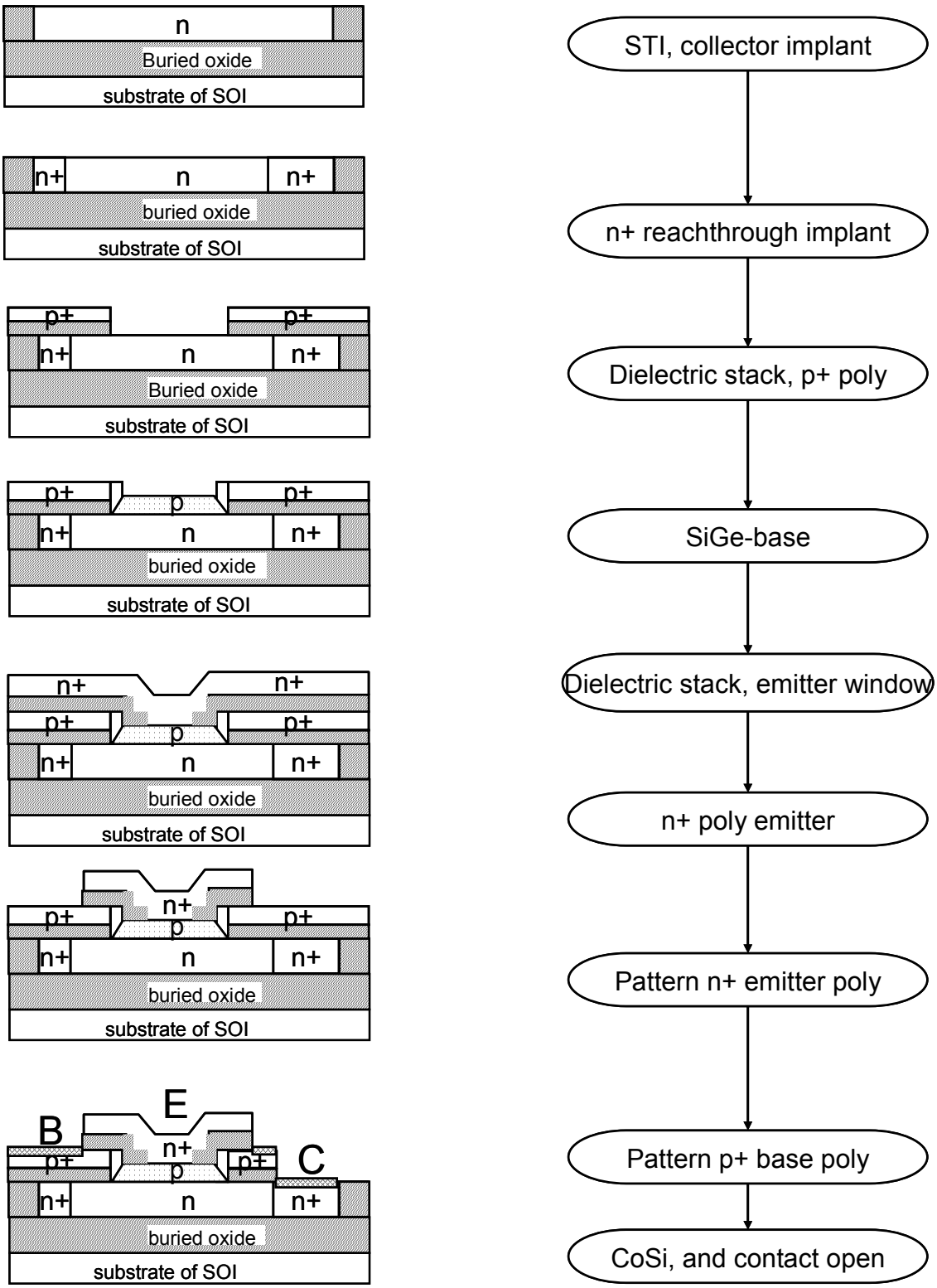


Figure 3.3.4 An example of process flow to make SiGe HBTs on CMOS-compatible SOI.

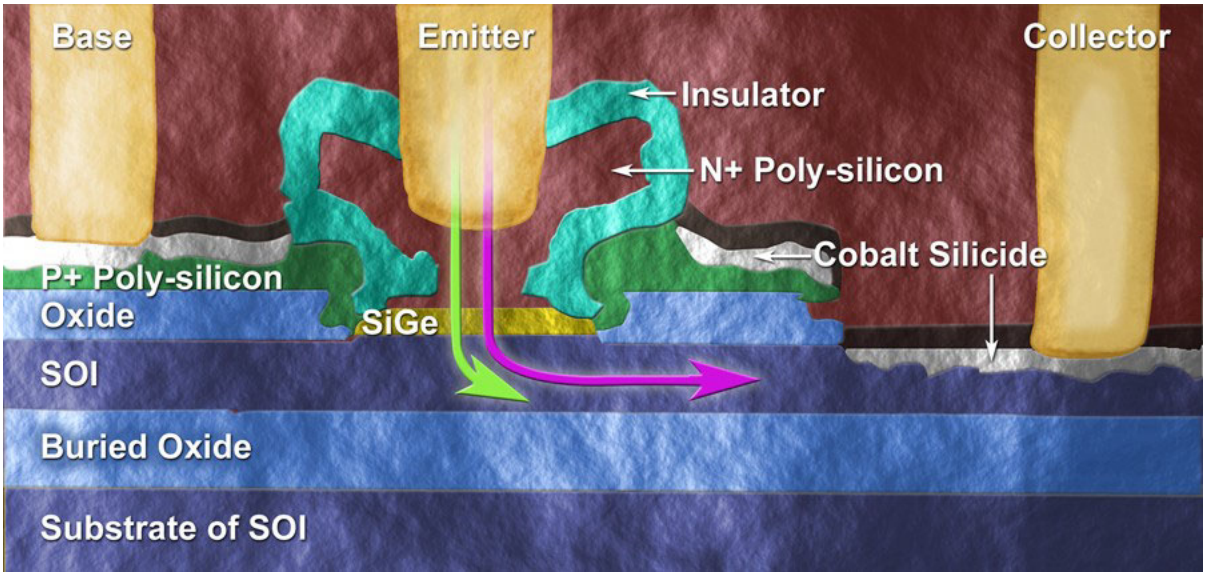
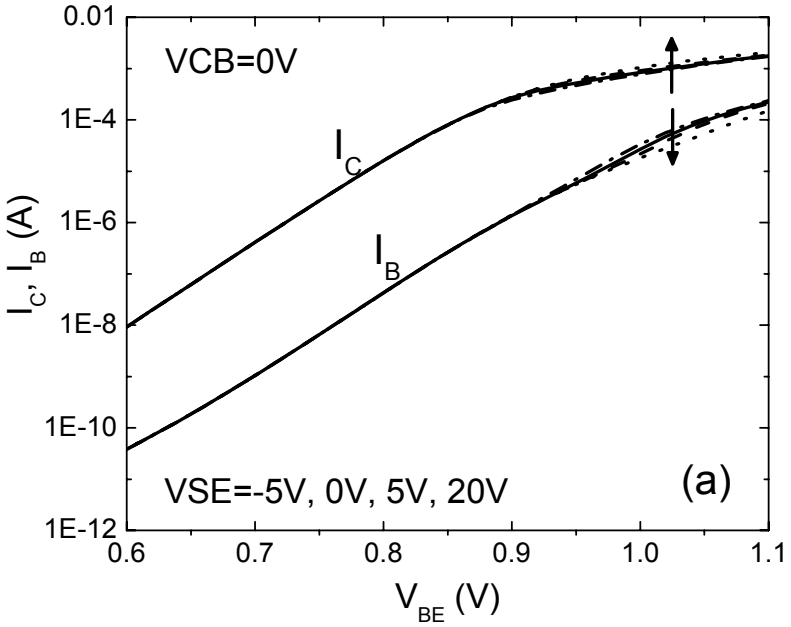


Figure 3.3.5 Cross-sectional SEM micrograph of a SiGe HBT on 0.12μm silicon film SOI.



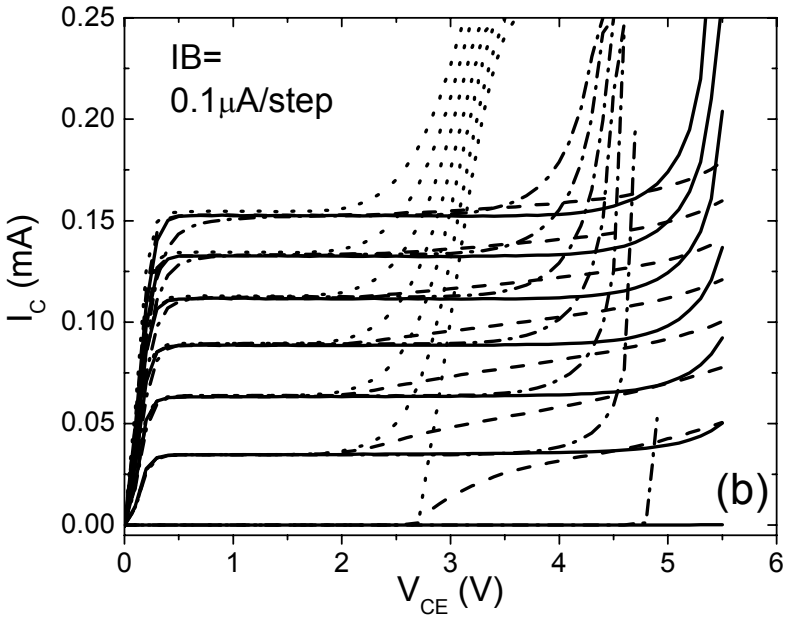


Figure 3.3.6 DC characteristics of a 0.16μm×0.8μm SOI SiGe HBT under four substrate bias (V_S-V_E) conditions: -5V (dash-dot), 0 (solid), 5V (dash) and 20V (dot). (a) Gummel plot, and (b) Output characteristics.

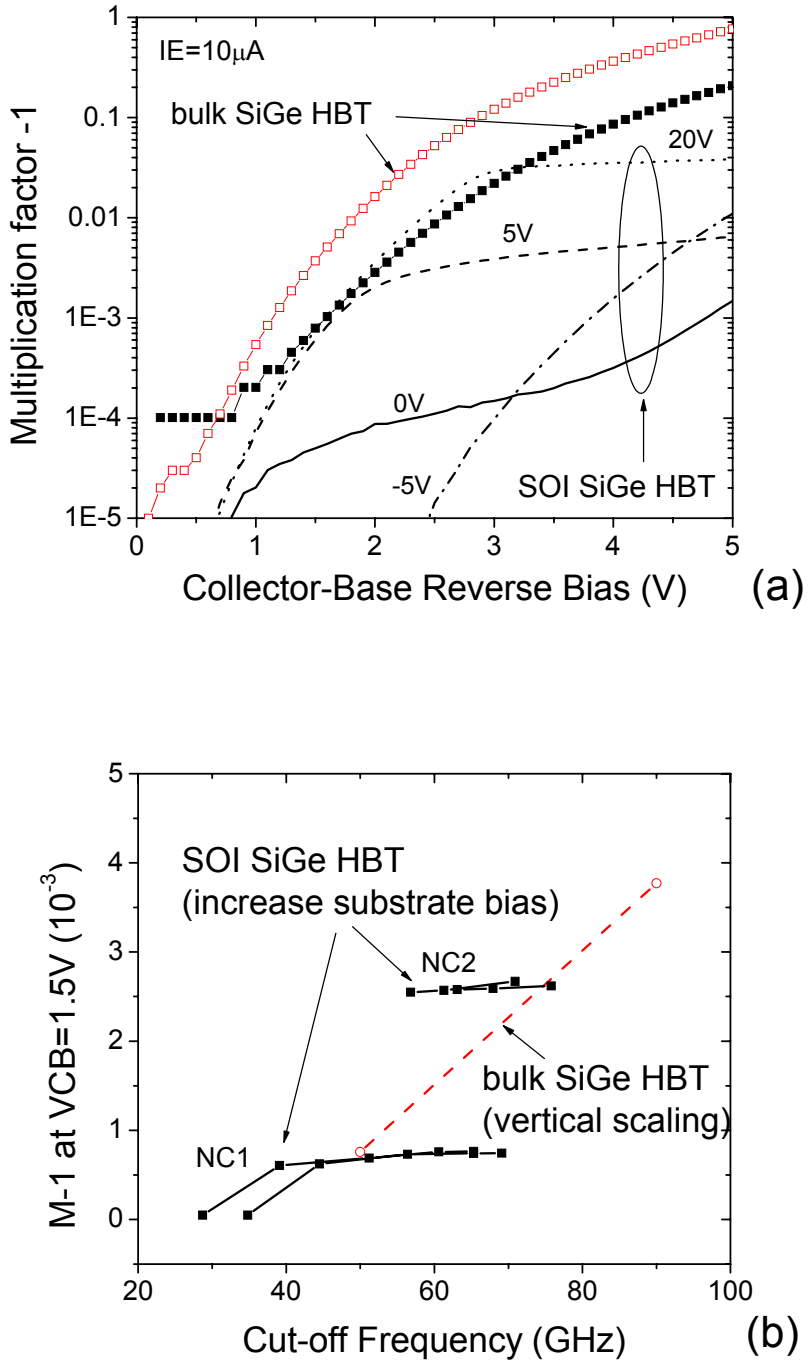


Figure 3.3.7 Measured avalanche multiplication factor (M-1) in base-collector junction of a SiGe HBT, with SOI substrate bias as a parameter. (a) 'M-1' as a function of reverse junction bias; (b) Correlation between 'M-1' and cut-off frequency, dashed line indicates trend from bulk SiGe HBT technologies.

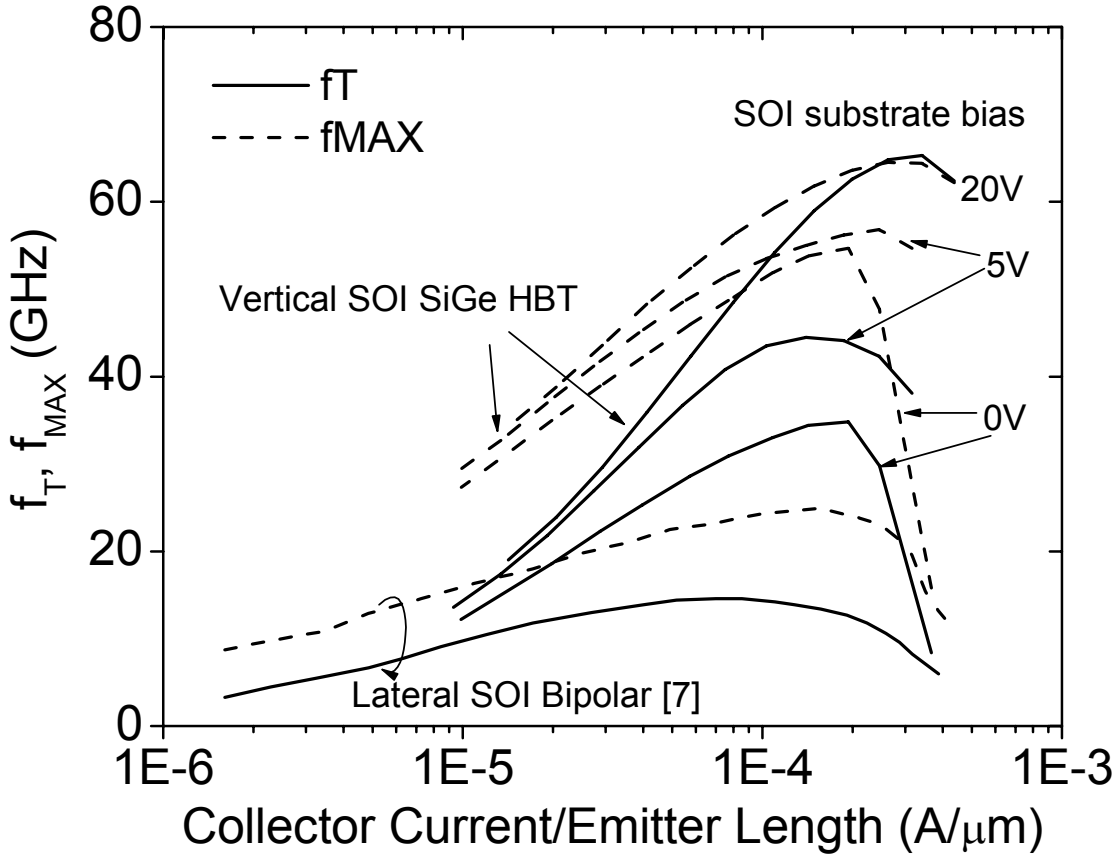
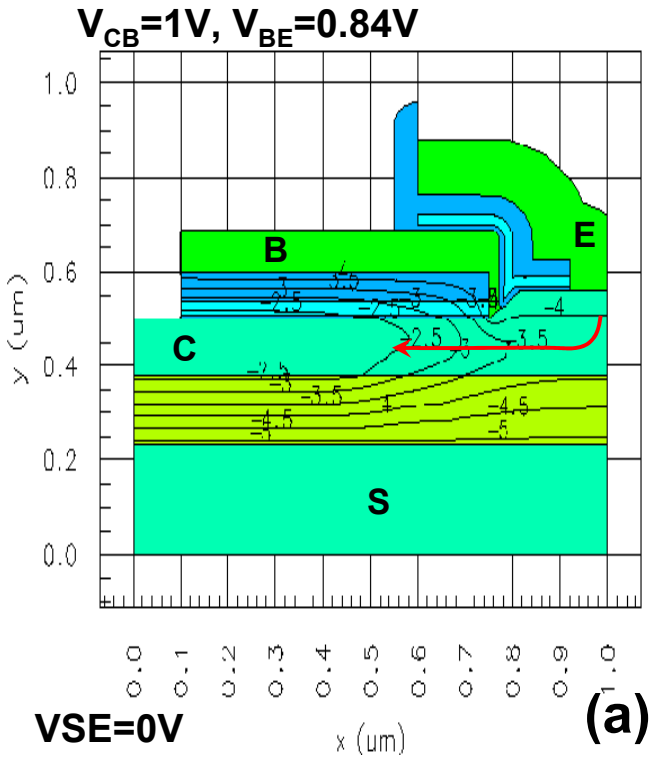


Figure 3.3.8 f_T and f_{MAX} characteristics of a 0.16μm×0.8μm SOI SiGe HBT, with SOI substrate bias as a parameter. The performance of recent lateral SOI bipolar transistor from [7] is plotted as a reference.



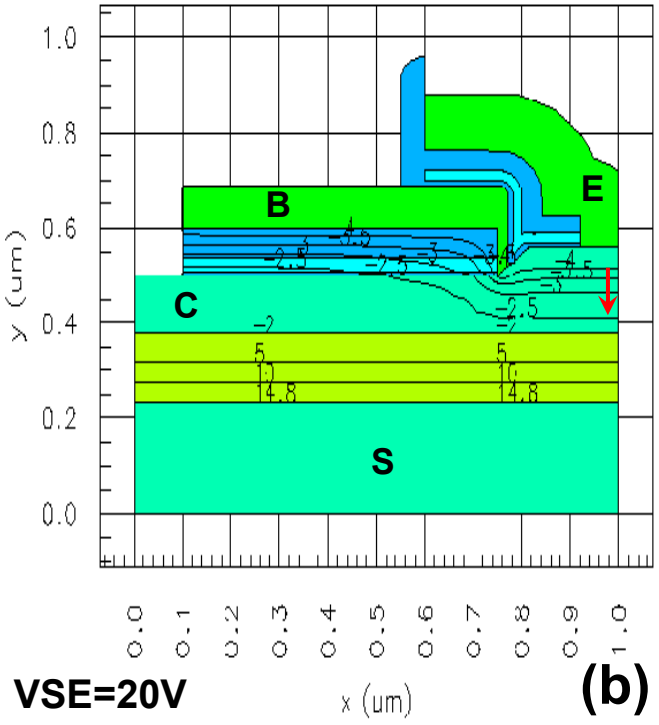


Figure 3.3.9 Simulated potential contours in (a) a fully-depleted collector device, and (b) the same device transformed to an accumulation subcollector device by a 20V substrate bias. The arrows represent direction of electron flow in the collector depletion region.

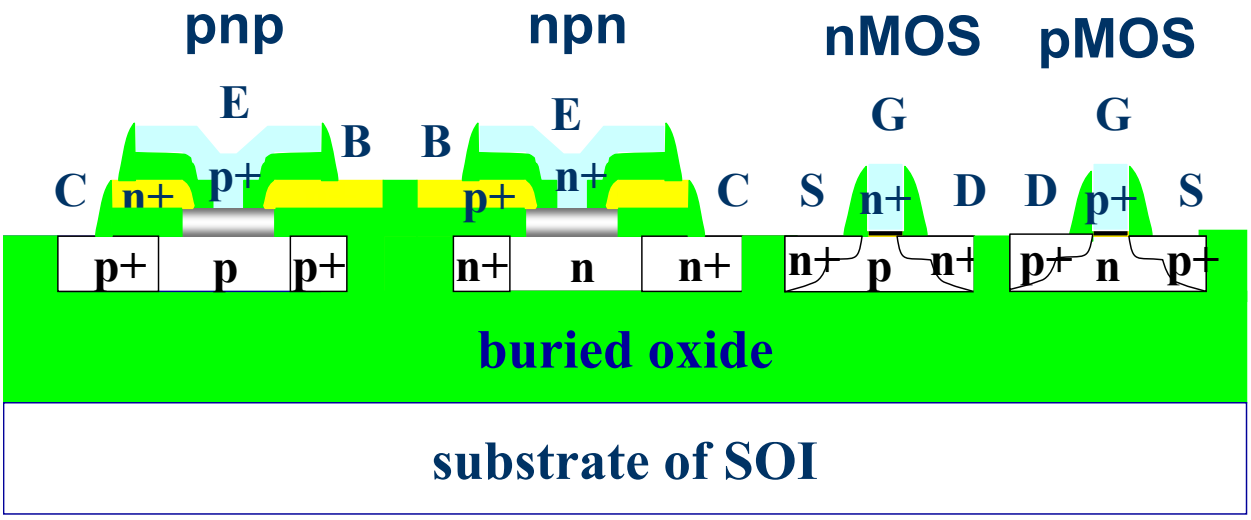


Figure 3.3.10 Illustration of an SOI complimentary bipolar and CMOS technology.

Parameters	Scaling factor		
	Fully-depleted-collector	Accu. sub-collector	Partially-depleted collector
W_E, L_B, L_C	α		
T_{SI}	β		
N_C	$1/\beta^2$		
I_C/L_E	α/β^2		
W_{dBC}, lateral	$\boldsymbol{\alpha}$	-	-
W_{dBC}, vertical	β	β	β
$R_C \cdot L_E$	-	α	$\alpha\beta$
C_{CB}/L_E	-	α/β	α/β
$R_C \cdot C_{CB}$	-	α^2/β	$\boldsymbol{\alpha^2}$

Table 1 Lithographical and SOI thickness scaling of vertical SOI bipolar transistors.