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120 Gb/s VCSEL-based Parallel Optical Links

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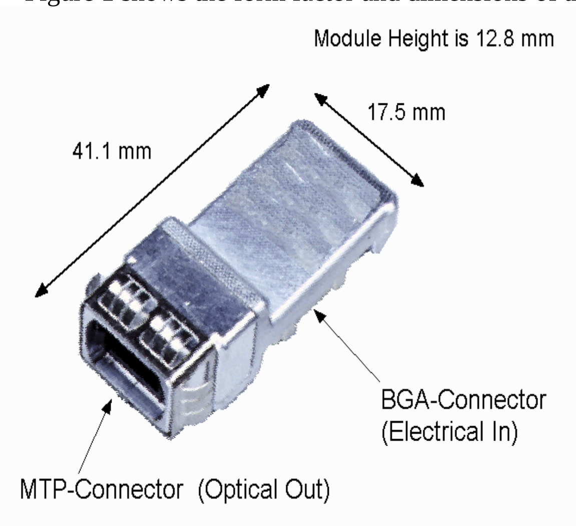
Abstract: A 120Gb/s parallel optical link using 850nm GaAs VCSELs is described and experimentally verified with all channels running simultaneous, with a custom-built 120Gb/s test station. Open eyes are obtained at 300m and low BER operation with margin is confirmed. Crosstalk from the opto-electronic devices is also described.

Introduction

The most recent release of the specifications of the Infiniband Architecture[1] describes a short distance (150m), 850nm, twelve channel, parallel optical link at 60GBaud for interconnecting processor and I/O nodes within a server. Work has already begun on the 120Gbaud implementation of this standard. This paper describes the performance of low cost optoelectronic and low power IC technology components which are suitable for such a standard. The transmitter consists of a CMOS laser diode driver array IC and an 850nm VCSEL array and is described below. An earlier version of this work using a SiGe laser diode driver array has been described in [2]. The receiver consists of a SiGe receiver array IC and a photodiode array. The receiver IC has been described extensively in [3][4]. Both the transmitter and receiver were packaged, separately, on a flexible printed circuit and assembled in a housing that conforms to the SNAP12 multisource agreement [5]. Figure 1 shows the form factor and dimensions of the optical module.



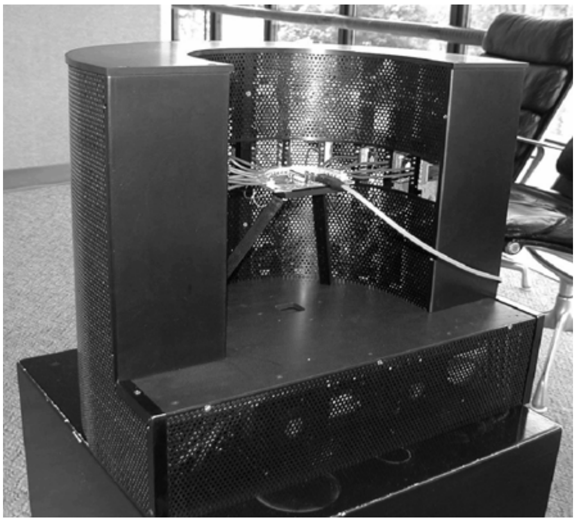


Figure 1 (Left) Picture of fully assembled optical module, without heatsink, for both transmitter and receiver.**(Right)** Picture of low cost 120Gb/s parallel testing station.

CMOS Driver IC

The 12-channel monolithic laser diode driver (LDD) array was fabricated in IBM's 120nm CMOS technology. A simplified schematic diagram of a single LDD channel is shown in Fig. 1. The signal path begins with a 100Ω floating termination and a limiting preamplifier, which consists of two Cherry-Hooper stages [6]. It is followed by a transconductance amplifier (TCA) output stage. The minimum input voltage is 100mV p-p with a common mode voltage of 0.9V. The inputs to each of the channels can be either DC or AC coupled. The signal path is fully differential to reduce crosstalk except for the output stage, which has a single-ended current output to accommodate a common-cathode laser array. However, the output of each channel has an adjacent ground pad that provides a low-inductance return path for the modulation current.
The high output impedance TCA is well suited for current modulation and can tolerate variations in laser's series resistance, up to 200Ω. In addition, output of the TCA is DC coupled, which is beneficial for array applications, as it eliminates the need for large coupling capacitors and separate laser bias circuitry. The TCA consists of a current switching differential pair M1–M2 and a PFET current source M4 as shown in Figure 2. Modulation is accomplished by diverting a part of M4 drain current, I_H, through M2, while the remaining current flows through the VCSEL Bias currents I_H and I_L can be adjusted off-chip to set the desired modulation levels. The maximum output current of 10mA is possible.

The LDD consumes about 85mW per channel including VCSEL. It uses dual supplies to save power. Most of the design operates from a 1.8V supply, while VCSEL bias is provided from a 3.3V supply. Supply independent biasing and on-chip decoupling are provided to improve channel isolation. The driver operates in an open-loop configuration with no optical feedback. The LDD die size is 1.3mm × 3.50mm, and the channels are on a 250μm pitch to facilitate direct and uniform wire bonding to the VCSEL array.

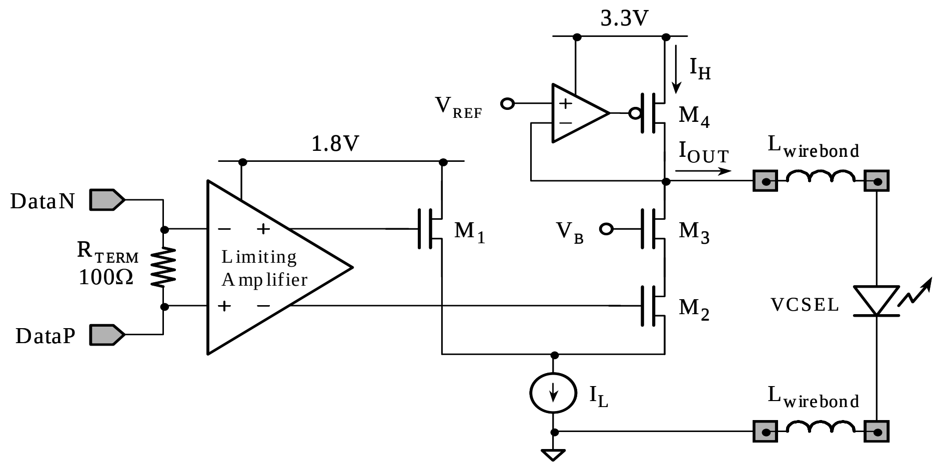


Figure 2 Simplified schematic of a single LDD channel

Low Cost Testing

One of the challenges to achieving low cost optical interconnects is to reduce the cost associated with testing. Commercially available parallel channel test equipment is currently too expensive. In this work, a low cost multi-channel tester was realized by arranging twelve 10 Gigabit Ethernet Standard[7] physical layer ICs into a tower which also holds the power supplies and cooling fans, and provides a platform for the device under test. The physical layer ICs contains built-in PRBS test patterns and error detectors. Additionally, the test station ICs have a two-wire interface which enables control from a remote PC for single channel or simultaneous multi-channel (crosstalk) testing. Figure 1, right side, shows a picture of this low cost testing station.

Link Results

Parallel inks with lengths ranging from 8m to 500m have been characterized. In all cases, the link has a minimum of four parallel connectors. Links with lengths under 50m have used standard 50/125 multimode bandwidth fiber. Links above 50m have used mostly high bandwidth (OM3) 50/125 fiber with short jumpers of standard fiber at each end. The edge rate of the received optical signal decreases with link length from 39ps at 8m, to 44ps at 300m, and 51ps at 500m. At 500m the eye opening is not sufficient for error free operation of all 12 channels. At 300m and below, short term error free operation can be observed with all 12 channels running simultaneously. Several long term BER measurements were conducted and BER ~1E-14 or lower was measured.

Optoelectronic Device Crosstalk

In the previous work [2], the transmitter was built using a common cathode VCSEL and transmitter amplitude crosstalk penalty was 2dB for the worst channel when all 12 channels were operating simultaneously but asynchronously, at 10 Gb/s. In this section, one of the sources for transmitter crosstalk, the VCSEL array, is investigated in detail. Seven different VCSELs arrays from four different manufacturers were used in this study. Five of the arrays were a common cathode configuration with different top surface metallurgy. The other two arrays were an isolated design on semi-insulating substrates (common nothing). All VCSELs are oxide confined structures suitable for 10 Gb/s operation. The inter-chip crosstalk was measured using a network analyzer and microwave probes on two channels of a bare VCSEL array with each channel biased to a level appropriate for 10 Gb/s operation. The crosstalk is defined as S21 between the two measured channels. Note, this is a four port measurement with two electrical ports and two optical ports. It was found that the electrical to neighboring optical coupling was the same as the electrical to electrical coupling after the laser's inherent response was accounted for. The crosstalk within the VCSEL array is thus electrical and not optical. The S21 results shown here are taken between the electrical ports. The worst case crosstalk occurs for nearest neighbor channels and drops down for further apart neighbors. All five common cathode designs were found to have similar crosstalk characteristics that fell within a 10dB band over frequency. Figure 3 upper right shows that the crosstalk for the common cathode designs has a capacitive characteristic which is very low at low frequencies and increases monotonically with frequency. For the frequency range covered by 3 Gb/s operation, the nearest neighbor crosstalk level is around -40dB. At this low level, a BER crosstalk penalty would not be observed for the 3 Gb/s data rate. For the 10 Gb/s frequency range, the nearest neighbor crosstalk level ranges from -17dB to

-25dB depending on design. For next nearest neighbors, the crosstalk level drops at a rate that varies from 0.6dB/ch to 1.4dB/ch depending on design. This decrease versus channel spacing is fairly small so that the accumulated crosstalk from all 11 neighboring channels can be rather significant. For example, see Figure 3 upper left, the common cathode design with the highest crosstalk coupling at 10 GHz created a BER floor for 12 channel operation whereas the design with the lowest crosstalk coupling resulted in a 2dB penalty for 12 channel operation at 10 Gb/s (see Figure 3 lower left). Figure 4 depicts the effect of crosstalk in the time domain for the design that resulted in a BER floor. Depending on tradeoffs in the link design, a 2dB transmitter penalty could be accommodated. For example, this penalty is smaller than the insertion loss of a coarse wavelength division multiplexer proposed for multi-channel VCSEL links [8].The common cathode designs appear well suited for 12 channel operation at data rates below 10 Gb/s or for fewer than 12 channel operation at 10 Gb/s. The isolated VCSEL designs had nearest neighbor coupling that was less than -40dB up to 20 GHz. The characteristic of this crosstalk looks capacitive with a large series resistance. For one design, the next nearest neighbors dropped down by 1dB/channel and for the other it was 5dB/ch. In both cases, the crosstalk level is sufficiently low that it should not present a significant penalty even up to 20 Gb/s/ch for 12 channels. Figure 3 lower right shows that the measured 12 channel BER penalty with one of the isolated designs was less than 0.3dB. The measurement repeatability is also about 0.3dB.

Two different types of isolated photodiodes were also characterized. The crosstalk coupling between nearest neighbors was at the -40dB level out to 20GHz. Receivers built with each type of photodiode design did not exhibit a difference in crosstalk penalty.

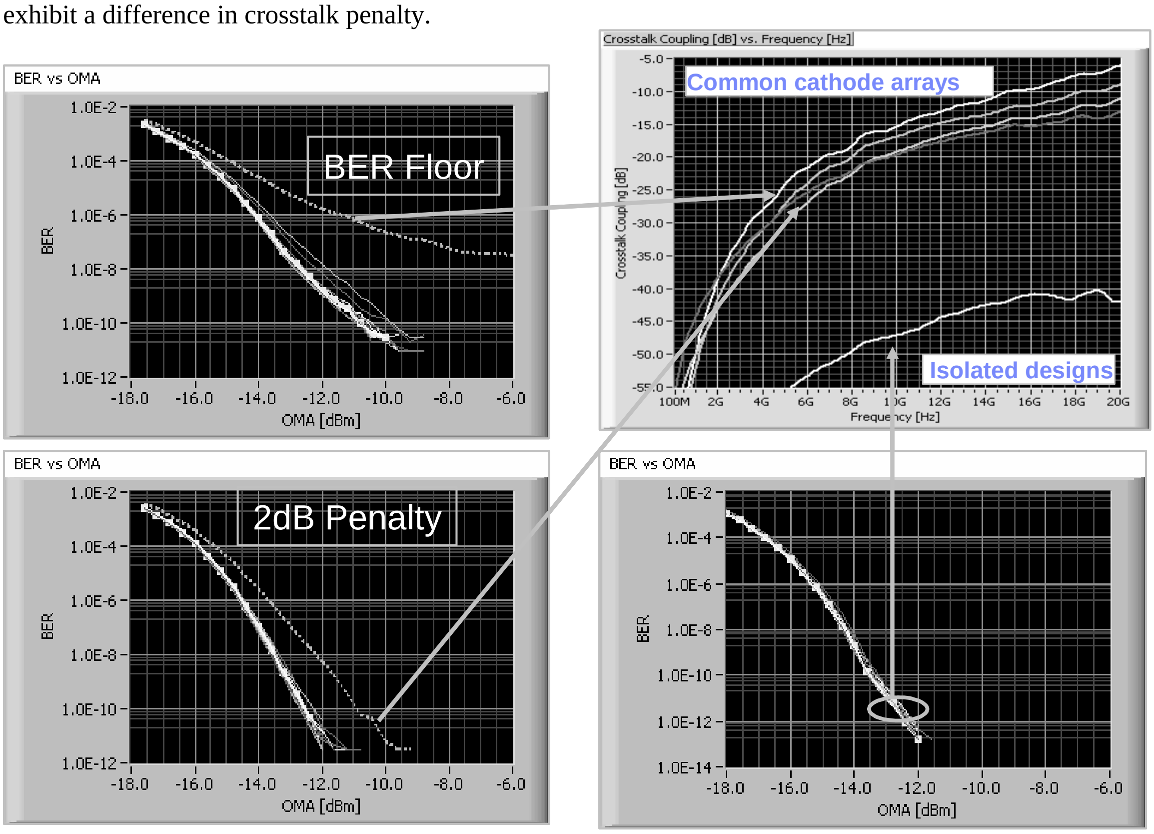


Figure 3 Nearest Neighbor Crosstalk coupling (S21) vs frequency for 7 different VCSEL designs and the corresponding 12 channel BER curves for 3 of these designs, exhibiting a BER floor (common cathode design with highest coupling) , a small transmitter penalty (common cathode design with lower coupling), and essentially no penalty (isolated design) for 10Gb/s operation.

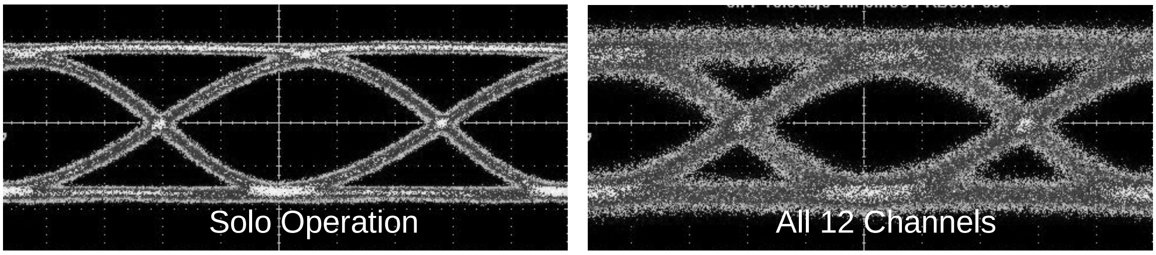


Figure 4 Time domain characterization of crosstalk for a common cathode design. The left eye shows single channel operation at 10Gb/s. The eye on the right is the same channel when all other 11 channels are operating.

Package Crosstalk
Figure 5 shows the measured electrical crosstalk (near end) of the flex circuit and it's BGA connector mounted on a test board. The crosstalk is below 40dB out to 20 GHz. The highest level of crosstalk comes from nearest neighbor transmission lines on the flex. The second highest contributions comes from nearest neighbor channels in the BGA pin field (these are not necessarily nearest neighbors on the flex due to layout and routing considerations) and the lowest contribution comes from diagonal neighbors in the BGA pin field. Overall, the package crosstalk contribution is very small.

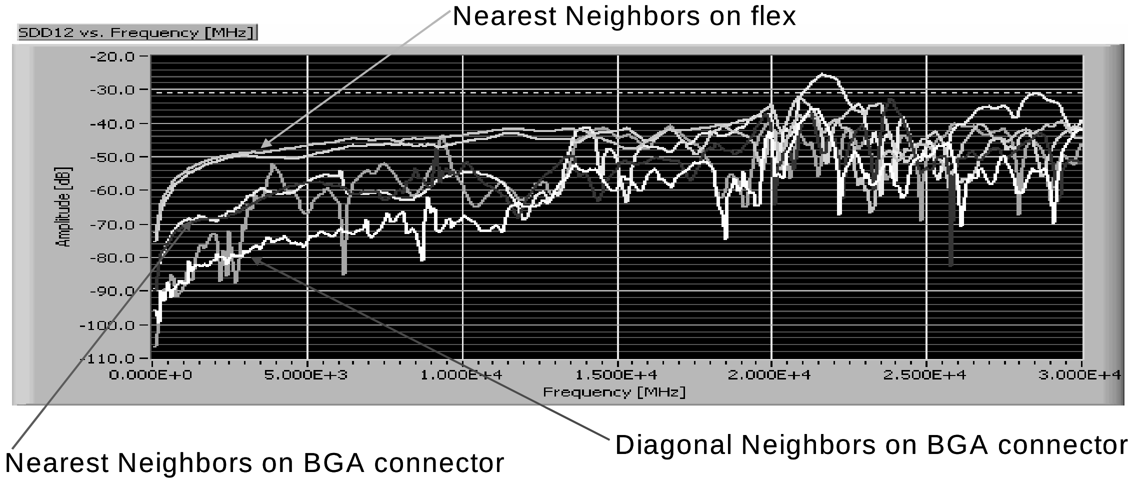


Figure 5 Electrical Crosstalk on flex circuit including BGA connector

Summary
A complete link running at 120Gb/s, driven by a novel low cost testing station, has been realized using a CMOS laser diode driver array IC and 850nm VCSEL array as the transmitter and a SiGe receiver array and photodiode array as the receiver. The complete link consumes 2.2W and operates with a BER below 1E-12 with all channels running simultaneously. This technology has the potential to replace distance challenged copper cables within parallel server systems.

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