RC23474 (W0412-066) December 21, 2004
Physics

IBM Research Report

Potential Imaging of Si/HfO_2/poly-Si Gate Stacks: Evidence for an Oxide Dipole

R. Ludeke, V. Narayanan, E. P. Gusev, E. Cartier, S. J. Chey
IBM Research Division
Thomas J. Watson Research Center
P.O. Box 218
Yorktown Heights, NY 10598

Research Division
Almaden - Austin - Beijing - Haifa - India - T. J. Watson - Tokyo - Zurich

LIMITED DISTRIBUTION NOTICE: This report has been submitted for publication outside of IBM and will probably be copyrighted if accepted for publication. It has been issued as a Research Report for early dissemination of its contents. In view of the transfer of copyright to the outside publisher, its distribution outside of IBM prior to publication should be limited to peer communications and specific requests. After outside publication, requests should be filled only by reprints or legally obtained copies of the article (e.g., payment of royalties). Copies may be requested from IBM T. J. Watson Research Center , P. O. Box 218, Yorktown Heights, NY 10598 USA (email: reports@us.ibm.com). Some reports are available on the internet at http://domino.watson.ibm.com/library/CyberDig.nsf/home.

Potential imaging of Si/HfO_2/poly-Si gate stacks: evidence for an oxide dipole

R. Ludeke, V. Narayanan, E. P. Gusev, E. Cartier and S. J. Chey

IBM T. J. Watson Research Center

P.O. Box 218 Yorktown Heights NY 10598

Abstract. *Surface potential profiles of the junction area of a cleaved n-Si/HfO_2/p^+-poly-Si gate stack reveal a dipole potential in the oxide, hole trapping at the HfO_2/poly-Si interface, with the Fermi level ~0.4 eV below the Si conduction band edge and enhanced and inhomogeneous hole depletion in the p^+-poly-Si. The dipole accounts for band bending reduction in the n-Si and is consistent with flat band voltage shifts reported for similar gate stacks.*

The limited range of the Fermi level movement in the band gap of Si/HfO_2/poly-Si CMOS devices is by now well established and publicized.[1-9] The problem is characterized by an undesirable shift in the flat band voltage from ideality, which translates to an unacceptable threshold voltage shift in the performance of MOSFET devices. This problem is particularly severe for p-channel devices and may render the HfO_2/poly-Si system unsuitable as a gate stack combination in future generations of MOSFETS. The origin of the shifts have been attributed to diverse effects, including dopant penetration from the poly-Si into the HfO_2,[1,2] acceptor and donor-like interface states,[6] the formation of an oxide interface dipole,[8] and silicide formation accompanied by Fermi level pinning near the top of the Si band gap.[4] The pinning mechanism was attributed to metal induced gap states (MIGS),[4,5] a notion that was recently disputed on the basis that the charge neutrality level of Si, which determines the position of the MIGS, is located near the bottom of the Si band gap.[10] However, based on the evolution of the interband pinning position for low HfO_2 coverages,[4,5,9] as well as from the observed weakening of the pinning following the addition of capping layers,[7] a consensus is developing that a Hf-Si reaction at the HfO_2/poly

interface is responsible for the trap states in the upper band gap region of Si that cause the pinning. This notion is supported by recent theoretical studies of diverse Hf-O/Si(100) configurations, which show that the presence of Hf-Si bonds introduce states with metallic-like behavior throughout the Si band gap. The partial filling of these states results in a configuration-independent Fermi level position in the upper part of the Si band gap.[10] In this letter we offer new insights into the issues at hand, specifically the direct observation of a dipole potential across the HfO_2 layer and pinning of the Fermi level in the upper part of the band gap at the p-poly Si/HfO_2 interface, findings that are consistent with reported electrical characteristics, including threshold voltage shifts. The findings are based on high resolution profiles of the potential variations in the Si/HfO_2/poly-Si gate region obtained by AFM imaging techniques in combination with a novel cleaving method of the gate stack structure. The physical origin of the dipole remains unknown but its presence contributes to several detrimental characteristics, such as poly-depletion and an inhomogeneous band bending in the poly-Si that is largely independent of its grain structure.

Two novel experimental aspects are prerequisite for these observations: a relatively flat and defect-free slice through the gate stack and a high resolution, surface potential profiling method in a non-contaminating environment. The former was achieved by cleaving in ultra-high vacuum (UHV) a pre-notched sample containing the planar gate stack. The gate oxide was composed of a 3 nm HfO_2 layer grown on lightly doped n^--Si(100) wafer with an intervening 1nm silicon oxynitride layer. The oxide was subsequently overgrown with a poly-Si film, which was then Boron-implanted and activated to produce the desired p^+-poly-Si layer. The surfaces of the wafer were coated with a SiN layer and a lithography-mediated narrow window was opened on the backside, through which a V-shaped notch was chemically etched to within 100 μm of the stack structure. Half of the notched sample was clamped on a holder and inserted into the UHV atomic force microscope (AFM). The other half cleaved off in-situ just prior to the potential measurements. The AFM is operated in the electrostatic force mode, with contact potential difference (CPD) images of the stack structure obtained directly by suitable feedback-control.[11] CPD and

topographic images were acquired simultaneously, which readily allows correlation studies between physical and electronic image features. Surface potential profiles were generated from cuts through the CPD images of the cross-sectioned stack structure.

Figs. 1a and b respectively show the topography and surface potential images of a large area of the interface region. The topography is characterized by an atomically smooth region in the upper part of the image that corresponds to the cleaved n-Si(111) surface. Below it lies the wider but rougher poly-Si layer characterized by regions of fracture bands that end at the poly-Si/SiN interface. The somewhat brighter (topographically) higher region at the bottom is the fractured SiN film. No evidence of the HfO_2 layer between the Si and poly-Si is apparent in the topography on this scale. In contrast the potential image shown in Fig. 1b reveals more contrast among the three regions, with the brighter band corresponding to the region bounded by the Si-HfO_2 interfaces. Fig. 1c and 1d show images of the stack region on a more detailed scale. The topography, Fig. 1c, now clearly shows a somewhat elevated (brighter) strip crossing the image that incorporates the HfO_2 layer.[12] Below it lies the granular region of the poly-Si, which progressively exhibits a rougher surface away from the interface. This roughness is a consequence of the increased directional choice the cleavage front has as it progresses through the polycrystalline Si away from the interface. A clearer view of the interface region is obtained from the potential image of the identical area, shown in Fig. 1d. The image consists, in coarse terms, of an upper region of high potential (bright) that corresponds to the cleaved n^--Si and extends to the oxide interface, and a region of lower potential (darker) that corresponds entirely of the p^+-poly-Si. The image contrast between the two regions is ~0.86 V, which is in good agreement with the expected band offsets between the n^- and p^+-doped regions. The transition between the two potential regions is the result of band bending across the gate stack.

We digress momentarily to illustrate and discuss the relationship between band bending and surface potential changes. Fig. 2a depicts the band diagram, the vacuum level E_{VAC} and the surface potential or CPD change, V_{CPD}, across an ideal n-Si/oxide/p-Si gate stack, i.e. without interface states and dipoles. The potential in the n-Si drops as the oxide interface is approached; equivalently the bands bend

up. The potential varies only modestly in the oxide region because of its large dielectric constant. The potential drops further in the poly-Si, again because of band bending in this region. In the absence of the oxide (not shown) the band diagram, E_{VAC} and V_{CPD} would further simplify and assume the smooth and monotonic changes corresponding to those of a p-n junction. In the presence of a dipole spanning the entire thickness of the gate oxide, specifically one with the field vector pointing to the Si substrate, the band diagram assumes the shape shown in Fig. 2b, with the corresponding E_{VAC} and V_{CPD} shown just above it. The characteristic signature of such a dipole in the CPD signal is the triangular feature in the region corresponding to the oxide, with the potential peaking at the oxide/poly-Si interface.

Verification of the existence and location of a dipole can be obtained from potential and topography profiles, that is, voltage and height variations along cuts that cross the interface region along identical paths in both images. The position of such matching cuts are indicated by dashed lines in Figs. 1c and. 1d. The resulting profiles are shown in Fig. 3, curve (a) representing the topography and (b) the surface potential. The qualitative agreement between the latter and the schematic V_{CPD} profile for the stack structure with a dipole, Fig. 2b, is remarkable. The experimental profile peaks at the HfO_2/poly-Si interface, as verified by detailed analysis of many larger scale images, which also indicate that the dipole field is mostly located within the boundary of the HfO_2 layer. The sense of the dipole requires positive charge to be located at the HfO_2/poly-Si and electrons near the n-Si/HfO_2 interface. The presence of the passivating oxynitride interlayer at the n-Si/HfO_2 interface would suggest that the electrons are not trapped there, but rather are delocalized conduction band electrons. Thus the positive charge must result from holes trapped at the HfO_2/p^+-poly Si interface. The compensating electron charge at the Si interface causes a reduction of the band bending in the Si. This concept is illustrated in Fig. 4, which depicts a superposition of the conduction band (CB) offsets for a gate stack with and without the dipole. The illustrated lowering of the flat band voltage V_{FB} in the presence of the dipole is consistent with experimental observation for Boron-doped poly-Si/HfO_2 gate stacks. The absence of a dipole corresponds to the more ideal Si/SiO_2 interface.

The net change in the poly-Si potential (i.e. the band bending) from its value in the "bulk" and at the HfO_2 interface averages 0.7 eV, which indicates that the Fermi level at the poly-Si interface is located 0.4 eV below the conduction band edge. This value in good agreement with prior experimental[9] and theoretical[10] values of 0.35 and 0.3 eV, respectively. The trapping of holes leads to an additional depletion of free holes in the p^+-poly-Si region adjacent to the oxide, thus exasperating an already critical problem. To make matters worse, the potential in the poly-Si was observed to fluctuate in directions both parallel and normal to the interface, as can be readily appreciated by the mottled appearance of the poly-Si region in the image of Fig. 1d. Furthermore, these fluctuations due not correlate very well with the poly-Si grain structure (Fig. 1c). A profile of the fluctuations for a cut 8 nm from the interface is shown in Fig. 3, curve (c). The origin of such lateral variations, which are reflected as well in the band structure, are stipulated to be due to fluctuations in the density of trapped holes at the interface, as the intensity of the fluctuations further increases towards the interface (not shown).

In summary, we have demonstrated a novel imaging application of the potential and topographic changes occurring across an integrated gate stack structure of device quality components. The potential profiles suggest Fermi level pinning at the HfO_2/p^+-poly-Si that leads to dipole formation in the oxide. A cause and effect relationship between these observations and the well-known flat band shifts is established.

1. L. Kang, K. Onishi, Y. Jeon, B. H. Lee, C. Kang, W.-J. Qi, R. Nieh, S. Gopalan, R. Choi, and J. C.Lee, IEDM Tech. Dig., 2000 , p. 38.
2. S. Pidin, Y. Morisaki, Y. Sugita, T. Aoyama, K. Irino, T. Nakamura, and T. Sugii, Symp. VLSI Tech. Dig., 2002, p. 28.
3. E. P. Gusev, D. A. Buchanan, E. Cartier, A. Kumar, D. DiMaria, S. Guha, A.Callegari, S. Zafar, P. C. Jamison, D. A. Neumayer, M. Copel, M. A. Gribelyuk, H. Okorn-Schmidt, C. D'Emic, P. Kozlowski, K. Chan, N. Bojarczuk, L.-A. Ragnarsson, P. Ronsheim, K. Rim, R. J. Fleming, A. Mocuta, and A. Ajmera, IEDM Tech. Dig. 2001, p. 20.1.1.

4. C. Hobbs, L. Fonseca, V. Dhandapani, S. Samavedam, B. Taylor, J. Grant, L. Dip, D. Triyoso, R. Hegde, D. Gilmer, R. Garcia, D. Roan, L. Lovejoy, R. Rai, L. Hebert, H. Tseng, B. White and P. Tobin, Symp. VLSI Tech. Dig., 2003, p. 9.
5. S. B. Samavedam, L. B. La, P. J. Tobin, B. White, C. Hobbs, L. R. C. Fonseca, A. A. Demkov, J. Schaeffer, E. Luckowski, A. Martinez, M. Raymond, D. Triyoso, D. Roan, V. Dhandapani, R. Garcia, S. G. H. Anderson, K. Moore, H. H. Tseng, C. Capasso, O, Adetutu, D. C. Gilmer, W. J. Taylor, R. Hegde and J. Grant, IEDM Tech. Dig. 2003, p. 13.1.1.
6. C. W. Yang, Y. K. Fang, C. H. Chen, S. F. Chen, C. Y. Lin, C. S. Lin, M. F. Wang, Y. M. Lin, T. H. Hou, C. H. Chen, L. G. Yao, S. C. Chen and M. S. Liang, Appl. Phys. Lett. **83**, 308 (2003).
7. E. Cartier, V. Narayanan, E. P. Gusev, P. Jamison, B. Linder, M. Steen, K. K. Chan, M. Frank, N. Bojarczuk, M. Copel, S. A. Cohen, A. Callegari, S. Zafar, M. Gribelyuk, C. Cabral, R. A. Carruthers, C. D'Emic, J. Newbury, D. Lacey, S. Guha and R. Jammy, Symp. VLSI Tech. Dig., 2004, p. 44.
8. L. Pantisano, et al. Symp. VLSI Tech. Dig., 2004, p. 122.
9. C. Hobbs, L. Fonseca, A. Knizhnik, V. Dhandapani, S. Samavedam, W. Taylor, J. Grant, L. Dip, D. Triyoso, R. Hegde, D. Gilmer, R. Garcia, D. Roan, L. Lovejoy, R. Rai, E. Hebert, H. Tseng, S. Anderson, B. White and P. Tobin, IEEE Trans. Electron Devices **51**, 971 (2004); ibid. **51**, 978 (2004).
10. X. Kiong, P. W. Peacock and J. Robertson, Appl. Phys. Lett. (accepted).
11. R. Ludeke1, P. Lysaght, E. Cartier,E. Gusev, M. Chudzik, B. Foran and G. Bersuker, J. Vac. Sci. Technol. **B 22**, 2113 (2004).
12. The ~5 nm projected width of the gate oxide is only discernable at even larger scales (not shown).

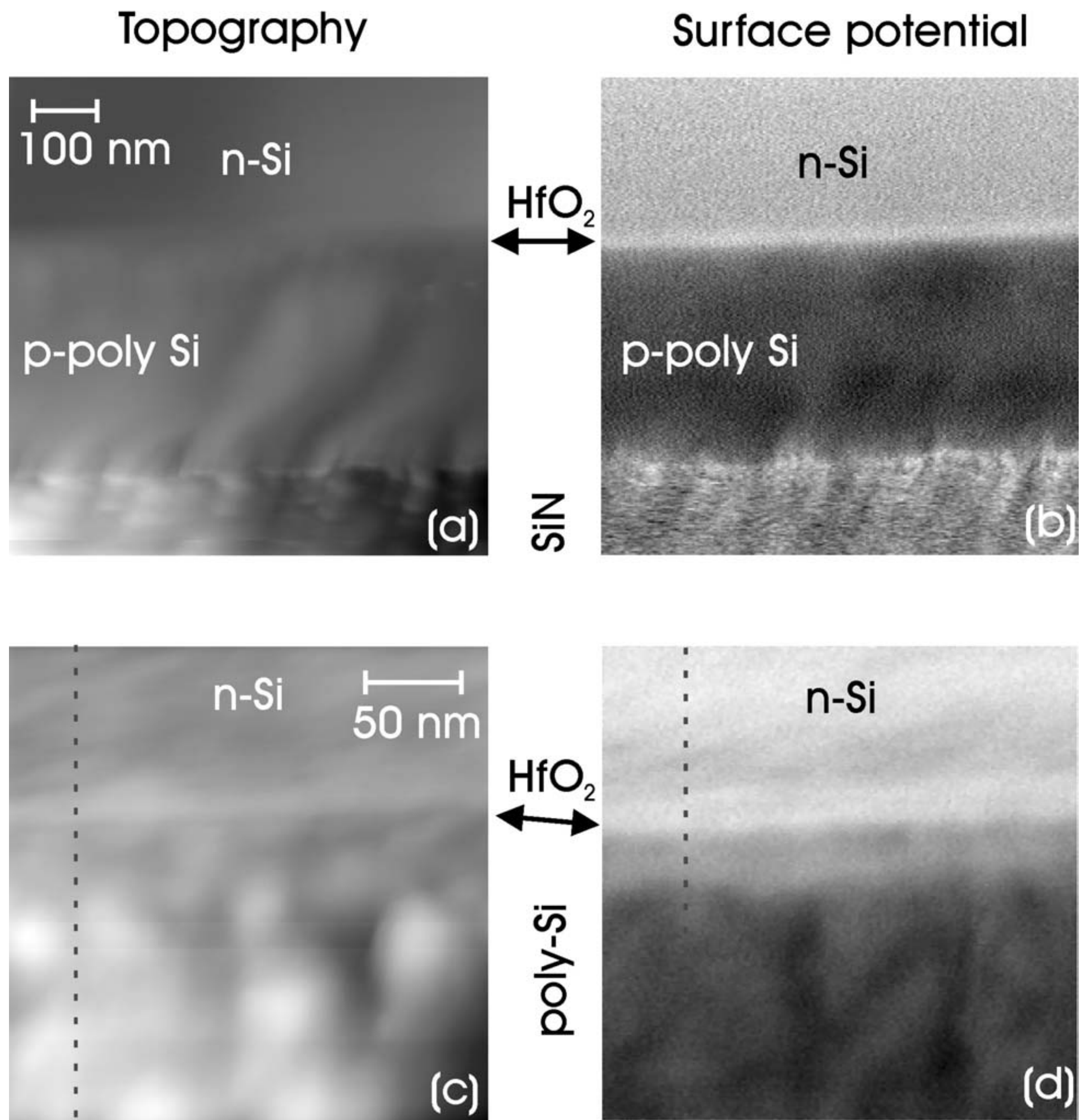

Fig. 1. Topography (a and c) and corresponding surface potential or CPD images in cross section of a HfO_2 gate stack. The lower pair is at an enhanced magnification. Contrast scales: (a) and (b) 51 nm and 0.8 V, respectively; (c) and (d), 14 nm and 0.86 V.

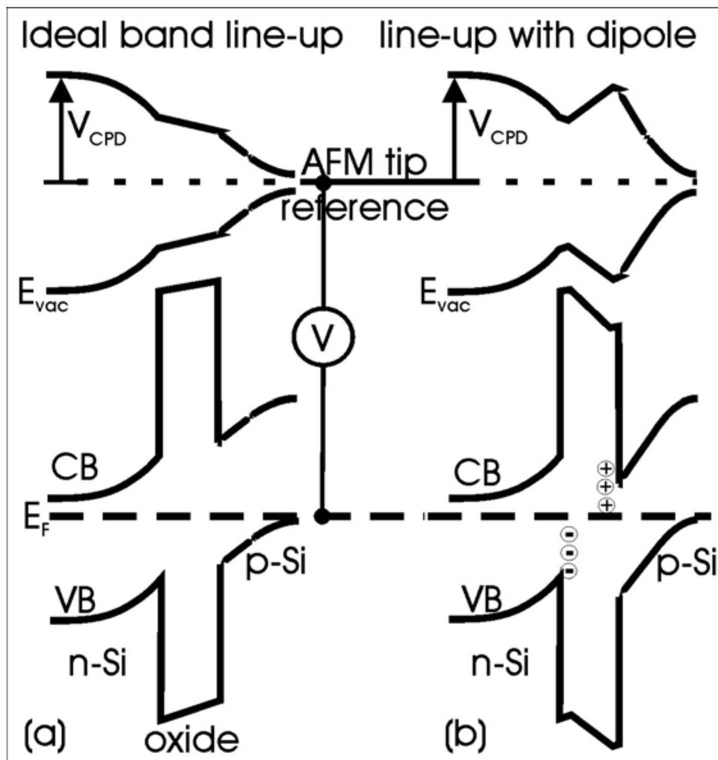

Fig. 2 Band diagrams and associated vacuum level and contact potential for an idealized n-Si/oxide/p-Si gate stack (left) and one with a dipole across the oxide (right).

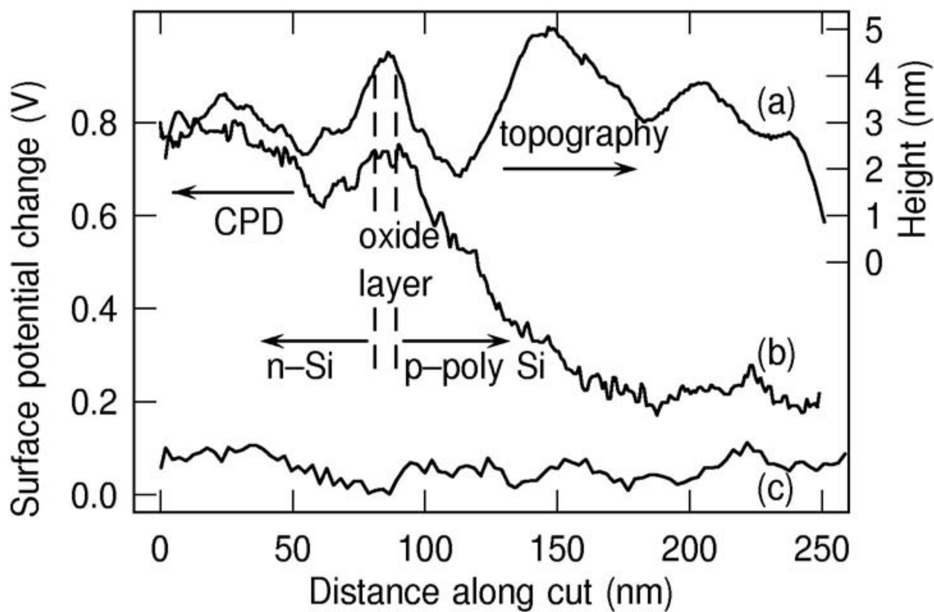

Fig. 3 Topography (a) and potential profile (b) across gate stack region marked by the dashed lines at the bottom of Fig. 1. Curve (c) is a potential profile along the interface at a distance of 8 nm into the poly-Si of Fig. 1d.

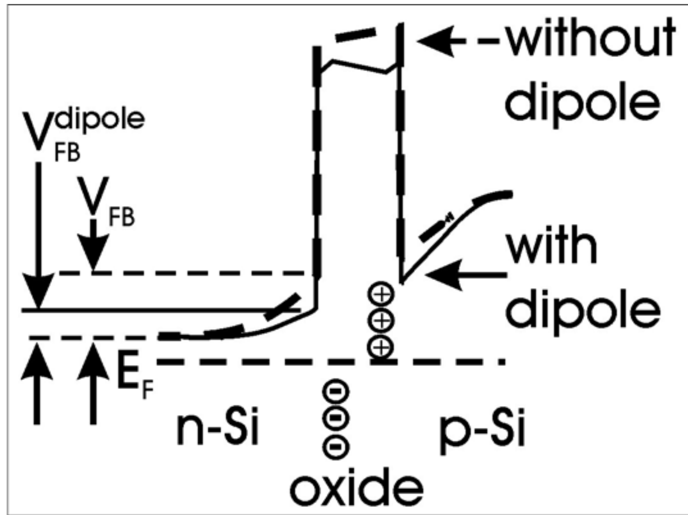

Fig. 4 Band diagram depicting the dipole-mediated decrease of the flat band voltage in n-Si.