RC23500 (W0501-093) January 21, 2005
Electrical Engineering

IBM Research Report

Predicting Interconnect Requirements in Ultra-Large-Scale Integrated Control Logic Circuitry

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Predicting interconnect requirements in ultra-large-scale integrated control logic circuitry

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ABSTRACT

Information about interconnect requirements is needed for the successful design of today's complex, ultra-large-scale integrated (*ULSI*) chip circuitry. Estimates of interconnect requirements, including average wire-length and wire-length distributions in chip designs, are obtained by evaluating existing on-chip wire-length distribution models. The overall objective of this paper is to present estimates and measurements of interconnect requirements in *ULSI* control logic circuitry. One goal of this paper is to present a comprehensive assessment of existing models and to quantify the agreement observed (1) between estimates and measurements of average wire-length in individual designs in real chips, and (2) between wire-length distributions provided by the models and wire-length distributions obtained from measurements. Another goal of this paper is to present an assessment of the interconnect requirements for all of the control logic in a chip. For this study, actual interconnect data is measured in ASIC-like control logic designs in the six functional units of the 1.3*GHz POWER4*. This paper compares interconnect measurements with estimates for control logic in individual designs, in functional units, and in the entire *POWER4* core. The results presented in this paper show that the estimates are typically lower than the actual wire-length measurements. The results also show that the estimates of the total wire-length for all of the control logic in the *POWER4* agree to within 31% of the total measured wire-length.

1. INTRODUCTION AND MOTIVATION

Information about interconnect requirements is needed for the successful design of today's complex, ultra-large-scale integrated (*ULSI*) chip circuitry. The circuitry and the associated wiring are required to satisfy a set of electrical and physical constraints that includes: a constrained amount of real estate area on a silicon die, a fixed number of back-end-of-the-line (*BEOL*) metal layers available for interconnect wiring, small cycle times, large switching edge rates, manufacturability requirements, and power dissipation limits. The wiring solution for a successful chip design satisfies these constraints and is completed and manufactured within a specified product schedule.

On-chip wire-length distribution models provide estimates of the interconnect requirements in *ULSI* chip circuitry. The input parameters to these models are referred to as either *external Rent parameters* or *topological Rent parameters*, depending on the choice of model [1]-[9]. For a complete assessment of the models, actual design data from today's chips is needed.

Prior assessments of the Donath (1979) model [10] and Donath (1981) model [11] compared assessments with a few examples of available design data; however, the models did not provide assessments with the required accuracy. An assessment of the Davis (1998) model [12], [13] fit the wire-length requirements to the wire-length distribution data. In 2000, two models [14] were presented by Christie for placement in the plane. Recent work [15] presented an assessment of the Davis (1998) model for all of the control logic designs in one functional unit of the *POWER4* microprocessor and also presented an assessment of the Donath and Christie models for one of these designs.

The *POWER4* is an example of a multi-core processor. Specifically, the *POWER4* contains two microprocessor cores, an on-chip *L2* cache, circuitry associated with the *L3* cache directory, and chip-to-chip interconnection circuitry [16]. The two cores have equivalent interconnect requirements. One of the cores is located in the upper left-hand corner of the chip, and the other core (a mirror-image of the first core) is located in the upper right-hand corner, as shown in [16, Fig.1]. Multi-core processors such as the *POWER4* provide examples of chips that are designed with a large amount of functional integration. Functional integration is one factor that contributes to the wiring complexity of today's *ULSI* chips. For the case of the *POWER4*, functional integration contributes to the wiring complexity because interconnect is required to connect circuitry within each core as well as to connect circuitry among the cores and other on-chip circuitry.

The overall objective of this paper is to present estimates and measurements of interconnect requirements in *ULSI* control logic circuitry. To achieve this objective, this paper has two primary goals. The first goal is to present a complete assessment of existing on-chip wire-length distribution models and to quantify the extent to which the wire-length estimates and wire-length distributions provided by the models agree with the measurements for individual designs in real chips. The second goal is to present an assessment of the quantity of interconnect required to connect all of the control logic in a microprocessor.

This paper presents a complete assessment of the Donath model [10], [11] and Christie model [14] for all of the control logic designs in one functional unit of the *POWER4*. For this study, estimates of the average wire-length and wire-length distribution are obtained by evaluating the models as functions of Rent's parameters. These estimates are then compared with actual interconnect requirements and with estimates provided by the Davis model. This paper also provides estimates and actual measurements of the wire-length requirements in the six functional units of the *POWER4*, and the estimates are compared with the measurements. Finally, estimates are obtained for the total wire-length requirement for all of the control logic in the entire *POWER4* core. These estimates are also compared with the actual total measured wire-length.

Categories and Subject Descriptors
B.7.2 [Hardware, Integrated Circuits, Design Aids]: Layout, Placement, Routing

General Terms Design, Interconnect, Model, Rent
Keywords
Wire-length distribution models, Rent, control logic, interconnect

This paper is organized as follows. Section 2 reviews the inputs to the wire-length distribution models of Donath [10], [11], Davis [12], [13], and Christie [14]. Section 3 presents estimates of interconnect requirements for designs in one functional unit of the *POWER4* and describes trends that are observed in the data. Section 4 presents estimates of the interconnect requirements in the other five functional units of the *POWER4*, where these estimates are based on the results in Section 3. Section 4 also compares these estimates with measurements. Section 5 presents estimates of the total interconnect requirement in all of the control logic in the *POWER4* and compares these estimates with measurements. Section 6 presents a discussion of the results, and Section 7 presents the conclusion.

2. BACKGROUND

This section reviews the choice of input parameters for the existing on-chip wire-length distribution models. The notation for the parameters in this paper is the same as the notation in [12], [15].

The *external Rent parameters* are inputs for the Davis model and are described with notation {*k*, *p*} [1], [2], [11], [12]. The method to extract the *external Rent parameters* from chip design data is discussed in [1], [2], [12], [15]. The *topological Rent parameters* are inputs for the Donath and Christie models and are described with notation {*k**, *p**} [7], [8], [14]. Complete details to extract values for {*k**, *p**} are in [7], [15]-[19] and are now reviewed briefly. The first step is to convert the design data from Cadence database format to an ascii hypergraph file. Next, a *k*-way partition of each design is computed with multi-level recursive bisection with a software program named *hMetis* developed at the University of Minnesota [17], [18]; *k* is given by the values in the list {2, 4, 8, … , }, with the largest value of *k* chosen such that no partition contains zero gates. For each partition, the software program *hMetis* is executed with the default configurations (*shMetis*) [17]-[20] on a computer workstation. The inputs to *shMetis* are: (1) the hypergraph file; (2) the appropriate value of *k*; and (3) a minimum (1%) allowed imbalance between the partitions during recursive bisection [7], [8], [15], [21].

The results of the recursive bisectioning for each design are plotted without averaging [9] on a log-log plot of the *Number of Terminals T* as a function of the *Number of Gates G*. Values of {*k**, *p**} are obtained for each design from least-squares recursive linear fits to the data in Region I to the expression,

$$Log(T) = Log(k^*) + p^* \times Log(G). \quad (1)$$

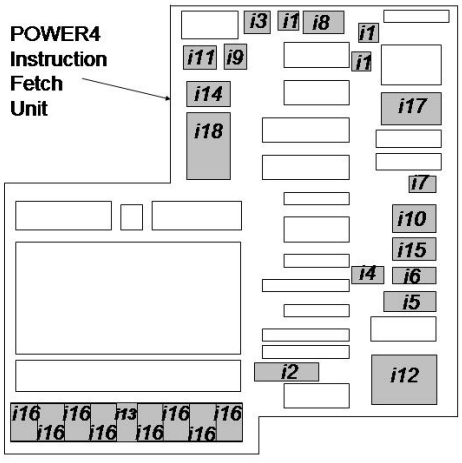

Figure 1. Locations of the 18 control logic designs in the POWER4 IFU floorplan. Designs are labelled in order of increasing N_{gates}.

3. TRENDS IN ESTIMATES PROVIDED BY THE INTERCONNECT MODELS

This section describes trends in estimates provided by the models for all of the control logic designs in one functional unit (the *Instruction Fetch Unit*, or *IFU*) in the *POWER4* chip. The locations of the 18 *IFU* designs are shown in Fig. 1; the designs are labeled in order of increasing N_{gates}. The control logic designs are also referred to as random logic macros [16].

For this study, the program *shMetis* [17], [18] is executed on an IBM *RS6000* workstation with 2GB memory running AIX4.3. Figure 2 shows the results of the recursive bisections for designs *i1-i8* and *i10-i18.* Results for design *i9* are in [15]. Regions I and II are shown in each plot. The values of {*k**, *p**} are extracted from these plots with Eqn. 1; the values are listed in Table 1. The table shows that *k** takes on values in the range {1.3, 2.9}, and that the values tend to range from 2.3 to 2.7. The table also shows that p^* is less than unity and that $0.58 < p^* < 0.87$.

Figure 3 shows the distributions provided by the Donath, Davis, and Christie models for designs *i1-i8* and *i10-i18*. In this figure, the normalized probability density is shown on the left ordinate, and the cumulative probability distribution is shown on the right ordinate of each plot. The measured normalized probability density is shown as solid circles, and the measured cumulative probability density is shown as hollow squares. In the figures, the distributions provided by the Christie models are shown as red dashed lines and green dashed lines; distributions provided by the Davis model are shown as black solid lines; distributions provided by the Donath (1979) model are shown with blue solid lines; and distributions provided by the Donath (1981) model are shown as black dashed lines. The plots in Fig. 3 show that the distributions provided by the models tend to underestimate the measured distributions, particularly for the cases in which the wire-length takes on large values. These results are consistent with the distribution obtained for design *i9* [15].

The plots in Fig. 3 also show that the curvature of the distributions provided by the Davis model shows the greatest qualitative agreement with the curvature of the measured distribution. The dotted lines in the figure show that the ranges tend to enclose the actual wire-length distribution. Note that as N_{gates} increases (from design *i1* to *i18*) the amount by which the distributions underestimate the measured distributions actually increases for the cases in which the wire-length takes on large values. Values for N_{gates} in individual designs are given in [15].

Table 2 shows the estimates of average wire-length provided by the Donath and Christie models for each design. This table compares these estimates with other estimates provided by the Davis model and with actual measurements. The error (in %) compared with measurements for estimates provided by the Donath model is given by the expression, $E(\overline{R}_{p^*}) = (\overline{R}_{p^*} - L_a) \times 100 / L_a$; the error for the estimate provided by the Davis model is given by the expression, $E(L_{avg}(p)) = (L_{avg}(p) - L_a) \times 100 / L_a$; and the error for the estimates provided by the Christie model is given by the expression, $E(L_{avg}(p^*)) = (L_{avg}(p^*) - L_a) \times 100 / L_a$, where L_a represents the measured average wire-length.

The results in Table 2 show that the estimates provided by the Donath model show closer agreement (to within 33%) with the measured average wire-length compared with the agreement shown for estimates provided by the other models. The results also show that the estimates of average wire-length provided by the Donath model show the closest agreement with the measured average wire-length for the largest designs (that is, for designs *i13-i18*) that have the largest values of $L_a > 7.0$ *gatepitches per signal*, and for the smallest designs (that is, for designs i1-i4). Table 2 also shows that estimates of the average wire-length provided by the Davis and Christie models show the closest

agreement with the measured average wire-lengths for designs with sizes in the middle of the range considered here (that is, for designs *i8*, *i11* and *i10*, respectively).

Table 3 shows estimates of the total wire-length in the 18 *IFU* designs. These estimates are obtained by multiplying the average wire-length estimate and the number of nets in each design. A comparison of the total wire-length estimates and the measured total wire-length is also shown in Table 3. The error (in %) compared with the measurements for the estimate provided by the Donath model is given by the expression, $E(\overline{R}_{p^*,tot}) = (\overline{R}_{p^*,tot} - L_T) \times 100 / L_T$; the error for the estimate provided by the Donath model is given by the expression, $E(L_{tot}(p)) = (L_{tot}(p) - L_T) \times 100 / L_T$; and the error for the estimate provided by the Christie model is given by the expression, $E(L_{tot}(p^*)) = (L_{tot}(p^*) - L_T) \times 100 / L_T$, where L_T represents the total wire-length measurement. Note that the errors shown in this table are the same as those in Table 2, because each average wire-length is multiplied by the number of nets. The results in the table show that the values of the total wire-length measurement range from 305.5 *gatepitches* (*i1*) to 43,767.3 *gatepitches* (*i18*).

Table 1. Topological Rent parameter pairs {k*, p*}.

IFU Design	k* [range]	p* [range]
i1	1.95 [1.66, 2.29]	0.71 +- 0.12
i2	2.69 [2.56, 2.83]	0.65 +- 0.03
i3	2.39 [2.16, 2.65]	0.59 +- 0.06
i4	2.44 [2.21, 2.69]	0.75 +- 0.06
i5	2.75 [2.62, 2.88]	0.59 +- 0.03
i6	2.52 [2.36, 2.68]	0.61 +- 0.03
i7	2.71 [2.59, 2.84]	0.65 +- 0.02
i8	2.90 [2.76, 3.05]	0.59 +- 0.02
i9 [15]	2.33 [2.22, 2.45]	0.63 +- 0.02
i10	2.88 [2.73, 3.03]	0.58 +- 0.02
i11	2.72 [2.59, 2.84]	0.58 +- 0.02
i12	2.67 [2.58, 2.77]	0.68 +- 0.02
i13	1.31 [1.27, 1.36]	0.87 +- 0.02
i14	2.45 [2.41, 2.50]	0.68 +- 0.01
i15	2.26 [2.21, 2.31]	0.73 +- 0.01
i16	2.55 [2.50, 2.60]	0.75 +- 0.01
i17	2.40 [2.37, 2.43]	0.72 +- 0.01
i18	2.16 [2.13, 2.19]	0.73 +- 0.01

Table 2: Comparison of average wire-length measurement (in gatepitches) with model estimates.

Design	Data	Davis	Davis Error (%)	Donath	Donath Error (%)	Christie	Christie Error (%)
(#)	L_a	$L_{avg}(p)$	$E(L_{avg}(p))$	R_{p^*}	$E(R_{p^*})$	$L_{avg}(p^*)$	$E(L_{avg}(p^*))$
i1	3.3	2.4 [2.2,2.6]	-28	2.95 [2.70, 3.22]	-10	2.40 [2.21,2.61]	-27
i2	5.5	3.0 [2.6,3.5]	-46	3.67 [3.53, 3.82]	-33	2.85 [2.75,2.95]	-48
i3	4.2	3.0 [2.6,3.5]	-29	3.42 [3.20, 3.67]	-18	2.68 [2.53,2.85]	-36
i4	4.0	3.0 [2.6,3.5]	-24	4.15 [3.88, 4.44]	5	3.18 [2.99,3.38]	-20
i5	3.7	3.8 [3.1,4.8]	2	4.33 [4.14, 4.53]	16	3.30 [3.18,3.42]	-12
i6	6.2	4.0 [3.2,5.1]	-36	4.63 [4.38, 4.90]	-26	3.49 [3.34,3.66]	-44
i7	5.7	4.0 [3.2,5.1]	-29	4.99 [4.78, 5.21]	-12	3.72 [3.59,3.86]	-34
i8	4.1	4.1 [3.3,5.2]	0	4.50 [4.30, 4.71]	11	3.42 [3.29,3.55]	-16
i9 [15]	4.8	4.1 [3.3,5.2]	-16	4.93 [4.71, 5.17]	2	3.69 [3.55,3.84]	-24
i10	3.6	4.1 [3.3,5.3]	14	4.53 [4.33, 4.74]	25	3.44 [3.31,3.57]	-5
i11	4.2	4.2 [3.3,5.4]	1	4.59 [4.41, 4.79]	10	3.48 [3.37,3.61]	-17
i12	9.3	4.8 [3.7,6.4]	-49	6.45 [6.21, 6.70]	-31	4.69 [4.54,4.84]	-50
i13	9.5	4.9 [3.7,6.6]	-49	10.1 [9.66, 10.6]	6	7.04 [6.74,7.36]	-26
i14	7.0	4.9 [3.7,6.7]	-30	6.61 [6.44, 6.78]	-6	4.79 [4.69,4.90]	-32
i15	8.1	4.9 [3.7,6.7]	-39	7.44 [7.22, 7.68]	-8	5.32 [5.17,5.47]	-35
i16	10.4	5.0 [3.8,6.8]	-52	7.85 [7.67, 8.04]	-24	5.58 [5.46,5.70]	-46
i17	8.7	5.6 [4.1,7.9]	-36	8.27 [8.10, 8.45]	-5	5.87 [5.76,5.98]	-33
i18	9.5	5.7 [4.1,8.2]	-40	8.85 [8.64, 9.07]	-7	6.24 [6.10,6.37]	-34

Table 3: Comparison of total wire-length measurement (in gatepitches) with model estimates.

Design	Data [15]	Davis [15]	Davis Err (%)	Donath	Donath Err (%)	Christie	Christie Err (%)
(#)	L_T	$L_{tot}(p)$		$L_{tot}(R_{p^*})$		$L_{tot}(p^*)$	
i1	305.5	220.5 [201.3,243.2]	-28	274.5 [251.4,299.7]	-10	223.0 [205.7, 243.1]	-27
i2	1745.8	944.4 [822.1, 1098.0]	-46	1166.7 [1121.2, 1214.4]	-33	905.5 [874.8, 938.0]	-48
i3	847.6	605.6 [526.6, 704.9]	-29	848.3 [792.4, 909.4]	0	664.8 [627.9, 705.8]	-22
i4	1011.2	764.7 [664.1, 891.3]	-24	1057.9 [988.4, 1131.9]	5	810.0 [761.8, 862.7]	-20
i5	2999.5	3063.3 [2500.1,3826.1]	2	3464.8 [3313.0, 3625.8]	16	2636.6 [2540.6, 2738.9]	-12
i6	6218.3	3982.3 [3211.3,5041.1]	-36	4799.9 [4542.2, 5076.5]	-23	3622.5 [3459.9, 3797.7]	-42
i7	4731.2	3348.7 [2699.9,4239.9]	-29	4374.4 [4190.1, 4568.3]	-8	3263.5 [3146.5, 3387.1]	-31
i8	4261.1	4269.2 [3427.3,5431.2]	0.1	4731.0 [4524.0, 4950.6]	11	3590.9 [3460.7, 3729.4]	-16
i9	4472.9	3769.5 [3024.3,4798.8]	-16	4762.4 [4546.6, 4990.8]	6	3562.4 [3425.9, 3707.2]	-20
i10	4140.6	4726.3 [3778.8,6040.3]	14	5195.2 [4963.8, 5441.7]	25	3943.4 [3797.9, 4098.4]	-5
i11	4312.9	4341.7 [3448.7,5589.4]	1	4916.2 [4714.9, 5129.1]	14	3728.9 [3602.6, 3862.5]	-14
i12	19794.9	10193.4 [7795.5,13691.2]	-49	14353.6 [13819.4, 14910.8]	-27	10421.2 [10086.3, 10771.4]	-47
i13	21765.9	11159.9 [8481.9,15094.0]	-49	23118.7 [22081.2, 24191.3]	6	16110.1 [15420.7, 16830.9]	-26
i14	16555.1	11623.6 [8806.3,15777.1]	-30	16069.9 [15663.4, 16488.3]	-3	11650.7 [11396.5, 11912.6]	-30
i15	20318.6	12374.6 [9363.1,16821.1]	-39	19252.5 [18663.0, 19860.9]	-5	13751.1 [13379.6, 14135.7]	-32
i16	31544.6	15215.2 [11479.4,20749.2]	-52	24181.2 [23609.1, 24766.9]	-23	17174.0 [16812.2, 17545.5]	-46
i17	38034.0	24362.2 [17730.2,34593.6]	-36	37329.3 [36538.7, 38137.7]	-2	26484.7 [25992.8, 26988.4]	-30
i18	43767.3	26291.6 [19002.1,37625.6]	-40	41603.5 [40601.1, 42631.1]	-5	29315.9 [28691.6, 29956.9]	-33

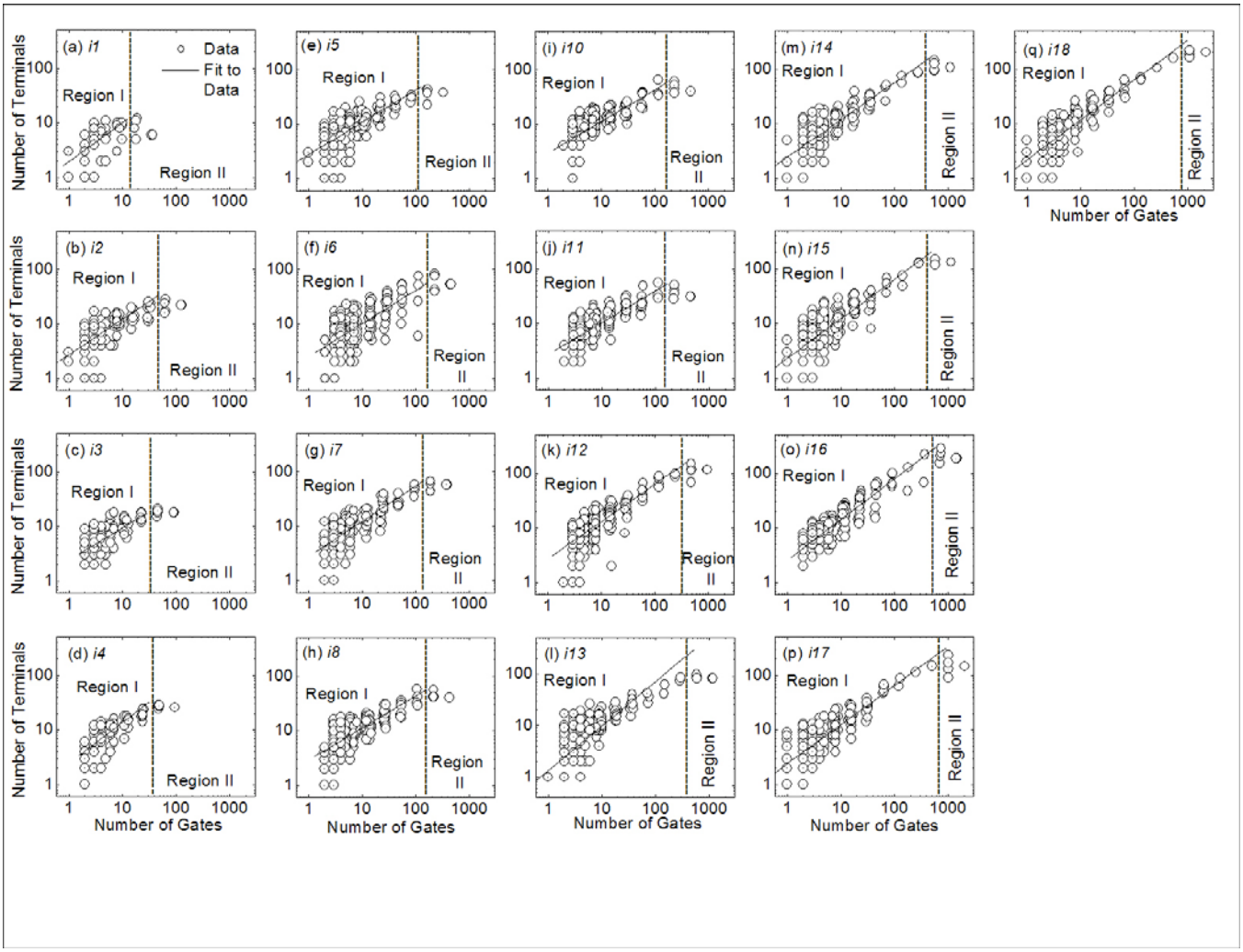

Figure 2. Number of terminals as a function of the number of gates (a)-(q) for designs i1-i8 and i10-i18 in the POWER4 IFU.

Table 4. Comparison of the total measured wire-length of 226,826.9 gatepitches for all of the control logic in the POWER4 IFU with three estimates.

Model	*Total Wire-Length Estimate [range]*	*Error (%)*
Donath	211500.4 [204923.8, 218325.2]	-7
Davis	141256.9 [106963.1,192256.1]	-38
Christie	151859.2 [147683.8, 156212.2]	-33

Table 4 shows three estimates of the total wire-length in all of the *IFU* control logic; these estimates are obtained by taking the sum of the contributions of all of the designs shown in Table 3. Table 4 compares these estimates with the total measured wire-length of *226,826.9 gatepitches.* The results show that the total wire-length estimate provided by the Donath model agrees most closely, to within 7%, with the total measured wire-length.

4. INTERCONNECT REQUIREMENTS IN FUNCTIONAL UNITS

In the previous section, three estimates are presented for the wire-length requirements in one functional unit of the *POWER4* core, and these estimates are compared with measurements. In this section, these results are extended to obtain estimates of the wire-length requirements in the five other functional units in the *POWER4*. These units are the *Floating Point Unit (FPU)*, *Fixed Point Unit (FXU)*, *Instruction Decode Unit (IDU)*, *Instruction Sequence Unit (ISU)*, and *Load Store Unit (LSU)*. The locations of these units are shown in Fig. 4.

To obtain these estimates, we observe that the estimates of average wire-length provided for the *IFU* designs tend to increase linearly as the number of gates increases, as shown in the log-log plots in Figs. 5(a)-(c). Linear least-squares fits to these estimates are shown as the solid lines. The fits are provided in the plots and are written as the expressions,

$$r_{p^*} = 0.82\left(n_{gates}\right)^{0.27}, \tag{2a}$$

$$l_{avg,p} = 0.98\left(n_{gates}\right)^{0.25}, \tag{2b}$$

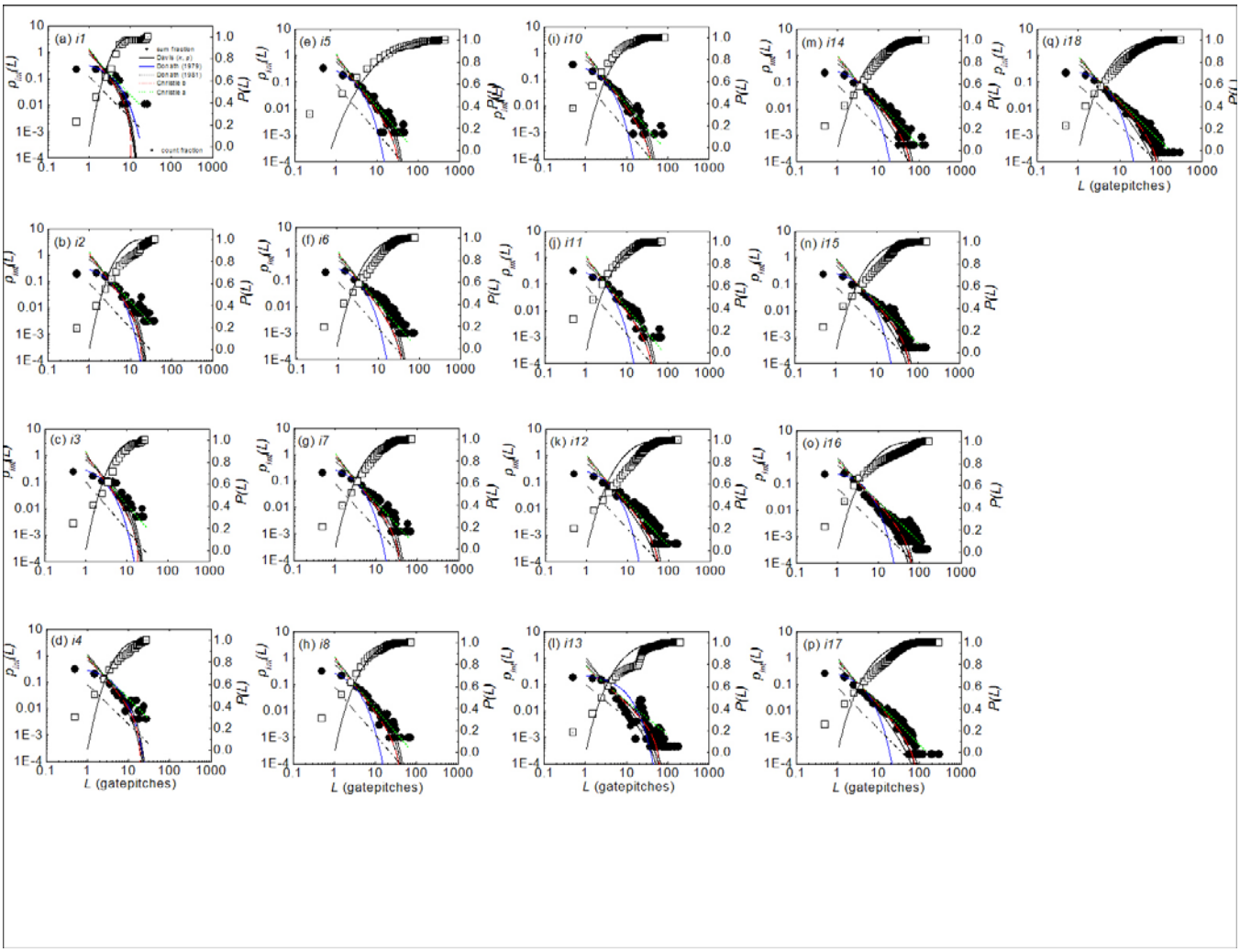

Figure 3. Normalized probability density (left-hand side ordinate) and cumulative interconnect distributions (right-hand side ordinate) for designs i1-i8 and i10-i18 in the POWER IFU.

$$l_{avg,p^*} = 0.77\left(n_{gates}\right)^{0.24}, \tag{2c}$$

where the values and number of significant figures of the coefficient and exponent in each expression are provided by the linear fit; the variable r_{p^*} represents the estimate provided by the Donath model (as shown in Fig. 5(a)); the variable $l_{avg,p}$ represents the estimate provided by the Davis model (as shown in Fig. 5(b)); and the variable l_{avg,p^*} represents the estimate provided by the Christie model (as shown in Fig. 5(c)).

We now make the assumption that Eqns. 2(a)-(c) can be used to obtain average wire-length estimates for the rest of the control logic designs, where the value of N_{gates} is known for each design. This assumption is valid because all of the control logic designs in this chip are synthesized, placed, and routed with the same set of CAD software programs [1]. These CAD programs perform all the decision-making about the number of gates, number of signals, placement, and wiring for each control logic design based on an input logic specification in an ascii file (VHDL).

Expressions for the total wire-length in each design are obtained by multiplying the expressions in Eqns. 4(a)-(c) and the number of nets. A plot of the number of nets N_{nets} as a function of N_{gates} for 18 *IFU* designs is shown in Fig. 6. The data in this figure shows that the number of nets also increases linearly as the number of gates increases. A linear least-squares recursive fit to this data is shown as the solid line in Fig. 6. The fit is also provided in the plot and can be written as the expression,

$$n_{nets} = 1.96\left(n_{gates}\right)^{0.90}, \tag{3}$$

where the values of the coefficient and exponent in this expression are provided by the linear fit. We make the assumption that Eqn. 3 can be used to obtain estimates of the number of nets for the rest of the control logic designs. This assumption is valid because all of the control logic in the chip is synthesized with the same set of CAD software programs [1], as discussed earlier.

The product of the expression in Eqn. 3 with the expressions in Eqn. 2(a)-2(c) provides estimates of the total wire-length. Taking this product produces three estimates of total wire-length that can be written as the expressions,

$$R_{tot,p^*} = \sum_{j=1}^{N} n_{nets}^{j} r_{p^*}^{j}, \tag{4a}$$

$$L_{tot,p} = \sum_{i=1}^{N} n_{nets}^{i} l_{avg,p}^{i}, \tag{4b}$$

$$L_{tot,p^*} = \sum_{k=1}^{N} n_{nets}^{k} \, l_{avg,p^*}^{k} \,, \tag{4c}$$

where the sums *i*, *j*, and *k* are taken over the *N* designs in each unit; R_{tot,p^*} represents the total wire-length estimate provided by the Donath model; $L_{tot,p}$ represents the total wire-length provided by the Davis model; and L_{tot,p^*} represents the total wire-length provided by the Christie model. For the case of the *POWER4*, *N* = 12 for the *FPU*; *N* = 4 for the *FXU*; *N* = 18 for the *IDU*; *N* = 16 for the *ISU*; and *N* = 32 for the *LSU*.

Estimates of the total wire-length in each unit are obtained by evaluating Eqn. 4(a)-4(c) as functions of N_{gates}; these values are shown in Table 5. This table also shows a comparison of these estimates with the total measured wire-length in each unit and shows that the total wire-length estimates underestimate the measurements. The errors (in %) between the measurements and the estimates are also shown. The results show that the total wire-length estimate derived with the average wire-length estimate provided by the Donath model and Eqn. 4(a) agrees to within 12% with measurements; the total wire-length estimate derived with the average wire-length estimate provided by the Davis model and Eqn. 4(b) agrees to within 6% with measurements; and the total wire-length estimate derived with the average wire-length estimate provided by the Christie model and Eqn. 4(c) agrees to within 35% with measurements.

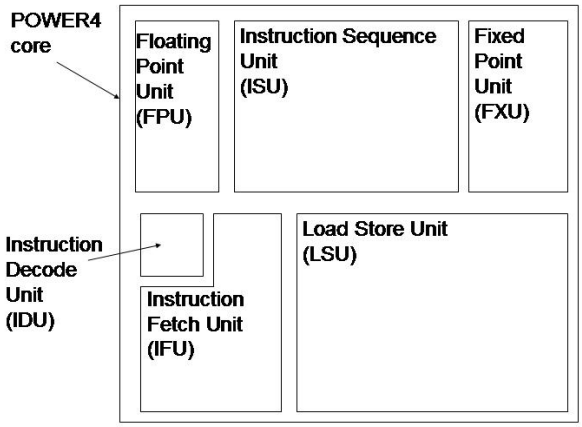

Figure 4. The POWER4 core and the locations of the six functional units.

5. INTERCONNECT REQUIREMENTS IN A MICROPROCESSOR

The purpose of this section is to present a measurement and three estimates of the interconnect requirements for control logic in all of the functional units in the *POWER4* microprocessor core. These estimates follow from the results presented in Section 4.

The measurement of the total wire-length of all of the control logic in the *POWER4* core is obtained by taking the sum of the total wire-length of all of the designs in the six units. Estimates of the total wire-length are obtained by taking the sum of the total wire-length estimates in all six units, according to the expressions,

$$R_{tot,p^*}^{core} = \sum_{n=1}^{6} R_{tot,p^*}^{n}, \tag{5a}$$

$$L_{tot,p}^{core} = \sum_{m=1}^{6} L_{tot,p}^{m}, \tag{5b}$$

$$L_{tot,p^*}^{core} = \sum_{q=1}^{6} L_{tot,p^*}^{q}, \tag{5c}$$

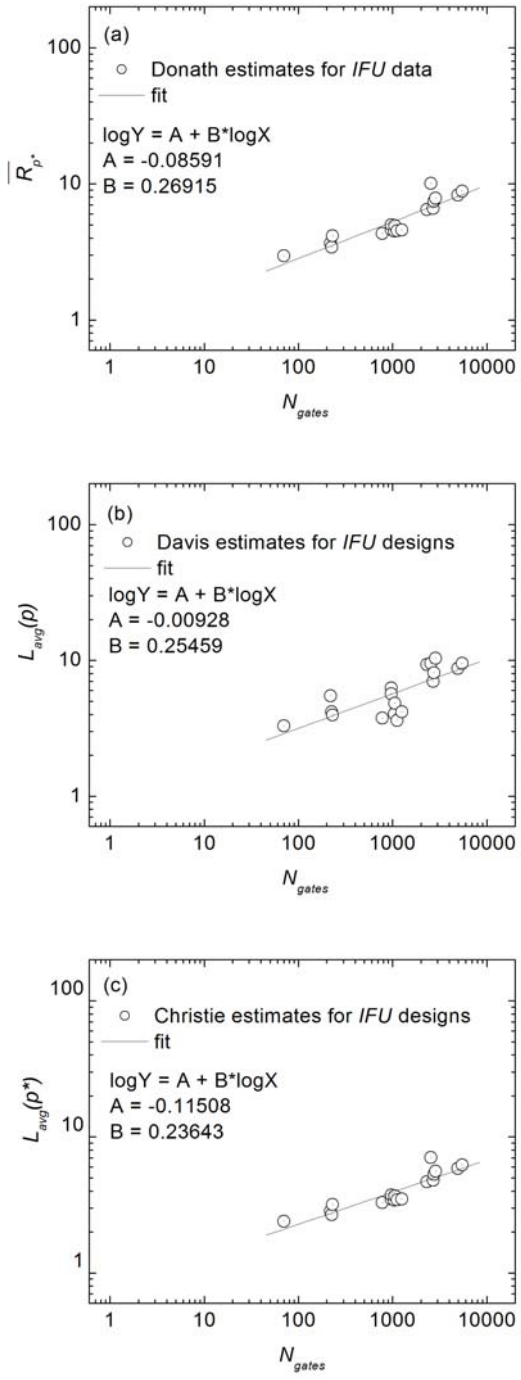

Figure 5. Log-log plots of the average wire-length estimates of the Donath (a), Davis (b), and Christie (c) models for 18 IFU designs as a function of N_{gates}. The solid lines represent the linear fits to the data in each plot. The number of significant figures is provided by the fit.

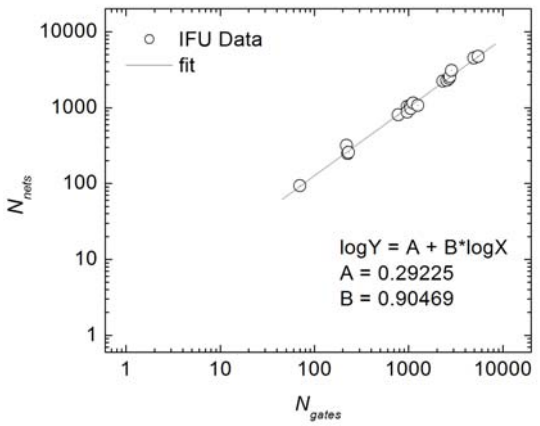

Figure 6. A log-log plot of N_{conn} as a function of N_{gates} for the 18 control logic designs in the POWER4 IFU. The solid line represents a linear fit to the data in the plot. The number of significant figures is provided by the fit.

where the sums over *m*, *n*, and *q* are taken over all of the six units; R_{tot,p^*}^{core}, $L_{tot,p}^{core}$, and L_{tot,p^*}^{core} represent estimates of total wire-length provided by the Donath, Davis, and Christie models, respectively; and where R_{tot,p^*}^{n}, $L_{tot,p}^{m}$, and L_{tot,p^*}^{q} are the total wire-length estimates in the m^{th} unit, n^{th} unit, or q^{th} unit. These expressions can be evaluated with the results of the previous sections, and the values of the total wire-length estimates in the entire *POWER4* core is shown in Table 6.

Table 6 shows that the estimate of the total wire-length based on the Donath model and Eqns. 2(a), 3, 4(a), and 5(a) underestimates the total wire-length measurement by 35%. The results also show that the estimate of the total wire-length based on the Davis model and Eqns. 2(b), 3, 4(b), and 5(b) underestimates the total wire-length measurement by 31%. The estimate of the total wire-length based on the Christie model and Eqns. 2(c), 3, 4(c), and 5(c) underestimates the total wire-length measurement by 53%.

Note that the expressions in Eqn. 5 can also be used to assess the potential impact on the total quantity of interconnect that is required as a result of the addition of one or more control logic designs. For these cases, the values of N_{gates} for the proposed designs are known or can be estimated from empirical measurements. Values of N_{gates} can then be substituted into Eqns. 2-4, and finally an estimate of total wire-length can be obtained with Eqn. 5. Note that the addition of a design with a large value of N_{gates} increases the estimate of the total wire-length more than the addition of a design with a smaller value of N_{gates}.

6. DISCUSSION

This paper presents a complete assessment of the interconnect requirements for control logic designs in a dual-core high-performance microprocessor. The assessments include estimates of the wire-length distributions, average wire-length, and total wire-length provided by the models of Donath, Davis, and Christie. Comparisons of the model distributions with measured distributions in *POWER4* control logic designs show that the distributions provided by the models tend to underestimate the number of signals with large values of wire-length and tend to overestimate the number of signals with small values of wire-length. The results show that of all the existing models assessed in this study, the curvature of the distributions provided by the Davis model most closely approximates the curvature of the measured distributions [15]. The results also show that the Donath model provides estimates that agree most closely with measurements for the majority of the designs. In particular, the estimates provided by the Donath model show closest agreement with measurements for the seven largest IFU designs (*i12* – *i18*) that have values of the measured average wire-length that exceed 7.0 *gatepitches per signal*.

Comparisons of estimates of the total wire-length with the measurements for the other five functional units (*FPU*, *FXU*, *IDU*, *ISU*, *LSU*) show that the estimates underestimate the measurements. The results show that the estimates agree the measurements to within 35% for the case in which the estimates are provided by the Donath model; to within 31% for the case in which the estimates are obtained with the Davis model; and to within 53% for the case in which the estimates are obtained with the Christie model. Note that these estimates underestimate the actual measured values because the average wire-length estimates provided by the models for the original set of *IFU* designs underestimated the actual average wire-length measurements. It is therefore expected that as the models improve, the agreement of the estimates with measurements will also improve.

Possible reasons for the differences between the model estimates and measurements are now discussed; these reasons are listed briefly in [15]. First, the models assume that the designs are square and have unity occupancy. In this study, the designs differ from these assumptions in a number of ways: the designs (a) are not completely filled with logic gates, (b) are slightly rectangular; (c) contain logic blocks that are typically rectangular, with widths that are typically less than the height; and (d) are generated with a complex placement methodology that combines commercial tools with internal tools and that is difficult to analyze in a single procedure. Second, the models assume that the signals in each design have unity fan-out. In this study, the majority of signals have unity fan-out, and the average fan-out is close to unity. However, the designs also contain signals with very high fan-out; some of these signals with high fan-out are associated with the clocking circuitry. Third, the models assume that the blocks are interconnected in the physical design. In this study, the designs contain an additional network of clocking circuitry that is superimposed on the interconnected logic gates. The purpose of the clocking circuitry is to synchronize the logic signals in order to ensure that the designs satisfy the cycle time requirement. Fourth, the range of applicability of Rent's rule covers only half the range of the gate partition sizes; the remaining range for Rent's rule in Region II is modeled in [22]. Future work is needed to assess the effects of designs that are not square [23], contain synchronization circuitry, and contain signals with an average signal fan-out that is greater than unity [24].

Table 5: Comparison of total wire-length measurements in the POWER4 FPU, FXU, IDU, ISU, and LSU with estimates.

POWER4 Unit	*Measured Total Wire-Length [15] (gatepitches)*	*Donath, Eqns. 1-4*	*Donath Err (%)*	*Davis, Eqns. 1-4*	*Davis Err (%)*	*Christie, Eqns.1-4*	*Christie Err (%)*
FPU	21915.9	14279	-35	15700	-29	11037	-50
FXU	26030.9	15512	-40	16600	-36	11339	-56
IDU	148700.6	130990	-12	140000	-6	96285	-35
ISU	309901.8	211120	-32	224000	-28	152030	-51
LSU	553852.8	464370	-16	492000	-11	333050	-40

Table 6. Comparison of the total measured wire-length of 1.28723E6 gatepitches [15] in the POWER4 with estimates.

Model and Eqns. 1-5	*Total Wire-Length Estimate (gatepitches)*	*Error (%)*
Donath	836280	-35
Davis	889000	-31
Christie	603740	-53

7. CONCLUSION

This paper presents a complete assessment of existing on-chip wire-length distribution models and estimates of the quantity of interconnect in all of the control logic in the *POWER4*, a high-performance dual-core microprocessor. The paper also presents a comparison of these estimates with actual wire-length measurements that are extracted from real chip designs. Based on these results, estimates of interconnect requirements are obtained for the other five functional units in the *POWER4* and for the entire core itself. For the total wire-length for all of the control logic designs in one unit (the *Instruction Fetch Unit*), the results show that the estimates can agree to within 7% of the total wire-length measurement. From these results, estimates are obtained for the quantity of interconnect in the other five units, and the estimates are compared with actual measurements. Finally, estimates are obtained for the total wire-length in all of the control logic designs in the *POWER4* core. The results show that the closest estimates agree with the measurement of the actual total wire-length to within 31% and 34%.

8. ACKNOWLEDGMENT

We thank I. Bendrihem and K. Lewis at the IBM T. J. Watson Research Center in Yorktown Heights, NY, for their superior IT support. We thank J. Davis and G. Lopez at the Georgia Institute of Technology for discussions about *gatepitch.* We also thank G. Karypis and N. Selvakkvamaran at the University of Minnesota for discussions about *hMeTIS* and thank D. Stroobandt and J. Dambre at the Universiteit Gent in Belgium for correspondence about their Ph.D. dissertations and Rent's parameters.

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