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Methods for Accurate Wirelength Estimation of Functional Circuitry in ULSI Chips

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Abstract

An accounting for circuitry type in *ULSI* chips within the context of the historically-equivalent interpretation of Rent's rule is needed for an assessment of existing on-chip wirelength distribution models. Although prior assessments of these models have separately considered the effects of these two factors (namely, circuitry type and Rent's rule), there does not exist an assessment for today's *ULSI* circuits that takes into account the role of circuitry type within the context of this interpretation of Rent's memos. Providing an assessment that properly accounts for both factors is needed and is the goal of this paper. The main contributions of this paper are: (1) a method that takes into account both factors for assessments of on-chip wirelength distribution models, and (2) wirelength estimates and model wirelength distributions that show much improved agreement with measurements. This paper presents assessments based on these methods for 100 chip designs in the *POWER4* microprocessor. The results presented in this paper show that the wirelength estimates now typically closely approximate the measurements and that the total wirelength estimate for all 100 designs agrees with the measured total wirelength to within 23%.

Keywords

ULSI, wirelength distribution models, Rent's rule, external Rent parameters, functional circuitry.

I. Introduction

Wirelength estimates that are of sufficient accuracy for wirelength estimation in *ULSI* chips are needed. Existing wirelength estimates have been provided by assessments of the wirelength distribution models of Donath [1], [2], Davis [3], [4], [5], [6], and Christie [7], [8], [9], [10], [11], [12], [13]. These assessments have considered separately the effects of two input factors, namely: (1) the type of chip circuitry and (2) the interpretation of Rent's rule. The choices of these factors that are addressed in these assessments are: (1a) the entire group of circuitry, or (1b) the subset of functional circuitry. The two choices of the interpretation of Rent's rule are: (2a) the 1971 interpretation [14], or (2b) the historically-equivalent interpretation [15]. While prior assessments of the wirelength distribution models have separately considered circuitry type or the interpretation of Rent's rule, an assessment is needed to account properly for circuitry type within the context of the historically-equivalent interpretation of Rent's rule.

The goal of this paper is to present an assessment that satisfies these requirements. To achieve this goal, the main contribution of this paper is a method to consider both factors

together and to properly take both factors into account in the analysis. The method presented in this paper are applied to 100 ASIC-like control logic designs in the *POWER4* chip [18], [19]. The results show that the wirelength estimates provided by these methods (1) show improved agreement with measurements for 79 of the 100 designs compared with prior work, (2) now typically closely approximate the wirelength measurements, and (3) are of suitable quality for wirelength estimation in *ULSI* chips.

II. Background

The separate impact of the input factors on wirelength estimates provided by existing on-chip wirelength distribution models has been considered in prior work [15], [16], [17]. For example, in [16], the inputs to the models are (1a) based on the entire group of circuitry and (2a) obtained with the 1971 interpretation of Rent's rule [14]. The results presented in [16] show that the estimates underestimate the average wirelength measurements by $-50.2\% \pm 18.5\%$. In [15], the inputs to the model are (1a) based on the entire group of circuitry and (2b) derived with the historically-equivalent interpretation of Rent's memos presented in [15]. The majority of the estimates in [15] show improved agreement with average wirelength measurements compared with the results presented in [16]; the results in [16] show that on average the estimates overestimate the average wirelength measurements by $21.4\% \pm 39.7\%$. Note that both of these prior assessments have considered the entire group of circuitry although the models are derived for function type signals and circuitry.

Therefore, to account properly for circuitry type in subsequent assessments such as that in [17], the portion of the circuitry that is functional circuitry is extracted from the entire group of circuitry. The resulting functional circuitry is referred to as a *functional netlist*. From the functional netlist, revised model inputs are extracted based on the 1971 interpretation of Rent's rule [14]. Model inputs that are derived from the functional netlist are referred to as *functional Rent parameters*. A review of the methods to extract the *functional netlists* and the *functional Rent parameters* is given in [17]. The results presented in [17] show that the estimates underestimate the average wirelength measurements by $-46.6\% \pm 21.5\%$, which demonstrates improved agreement compared with prior results[16] that are also based on the 1971 interpretation of Rent's rule.

III. Factors that impact assessments of wirelength distribution models

This section reviews two factors that impact assessments of on-chip wirelength distribution models. The first factor is circuitry type, for which assessments can consider two choices, namely functional circuitry and the entire group of circuitry. The second factor is the interpretation of Rent's rule, for which assessments can consider two choices, namely the 1971 interpretation and the historically-equivalent interpretation.

A. Circuitry type

Today's *ULSI* chip designs typically contain two types of circuitry - *functional circuitry* and *synchronization circuitry* - and two types of signals - *functional signals* and *synchronization signals*. A detailed discussion of the two circuitry types and the two signal types is given in [17]. For functional circuitry, examples of functional signals include signals that perform functions such as that of addition or multiplication. The quantity, drive strength, and type of gates for functional logic is specified by an automated logic synthesis program that selects and assembles a group of gates that satisfy project constraints. These gates occupy a smaller portion of chip real estate compared with the real estate occupied by synchronization circuitry in typical *ULSI* chip designs, as discussed in [17].

B. Interpretation of Rent's rule

The 1971 interpretation of Rent's rule is discussed in [6], [14], and the historically-equivalent interpretation of Rent's rule is discussed in [15]. The former interpretation provides a method to extract values of the *topological Rent parameters* and the *external Rent parameters*. This interpretation provides one set of *external Rent parameters* that are inputs to the Davis model and that are obtained from least-squares linear fits to log-log plots of the total number of input/output pins T_{IO} as a function of the number of used gates N_{gates} [3], [6]. In [3], [4], the external Rent parameters obtained with this method are represented with the notation $\{k, p\}$.

The latter interpretation of Rent's rule provides a method to extract a second set of *external Rent parameters* from least-squares linear fits to log-log plots of the number of used connections N_{conn} as a function of the number of used gates N_{gates}, where N_{conn} and

N_{gates} are given by the expressions,

$$N_{conn} = F_{total} + N_{nets} - T_{IO}, \tag{1}$$

and

$$N_{gates} = N_{all} - N_{unconn} - N_{spare} - N_{fill} - N_{decap}, \tag{2}$$

where the terms F_{total}, N_{nets}, N_{all}, N_{unconn}, N_{spare}, N_{fill}, and N_{decap} represent, respectively, the total fanout, number of nets, the total number of gates, the number of unconnected gates, the number of spare gates, the number of filler gates, and the number of decoupling capacitors. In [15], the external Rent parameters obtained with this method for the entire group of circuitry are represented with the notation $\{k_R, p_R\}$.

IV. Review of the wirelength distribution model

The *external Rent parameters* derived for functional circuitry within the context of the historically-equivalent interpretation of Rent's rule are referred to as *external functional Rent parameters* and are represented with the notation $\{k_R^f, p_R^f\}$; recall that in [17], the *external functional Rent parameters* derived with the 1971 interpretation of Rent's rule are represented with the notation $\{k^f, p^f\}$.

In this paper, the *external functional Rent parameters* $\{k_R^f, p_R^f\}$ are provided as inputs to the Davis (1998) model [3], [4], [5] to obtain estimates for the average wirelength and wirelength distributions. The model provides expressions for two types of wirelength distribution functions, namely, the interconnection density function (the *idf*) and the cumulative interconnection density function (the *cumulative idf*). Some assumptions of this model are: square chip designs, completely tiled designs (that is, designs with unity area occupancy), signals with unity fanout, and square logic gates with height described as the *gatepitch*.

V. Method to obtain external functional Rent parameters within the context of the historically-equivalent interpretation of Rent's rule

The purpose of this section is to describe methods to obtain values of the *external functional Rent parameters* $\{k_R^f, p_R^f\}$ within the context of the historically-equivalent in-

terpretation of Rent's rule. The procedure to extract the values of $\{k_R^f, p_R^f\}$ proceeds as follows.

First, a count is made of the number of connections $N_{conn}(f)$ for functional signals and circuitry, where the parameter f represents *functional* signals and circuitry. In this case, Eqn. 1 takes the form,

$$N_{conn}(f) = F_{total}(f) + N_{nets}(f) - T_{IO}(f), \tag{3}$$

where the quantities N_{conn}, $F_{total}(f)$, $N_{nets}(f)$, and $T_{IO}(f)$ represent the total number of used connections, total fanout, total number of nets, and number of input/output pins, respectively, that are associated with functional circuitry. A count is also made of the number of gates $N_g(f)$ that implements the logic function.

Next, a log-log plot of $N_{conn}(f)$ as a function of $N_g(f)$ is generated [3], [4], [6] for the designs in each functional unit. For each plot, the values of $\{k_R^f, p_R^f\}$ are extracted from a least-squares linear regression fit of the data to the following expression,

$$Log(N_{conn}(f)) = Log(k_R^f) + p_R^f \times Log(N_g(f)). \tag{4}$$

We now apply these methods to assessments for 100 *POWER4* chip designs. Data obtained from these designs with Eqn. 3 is plotted in the six graphs shown in Fig. 1. In this figure, each graph corresponds to data obtained from the designs in each functional unit. With Eqn. 4, six sets of values of the external functional Rent parameters $\{k_R^f, p_R^f\}$ are extracted from the six plots.

Table I summarizes the values of these parameters and compares them with values of the parameters $\{k^f, p^f\}$ that are derived previously [15] for functional circuitry within the context of the 1971 interpretation of Rent's rule. For each set, the values and ranges within one standard deviation for both parameter pairs are also shown in the table. The results in the table demonstrate that with the 1971 interpretation of Rent's memos, $0.68 \leq k^f \leq 37.9$ and $0.21 \leq p^f \leq 0.72$, whereas with the historically-equivalent interpretation of Rent's rule, $1.7 \leq k_R^f < 6.1$ and $0.89 \leq p_R^f \leq 1.08$. Note that the values of k_R^f are greater than 1, that the range of k_R^f is smaller than the range of k^f, and that the values of p_R^f are on the order of unity for each of the six units.

VI. Comparison of wirelength estimates with wirelength measurements for functional circuitry

In the previous section, methods are presented to extract values of the *external functional Rent parameters* $\{k_R^f, p_R^f\}$ within the context of the historically-equivalent interpretation of Rent's rule. In this section, results are presented to show how the values of these parameters impact estimates of the three wirelength characteristics:

(1) Interconnection distributions of functional signals,

(2) Average wirelength of functional signals,

and

(3) Total wirelength of functional signals.

A. Interconnection distributions of functional signals

This section discusses two types of interconnection distributions: (1) interconnection density functions (that is, *idf's*), and (2) cumulative interconnection density functions (that is, *cumulative idf's*). Estimates of the *idf's* for functional circuitry in *ULSI* chip designs are obtained by evaluating Eqns. 3 - 5 in [3] as functions of $\{k_R^f, p_R^f\}$. Estimates of the *cumulative idf's* for functional circuitry are obtained by evaluating Eqns. B20 - B22 in [3] as functions of $\{k_R^f, p_R^f\}$.

The *idf's* and *cumulative idf's* obtained by evaluating these expressions in the model are compared with the corresponding measured interconnection distributions and measured cumulative interconnection distributions that are obtained by measuring the wirelengths of the functional signals in the chip designs. To obtain the measured *idf's*, the wirelength of each signal is measured in the chip design, and the number of signals with each value of wirelength is plotted as a function of wirelength (in units of *gatepitches*), where the bin size is taken to be the *gatepitch*. To obtain the measured *cumulative idf's*, the total number of signals having values of wirelengths less than or equal to each value is plotted as a function of wirelength, where the bin size is also taken to be the *gatepitch*.

Figure 2 shows examples of the *idf* and examples of the *cumulative idf* for four *IFU* designs (a) $i1$, (b) $i3$, (c) $i9$, and (d) $i18$. For each design in the figure, the *idf's* are shown on the left-hand ordinate, and the *cumulative idf's* are shown on the right-hand

ordinate. The black dotted lines represent the *idf's* and *cumulative idf's* obtained by evaluating expressions in the model as functions of $\{k^f, p^f\}$ within the context of the 1971 interpretation of Rent's rule; these distributions are also shown in prior work [17]. The red solid lines represent the *idf's* and *cumulative idf's* obtained by evaluating the expressions in the model as functions of $\{k_R^f, p_R^f\}$ within the context of the historically-equivalent interpretation of Rent's rule and are new results presented in this paper.

This figure also compares the *idf's* and the *cumulative idf's* with the corresponding measured distributions for each of the four designs. In this figure, the data for the measured *idf* are shown as solid circles on the left-hand ordinate, and the data for the measured *cumulative idf* are shown as hollow squares on the right-hand ordinate. The figure shows that the distributions obtained by evaluating the models as functions of $\{k_R^f, p_R^f\}$ show better qualitative agreement with the measured distributions compared with the agreement observed for distributions obtained in prior work. For example, the values of the slopes of the estimate *idf's* obtained with $\{k_R^f, p_R^f\}$ (shown as red solid lines) take on less negative values and therefore more closely approximate the values of the slopes of the measured *idf's*. In addition, the estimate *idf's* show improved qualitative agreement with the measured distributions when the value of wirelength becomes large. The figure also shows that the curvature of the estimate *cumulative idf's* obtained with $\{k_R^f, p_R^f\}$ agrees more closely with the curvature of the measured cumulative distributions for three of the four designs ($i1$, $i3$, $i18$) when the value of the wirelength becomes much larger than unity.

B. Average wirelength of functional signals

Estimates of the average wirelength for functional circuitry are obtained by evaluating Eqn. 3 for the model expression for the average wirelength $L_{avg}(p)$ in [4] as functions of the two sets of parameters $\{k^f, p^f\}$ and $\{k_R^f, p_R^f\}$. The values for $L_{avg}(p^f)$ are shown on the left sides of Tables II and IV- VII. The values for $L_{avg}(p_R^f)$ are shown on the right sides of Tables II and IV- VII. Values of the average measured wirelength $L_a(f)$ for the functional signals are obtained from each chip design by dividing the total measured wirelength $L_T(f)$ for all functional signals by the number of functional signals.

Tables II and IV-VII compare the values of $L_a(f)$ for 100 *POWER4* designs with the values of two sets of average wirelength estimates for functional circuitry. The errors (in

%) between the estimates and measurements are given by the expressions, $E(L_{avg}(p^f)) = \frac{L_{avg}(p^f) - L_a(f)) \cdot 100}{L_a(f)}$ and $E(L_{avg}(p_R^f)) = \frac{(L_{avg}(p_R^f) - L_a(f)) \cdot 100}{L_a(f)}$. In these expressions, $E(L_{avg}(p^f))$ represents the error between the model estimate obtained with the 1971 interpretation of Rent's memos and $L_a(f)$; and $E(L_{avg}(p_R^f))$ represents the error between the model estimate obtained with the historically-equivalent interpretation of Rent's memos and $L_a(f)$.

The results in the tables show that the estimates of the average wirelength for functional circuitry typically agree more closely with the average wirelength measurements for the cases in which the historically-equivalent interpretation of Rent's memos is used in the analysis. In particular, the estimates of the average wirelength show improved agreement with measurements for 13 (72%) of 18 *IFU* designs, 12 (100%) of 12 *FPU* designs, 4 (100%) *FXU* designs, 14 (81%) of 18 *IDU* designs, 14 (88%) of 16 *ISU* designs, and 22 (69%) of 32 *LSU* designs. Overall, the estimates of average wirelength presented in this paper show improved agreement with measurements for 79 (79%) of the 100 *POWER4* designs, compared with prior work [17].

C. Total wirelength of functional signals

An estimate of the total wirelength for the functional signals within the context of the historically-equivalent interpretation of Rent's rule for a collection of designs is referred to as $L_{tot}(p_R^f)$ and is given by the expression,

$$L_{tot}(p_R^f) = \sum_{i=1}^{N_{designs}} N_{signals} \times L_{avg}(p_R^f), \tag{5}$$

where $N_{signals}$ is the number of functional signals in each design, and where the sum is taken over all the designs $N_{designs}$. The total measured wirelength $L_T(f)$ is obtained by summing the wirelengths of all functional signals in all designs, and can be written as,

$$L_T(f) = \sum_{i=1}^{N_{designs}} N_{signals} \times L_a(p_R^f). \tag{6}$$

The error (in %) between the total wirelength estimate and the total wirelength measurement is given by the expression, $E(L_{tot}(p_R^f)) = \frac{(L_{tot}(p_R^f) - L_T(f)) \cdot 100}{L_T(f)}$.

Table III compares the total measured wirelength $L_T(f)$ for functional signals in each of the six *POWER4* units with an estimate of the total wirelength $L_{avg}(p_R^f)$ provided

by the model, where the estimates shown on the right side of Table III are obtained by evaluating the model as functions of $\{k_R^f, p_R^f\}$, and the estimates shown on the left side of Table III are obtained by evaluating the model as functions of $\{k^f, p^f\}$. The results in the table show that estimates obtained with $\{k_R^f, p_R^f\}$ agree more closely with measurements and agree to within $\{1\%, 16\%, 32\%, -25\%, -18\%, -34\%, -23\%\}$ with $L_{tot}(p_R^f)$ compared with the agreement seen for results in prior assessments [16], [15], [17] which obtained agreement to within $\{-31\%, -46\%, -55\%, -63\%, -69\%, -55\%, -55\%\}$, respectively.

VII. Discussion

In the previous section, an assessment of on-chip wirelength distribution models for functional circuitry is presented for real chip designs within the context of the historically-equivalent interpretation of Rent's rule. The purpose of this section is to compare the results obtained in this paper with results obtained in prior assessments [16], [15], [17].

Figure 3 shows a comparison of the errors in the average wirelength estimates for the 100 *POWER4* control logic designs considered in three prior assessments with the error distribution obtained in the present assessment. In this figure, the errors obtained in [16] are shown as red open bars, the errors obtained in [15] are shown as green boxed bars, the errors obtained in [17] are shown as blue hashed bars, and the errors reported in the present assessment are shown as black solid bars. This figure shows that the value of the error is minimized with the methods described in the present assessment. Overall, for each of the four assessments, the average error obtained between the model estimates and the actual wirelength measurements is: $-50.2\% \pm 18.6\%$ in [16], $21.4\% \pm 39.7\%$ in [15], $-46.6\% \pm 21.5\%$ in [17], and $20.9\% \pm 42.2\%$ reported in this paper. These results show that the absolute value of the error is reduced slightly for both interpretations of Rent's memos when functional circuitry taken into account; that is, the error is reduced from -50.2% in [16] to -46.6% in [17] with the 1971 interpretation of Rent's rule and from 21.4% in [15] to 20.9% in this paper with the historically-equivalent interpretation of Rent's rule. The results also show that the error is reduced when both circuitry types are considered within the historically-equivalent interpretation of Rent's rule; that is, the error is reduced from -50.2% in [16] to 21.4% in [17] for the entire group of circuitry, and from -46.6% in [17] to 20.9% for functional circuitry. The results presented in this paper show that the average

wirelength estimates and the measurements now agree to within $20.9\% \pm 42.2\%$, which is an improvement compared with results reported in prior work [16], [15], [17].

Results obtained in this paper for total wirelength are now compared with results obtained in prior assessments [16], [15], [17]. Figure 4 shows the error distributions for total wirelength estimates in the three prior model assessments and in the present assessments. The errors obtained for the total wirelength estimates in the three prior assessments are shown as red open bars for [16], green boxed bars for [15], blue hashed bars for [17], and black solid bars for the results of this paper. A comparison of the error distribution shown in this figure shows that the assessment presented in this paper provides the best agreement between the total wirelength estimate and the total wirelength measurement for the four units that contain the largest total wirelength, namely, the *IFU*, *IDU*, *ISU*, and *LSU*. In these cases, the results in the present assessment show that the total wirelength estimates agree to within 1%, -25%, -18%, and -34%, respectively, of the measured total wirelength in these units.

The results presented in this paper also show that the overall total wirelength estimate for the 100 *POWER4* designs shows an improved agreement with measurements and now agrees to within 23% of the total wirelength requirement. This result compares favorably with results obtained in prior assessments that report agreement to within -58%, 30%, and -55% in [16], [15], and [17], respectively.

A few reasons for the remaining differences between the model estimates and measurements are:

(1) The model assumes square floorplans that are tiled completely with square blocks, whereas real chip designs are rectangular, are incompletely tiled, and contain rectangular logic gates. Future work is needed to compare designs with aspect ratios that deviate greatly from square with models that take into account the effects of rectangular design [20].

(2) The model assumes that the functional signals have unity fanout. Future work is needed to compare wirelength measurements in chip designs that contain signals with large fanout with model estimates that take into account the effects of multi-terminal nets [21].

VIII. Conclusions

This paper considers the impact of functional circuitry on assessments of wirelength distribution models for *ULSI* chip designs within the context of the historically-equivalent interpretation of Rent's rule. The results presented in this paper show that good agreement can be obtained between wirelength estimates and actual wirelength measurements by taking these two factors - circuitry type and the interpretation of Rent's rule - properly into account in the analysis. The results presented in this paper show that for cases in which both factors are taken properly into account, the estimate distributions provided by the models (1) show improved agreement when the value of the wirelength becomes large and (2) exhibit slopes that qualitatively agree more closely with the slopes of the measured distributions. Average wirelength estimates presented in this paper show improved agreement with measurements for 79 of 100 *POWER4* ASIC-like control logic designs, including 13 (72%) of 18 *IFU* designs, 12 (100%) of 12 *FPU* designs, 4 (100%) of 4 *FXU* designs, 14 (81%) of 18 *IDU* designs, 14 (88%) of 16 *ISU* designs, and 22 (69%) of 32 *LSU* designs. Overall, for the *POWER4* core, this paper reports an improved total wirelength estimate that now agrees to within 23% with the measured total wirelength requirement in this chip.

IX. Acknowledgments

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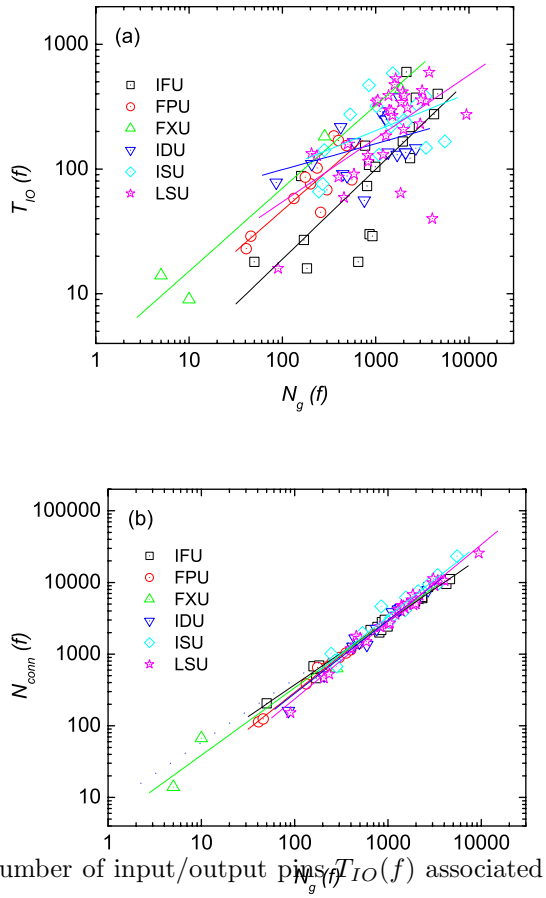

Fig. 1. (a) The number of input/output pins $T_{IO}(f)$ associated with functional circuitry as a function of used gates $N_{gates}(f)$ associated with the same functional circuitry, for the six functional units in the *POWER4* core. (b) The number of connections $N_{conn}(f)$ associated with *functional* signals as a function of the number of gates $N_g(f)$. Least-squares linear fits of data in (b) to Eqn. 4 provide values for $\{k_R^f, p_R^f\}$ shown in Table I.

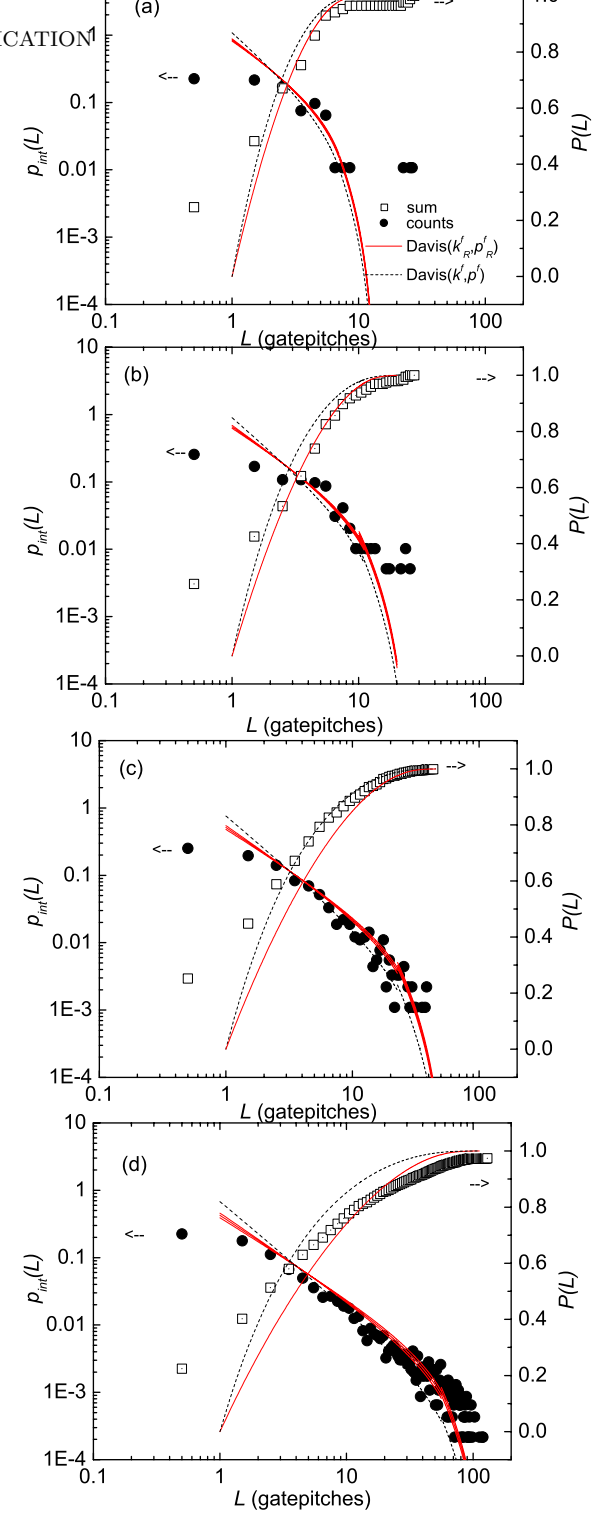

Fig. 2. Measured interconnection density functions for functional circuitry (left abscissa, solid circles) and measured cumulative interconnection density functions (right abscissa, hollow squares) are shown with new estimates provided by the Davis model (red solid lines) evaluated as functions of $\{k_R^f, p_R^f\}$. Previous estimates are also shown, in which the Davis model (black dashed lines) is evaluated for functional circuitry as functions of $\{k^f, p^f\}$ [15]. Comparisons are shown for four *POWER4 IFU* designs: (a) *i1*, (b) *i3*, (c) *i9*, and (d) *i18*.

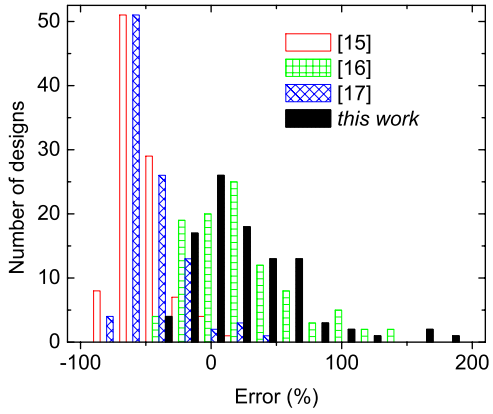

Fig. 3. Error distributions of average wirelength for 100 *POWER4* control logic designs obtained for four assessments of on-chip wirelength distribution models. The errors are measured between the model estimates and average wirelength measurements in [16] shown as red open bars, in [15] shown as green boxed bars, in [17] shown as blue hashed bars, and this work shown as black solid bars. The average error between the model estimates and actual wirelength measurements is $-50.2\% \pm 18.6\%$ [16], $21.4\% \pm 39.7\%$ [15], $-46.6\% \pm 21.5\%$ [17], and $20.9\% \pm 42.2\%$ (this work).

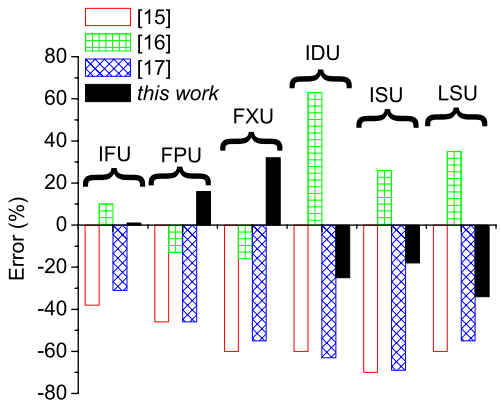

Fig. 4. Error distributions of for total wirelength in the six *POWER4* functional units for the four assessments of on-chip wirelength distribution models. The errors are measured between the model total wirelength estimates and total wirelength measurements in [16] shown as red open bars, in [15] shown as green boxed bars, in [17] shown as blue hashed bars, and this work shown as black solid bars.

TABLE I

COMPARISON OF $\{k^f, p^f\}$ AND $\{k_R^f, p_R^f\}$ FOR THE SIX *POWER4* FUNCTIONAL UNITS. RANGES INDICATES VALUES WITHIN ONE STANDARD DEVIATION OF THE PARAMETER PAIRS.

POWER4	*Rent [14], [15]*		*Rent (this work)*	
Unit (# designs)	k^f *[range]*	p^f *[range]*	k_R^f *[range]*	p_R^f *[range]*
IFU designs (18)	$0.68[0.24, 1.90]$	$0.72[0.57, 0.87]$	$6.1[5.2, 7.3]$	$0.89[0.87, 0.92]$
FPU designs (12)	$2.30[1.10, 4.81]$	$0.65[0.52, 0.79]$	$2.5[2.2, 3.0]$	$1.03[1.00, 1.06]$
FXU designs (4)	$3.29[1.98, 5.47]$	$0.66[0.56, 0.77]$	$4.5[2.6, 7.7]$	$0.94[0.83, 1.05]$
IDU designs (18)	$37.9[15.01, 95.6]$	$0.21[0.07, 0.34]$	$2.6[1.2, 5.6]$	$1.02[0.91, 1.13]$
ISU designs (16)	$25.2[8.64, 73.4]$	$0.30[0.15, 0.45]$	$2.7[1.8, 4.1]$	$1.03[0.97, 1.09]$
LSU designs (32)	$5.27[2.10, 13.2]$	$0.51[0.38, 0.63]$	$1.7[1.4, 2.0]$	$1.08[1.05, 1.10]$

TABLE II

COMPARISON OF AVERAGE WIRELENGTH MEASUREMENTS (IN *gatepitches*) FOR THE FUNCTIONAL CIRCUITRY IN THE *POWER4 IFU* DESIGNS WITH ESTIMATES PROVIDED BY THE DAVIS MODEL. ERRORS ARE SHOWN IN %.

IFU		*Rent [14], [15]*		*Rent (this work)*	
Design	$L_a(f)$	$L_{avg}(p^f)$ *[range]*	$E(L_{avg}(p^f))$	$L_{avg}(p_R^f)$*[range]*	$E(L_{avg}(p_R^f))$
i1	3.2	$2.3[2.1, 2.5]$	-29	$2.5[2.5, 2.6]$	-21
i2	4.8	$2.9[2.5, 3.3]$	-40	$3.4[3.3, 3.5]$	-29
i3	3.8	$2.9[2.5, 3.4]$	-25	$3.4[3.3, 3.5]$	-11
i4	3.5	$2.9[2.5, 3.4]$	-17	$3.5[3.4, 3.6]$	-1
i5	3.3	$3.8[3.1, 4.8]$	17	$5.0[4.8, 5.2]$	52
i6	5.6	$4.0[3.2, 5.0]$	-29	$5.2[5.0, 5.4]$	-6
i7	4.8	$4.0[3.2, 5.1]$	-17	$5.3[5.1, 5.5]$	9
i8	3.5	$4.1[3.2, 5.2]$	17	$5.4[5.2, 5.6]$	55
i9	4.3	$4.1[3.3, 5.2]$	-6	$5.4[5.1, 5.6]$	24
i10	3.1	$4.1[3.3, 5.3]$	34	$5.5[5.3, 5.8]$	79
i11	3.7	$4.2[3.3, 5.4]$	15	$5.6[5.4, 5.9]$	54
i12	8.7	$4.9[3.7, 6.6]$	-44	$6.9[6.5, 7.3]$	-21
i13	8.8	$5.0[3.7, 6.8]$	-44	$7.1[6.7, 7.5]$	-19
i14	6.5	$5.0[3.8, 6.9]$	-22	$7.3[6.9, 7.7]$	12
i15	7.6	$5.0[3.8, 6.9]$	-33	$7.2[6.9, 7.7]$	-4
i16	10.1	$5.2[3.8, 7.2]$	-49	$7.6[7.2, 8.0]$	-25
i17	7.8	$5.7[4.1, 8.3]$	-26	$8.7[8.2, 9.3]$	12
i18	8.9	$5.9[4.2, 8.5]$	-34	$9.0[8.4, 9.6]$	1

TABLE III

COMPARISON OF TOTAL MEASURED WIRELENGTH (IN *gatepitches*) WITH ESTIMATES PROVIDED BY THE DAVIS MODEL FOR FUNCTIONAL CIRCUITRY IN THE *POWER4* CHIP. THE ERRORS (IN %) ARE $E^f = E(L_{tot}(p^f))$ AND $E_R^f = E(L_{tot}(p_R^f))$.

Unit (#)	*Data*	*Davis estimate with* $\{p^f, k^f\}$ *[15]*		*Davis estimate with* $\{p_R^f, k_R^f\}$	
	$L_T(f)$	$L_{tot}(p^f)$*[range]*	E^f	$L_{tot}(p_R^f)$*[range]*	E_R^f
IFU (18)	200164.4	$137568.6[102738.8, 189032.2]$	-31	$198264.0[187512.2, 209624.0]$	1
FPU (12)	21805.1	$11731.6[10109.1, 13826.8]$	-46	$18848.4[18161.7, 19557.9]$	16
FXU (4)	24634.4	$10991.4[9222.6, 13301.7]$	-55	$18626.0[14960.6, 23103.4]$	32
IDU (18)	140842.3	$52723.0[47032.1, 60832.6]$	-63	$188789.8[152420.7, 231605.0]$	-25
ISU (16)	286661.6	$87765.5[74735.9, 108056.5]$	-69	$350055.3[308689.3, 395308.6]$	-18
LSU (32)	502571.6	$228186.2[186731.6, 289601.9]$	-55	$764213.6[720808.5, 809238.4]$	-34
POWER4	1176679.4	$528966.2[430570.1, 674651.8]$	-55	$1.54E6[1.40E6, 1.69E6]$	-23

TABLE IV

COMPARISON OF AVERAGE WIRELENGTH MEASUREMENTS (IN *gatepitches*) FOR *POWER4 FPU* DESIGNS (UPPER TABLE) AND *FXU* DESIGNS (LOWER TABLE) WITH ESTIMATES PROVIDED BY THE DAVIS MODEL. ERRORS ARE SHOWN IN %.

Unit		*Rent [14], [15]*		*Rent (this work)*	
FPU	L_a	$L_{avg}(p^f)$ *[range]*	$E(L_{avg}(p^f))$	$L_{avg}(p_R^f)$*[range]*	$E(L_{avg}(p_R^f))$
f1	3.3	$2.1[2.0, 2.3]$	-36	$2.6[2.5, 2.6]$	-21
f2	2.7	$2.1[2.0, 2.3]$	-22	$2.7[2.6, 2.7]$	-2
f3	4.5	$2.6[2.3, 2.9]$	-43	$3.7[3.6, 3.8]$	-19
f4	5.2	$2.8[2.5, 3.2]$	-46	$4.2[4.1, 4.3]$	-19
f5	4.0	$2.7[2.4, 3.1]$	-32	$4.0[3.9, 4.1]$	0
f6	4.7	$2.9[2.5, 3.3]$	-39	$4.4[4.3, 4.6]$	-6
f7	5.8	$2.9[2.6, 3.4]$	-50	$4.5[4.4, 4.7]$	-23
f8	5.3	$3.0[2.6, 3.5]$	-43	$4.8[4.6, 4.9]$	-10
f9	6.0	$3.1[2.7, 3.7]$	-48	$5.0[4.9, 5.2]$	-16
f10	7.1	$3.2[2.7, 3.8]$	-55	$5.2[5.0, 5.4]$	-26
f11	5.0	$3.3[2.8, 4.0]$	-34	$5.6[5.4, 5.8]$	12
f12	7.3	$3.4[2.8, 4.1]$	-54	$5.9[5.6, 6.1]$	-20
FXU	L_a	$L_{avg}(p^f)$ *[range]*	$E(L_{avg}(p^f))$	$L_{avg}(p_R^f)$*[range]*	$E(L_{avg}(p_R^f))$
x1	1.4	$1.5[1.4, 1.5]$	6	$1.5[1.5, 1.5]$	11
x2	3.5	$1.6[1.6, 1.7]$	-53	$1.8[1.7, 1.8]$	-50
x3	6.9	$3.0[2.7, 3.4]$	-57	$4.2[3.6, 4.8]$	-40
x4	9.7	$4.3[3.6, 5.3]$	-55	$7.5[6.0, 9.4]$	-22

TABLE V

COMPARISON OF AVERAGE WIRELENGTH MEASUREMENTS (IN *gatepitches*) FOR THE *POWER4 IDU* DESIGNS WITH ESTIMATES PROVIDED BY THE DAVIS MODEL. ERRORS ARE SHOWN IN %.

IDU		*Rent [14], [15]*		*Rent (this work)*	
Design	$L_a(f)$	$L_{avg}(p^f)$ *[range]*	$E(L_{avg}(p^f))$	$L_{avg}(p_R^f)$*[range]*	$E(L_{avg}(p_R^f))$
d1	2.8	1.8[1.7, 2.0]	−35	3.2[2.9, 3.5]	13
d2	4.4	2.0[1.8, 2.1]	−56	4.2[3.7, 4.7]	−7
d3	6.3	2.1[1.9, 2.3]	−68	5.3[4.5, 6.1]	−17
d4	5.8	2.1[1.9, 2.3]	−65	5.3[4.6, 6.2]	−9
d5	2.8	2.1[1.9, 2.3]	−25	5.5[4.7, 6.5]	101
d6	4.3	2.1[1.9, 2.4]	−51	5.9[5.0, 7.0]	37
d7	5.1	2.2[2.0, 2.6]	−58	6.4[7.2, 11.4]	26
d8	7.8	2.2[1.9, 2.5]	−72	7.3[6.0, 8.9]	−7
d9	7.2	2.2[2.0, 2.5]	−70	7.7[6.2, 9.4]	7
d10	5.2	2.2[2.0, 2.5]	−58	7.8[6.3, 9.6]	51
d11	6.8	2.2[2.0, 2.5]	−68	7.7[6.3, 9.4]	14
d12	5.5	2.2[2.0, 2.5]	−60	7.7[6.4, 9.7]	40
d13	5.9	2.2[2.0, 2.5]	−63	7.9[6.3, 9.4]	35
d14	5.2	2.2[2.0, 2.6]	−57	8.5[7.2, 11.4]	63
d15	6.5	2.2[2.0, 2.6]	−66	8.7[6.9, 10.7]	33
d16	5.8	2.3[2.0, 2.7]	−62	9.1[7.8, 12.7]	56
d17	5.5	2.1[1.9, 2.4]	−59	9.2[5.3, 7.6]	66
d18	5.5	2.2[2.0, 2.6]	−59	10.0[6.8, 10.5]	83

TABLE VI

COMPARISON OF AVERAGE WIRELENGTH MEASUREMENTS (IN *gatepitches*) FOR *POWER4 ISU* DESIGNS WITH ESTIMATES PROVIDED BY THE DAVIS MODEL. ERRORS ARE SHOWN IN %.

ISU		*Rent [14], [15]*		*Rent (this work)*	
Design	$L_a(f)$	$L_{avg}(p^f)$ *[range]*	$E(L_{avg}(p^f))$	$L_{avg}(p_R^f)$*[range]*	$E(L_{avg}(p_R^f))$
s1	3.7	$2.1[1.9, 2.4]$	-43	$4.5[4.2, 4.8]$	20
s2	5.8	$2.1[1.9, 2.4]$	-63	$4.6[4.3, 4.9]$	-20
s3	2.8	$2.1[1.9, 2.4]$	-24	$4.7[4.3, 5.0]$	65
s4	4.8	$2.3[2.0, 2.6]$	-53	$5.8[5.3, 6.3]$	19
s5	7.4	$2.3[2.0, 2.8]$	-69	$6.8[6.1, 7.4]$	-9
s6	6.1	$2.4[2.1, 2.8]$	-61	$7.4[6.7, 8.2]$	21
s7	6.5	$2.4[2.1, 2.8]$	-64	$7.2[6.5, 8.0]$	11
s8	5.5	$2.4[2.1, 2.9]$	-55	$8.2[7.4, 9.1]$	50
s9	7.9	$2.4[2.1, 2.9]$	-69	$8.3[7.5, 9.3]$	6
s10	7.1	$2.4[2.1, 3.0]$	-65	$8.4[7.5, 9.4]$	19
s11	6.6	$2.5[2.1, 3.0]$	-63	$9.2[8.2, 10.3]$	39
s12	7.6	$2.5[2.1, 3.1]$	-67	$9.4[8.3, 10.5]$	23
s13	8.6	$2.5[2.1, 3.1]$	-71	$10.3[9.1, 11.7]$	20
s14	4.1	$2.6[2.2, 3.2]$	-37	$11.3[9.9, 12.8]$	178
s15	10.9	$2.6[2.2, 3.2]$	-76	$11.2[9.8, 12.7]$	3
s16	12.4	$2.6[2.2, 3.4]$	-79	$13.4[11.6, 15.4]$	9

TABLE VII

COMPARISON OF AVERAGE WIRELENGTH MEASUREMENTS (IN *gatepitches*) FOR *POWER4 LSU* DESIGNS WITH ESTIMATES PROVIDED BY THE DAVIS MODEL. ERRORS ARE SHOWN IN %.

LSU		*Rent [14], [15]*		*Rent (this work)*	
Design	$L_a(f)$	$L_{avg}(p^f)$ *[range]*	$E(L_{avg}(p^f))$	$L_{avg}(p_R^f)$*[range]*	$E(L_{avg}(p_R^f))$
l1	2.7	$2.2[2.0, 2.4]$	-18	$3.4[3.3, 3.5]$	27
l2	7.4	$2.5[2.2, 2.8]$	-67	$4.4[4.3, 4.6]$	-40
l3	7.5	$2.5[2.2, 2.8]$	-67	$4.6[4.5, 4.8]$	-38
l4	5.8	$2.7[2.4, 3.1]$	-54	$5.6[5.4, 5.8]$	-4
l5	5.7	$2.7[2.4, 3.2]$	-52	$5.8[5.6, 6.1]$	3
l6	5.6	$2.8[2.4, 3.2]$	-51	$6.0[5.8, 6.3]$	7
l7	6.1	$2.8[2.5, 3.3]$	-53	$6.4[6.1, 6.6]$	5
l8	5.2	$3.0[2.5, 3.5]$	-43	$7.2[6.9, 7.5]$	40
l9	5.3	$3.0[2.5, 3.5]$	-44	$7.3[6.9, 7.6]$	37
l10	5.0	$3.0[2.6, 3.7]$	-39	$7.8[7.4, 8.2]$	57
l11	5.2	$3.1[2.6, 3.7]$	-41	$7.9[7.6, 8.3]$	52
l12	5.8	$3.1[2.6, 3.8]$	-46	$8.3[7.9, 8.7]$	44
l13	5.9	$3.1[2.6, 3.8]$	-46	$8.5[8.1, 9.0]$	46
l14	6.9	$3.2[2.7, 3.9]$	-54	$8.8[8.4, 9.2]$	27
l15	9.9	$3.2[2.7, 3.9]$	-68	$8.7[8.3, 9.2]$	-11
l16	6.5	$3.2[2.7, 3.9]$	-51	$9.1[8.6, 9.5]$	39
l17	9.4	$3.2[2.7, 3.9]$	-66	$9.0[8.5, 9.4]$	-5
l18	9.9	$3.2[2.7, 4.0]$	-67	$9.3[8.9, 9.8]$	-6
l19	8.9	$3.2[2.7, 4.0]$	-64	$9.3[8.8, 9.7]$	4
l20	4.6	$3.3[2.7, 4.1]$	-28	$9.8[9.3, 10.3]$	114
l21	8.1	$3.3[2.7, 4.1]$	-60	$9.8[9.3, 10.4]$	21
l22	10.7	$3.3[2.7, 4.1]$	-69	$10.0[9.5, 10.5]$	-7
l23	5.3	$3.3[2.7, 4.1]$	-37	$10.1[9.5, 10.6]$	91
l24	7.7	$3.3[2.7, 4.1]$	-57	$10.1[9.6, 10.7]$	31
l25	6.9	$3.3[2.8, 4.2]$	-52	$10.4[9.9, 11.0]$	51
l26	7.3	$3.5[2.8, 4.4]$	-52	$11.8[11.1, 12.5]$	63
l27	8.4	$3.5[2.8, 4.5]$	-59	$12.0[11.3, 12.7]$	42
l28	8.9	$3.5[2.8, 4.5]$	-60	$12.4[11.7, 13.2]$	40
l29	11.1	$3.5[2.9, 4.6]$	-69	$11.9[11.2, 12.6]$	7
l30	7.4	$3.6[2.9, 4.6]$	-52	$12.9[12.1, 13.7]$	74

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