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Superior Electrical Properties of High Performance Glass Ceramic Packaging for Demanding SiGe, ASIC, Microprocessor and Advanced Server Applications

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Abstract

IBM's High Performance Glass Ceramic (HPGC) LTCC modules are used in a wide range of SiGe, ASIC, microprocessor and advanced server applications in SCM and MCM configurations. Electrical test structures are designed and electrically modeled to provide guidance for producing parts on high volume manufacturing tools. Substrates are characterized at frequencies from DC to 40 GHz in microstrip and stripline environments for single ended and differential transmission line elements. Test structures include High Speed Serial link core compatible designs, controlled impedance via (CIV) structures, and designs to minimize line-via signal impedance / mode transition discontinuities. Material properties thermal solutions are characterized to simulate high power application environments. The beneficial attributes of designs with various transmission line structures are described, as are the advantages derived from uniformly thick, symmetric, reproducible, and smooth surface copper conductors for signal routing and shielding planes.

This work reflects the use of both IBM produced and non-IBM electrical modeling tools. These tools include ANSOFT HFSS, HSpice and IBM tools such as CZ2D and EMITPKG. It will be shown how the suite of tools has been used to optimize design structures for optimum electrical performance of glass ceramic packaging for low and high speed applications. Correlation of design models to finished product are demonstrated with electrical measurement data obtained with both time-domain and frequency-domain techniques.

Introduction

High Performance Glass Ceramic packaging materials were selected many years ago as the foundation for IBM's high-end server packaging. The basic ceramic formulation provides a thermal coefficient of expansion (TCE) match to silicon-based semiconductor devices while providing low dielectric constant and loss factor using high purity, essentially alkali-free raw materials. Adequate strength for surface treatments such as lapping and polishing, as well as the ability to withstand tensile and flexural loads during lid attach and engagement in pin grid array and land grid array (LGA) sockets, was derived from the crystallization of the single component glass into a predominantly ceramic phase. Copper metallization was chosen to provide the highest electrical conductivity possible while minimizing the overall processing temperatures to below 1000 ^{o}C [1, 2].

The initial use of glass ceramic packaging involved the deposition of sequential thin film surface wiring to produce mechanically tolerant pin attach metallization on the second level interconnect side. This involved a lapping and planarization process to produce a defect-free surface for spin-on dielectric layer application that was subsequently patterned to present brazeable I/O pads to support a pin grid array.

Current HPGC technology employs unique metal features to allow reliable direct solder attach of solder balls, solder columns and copper columns for second level attach to cards. For large multichip modules (MCMs), including server processor modules up to 95 mm square, LGA pads with thick gold are used. For top surface component joins, internal metallization transition features were introduced to allow reliable, direct solder joining of flip chip devices as well as surface mount passives such as IDC capacitors, TSSOP, and other large pad joining configurations. These features were used in the design of the packages discussed in this paper. The samples were built in IBM's manufacturing facility in East Fishkill, NY using production tooling .

Test Vehicle Description

IBM's HPGC wiring groundrules allow routine wiring to a 200 um pitch using signal line widths from 55 to over 125 um. These are patterned using thick film, extrusion screening techniques that deposit high aspect ratio lines which provide high wiring density and considerably greater current carrying capacity than traditional silk screening line deposition techniques. Examples of screened features are shown in Figures 1, 3a & 3b.

HPGC materials properties are compared to IBM's traditional 92% alumina HTCC ceramic in Table 1.

Material Properties	IBM Glass Ceramic	IBM Alumina
Dielectric Constant	5.4 (Cordierite GC)	9.5
Conductor Resistivity (uohm-cm)	2.2 (Copper)	10.0 (Molybdenum)
Thermal Coefficient of Expansion (ppm/$_{o}$C)	3.0	6.5
Shrinkage Tolerance	+/- 0.10	+/- 0.35
Camber/Flatness, typ. (um/cm)	<7.5	<30
Flexural Strength (MPa)	210	350

Table 1.

Automatic inspection techniques verify feature spacing and via integrity ensuring reliable manufacturing yields.

Metallized layers are collated, aligned and laminated using elevated temperature and uniaxial pressure. After sintering all surface features are plated with electroless NiP and Au. Where LGA contacts are used thick Au is also electroless plated, typically on just the bottom I/O pads.

Design Process Methodology

An integral part of executing HPGC designs is the design flow and verification process. The HPGC design process is shown in Figure 1 below. The process begins with a package netlist with the chip I/O identified by pad name and x-y coordinates. The board I/O is identified by net name and x-y coordinates. The package cross section is then planned based on chip power and redistribution requirements to accommodate the fan-out to the board. This is accomplished using Cadence Allegro APD and other supported file formats. The design is chiefly driven by the electrical specification requirements of the critical net I/Os. This function relies on modeling and simulation software to ensure that the electrical requirements will be met. This will be described in greater detail later in the paper. When the package is first manufactured, initial part performance is measured and analyzed in the laboratory to ensure compliance with all required performance specifications.

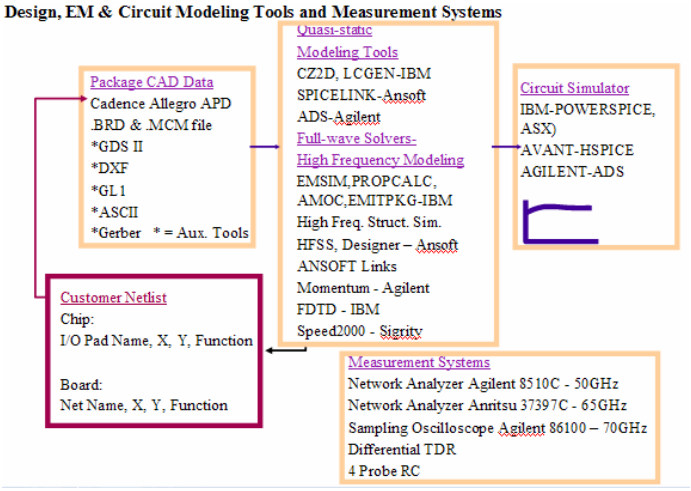

Figure 1

Signal Integrity on Glass-Ceramic Wiring

MCM technology has been in use in IBM from the 1980s, but the HPGC packaging material set offers substantially better electrical characteristics than traditionally used alumina packages. The high-end IBM Servers have used glass-ceramic MCMs with close to 100 layers [3] and greater than 4000 LGA contacts to printed-circuit boards. These modules offer high wiring and power densities and therefore high performance. In addition, most ceramics, unlike printed-circuit board materials, have been shown to have very low dielectric loss, tanδ. This results in low overall wiring loss and thus lower risetime dispersion as explained in [4]. Typical MCMs today [3] can sustain 100-200 ps risetimes, especially on the topmost layers and thus very high data-rates and throughput. Typical IBM Servers could have more than 20 processor chips connected with more than 11,000 I/Os (>100K solder-ball contacts) with an aggregate throughput of > 5.5 Tbps or >35 Gbps/cm^2. The better TCE match to silicon devices and tighter via grids than for printed-circuit boards provide a much better solution at the system level. Wiring lengths between chips are in the range of 8-12 cm and thus have higher bandwidth than board interconnects.

The practical limitations of high speed interconnects are introduced by the large layer stack that results in via length in excess of 1 cm. Most ground planes are hollow meshes allowing punched conductive vias to connect between dielectric layers. Signal integrity is mostly affected by the distortions caused by coarse-featured and long via stacks, orthogonal wiring, non-ideal shielding of the mesh planes, resistive losses in the wiring, and noise-induced distortion due to crosstalk between signal layers and via columns. These are features to be avoided in HPGC designs. Redistribution wiring layers are used to translate from the tight chip I/O connections to the less dense wiring pitch in the package and the fan-out line characteristics are difficult to control for >1000 signal connections on each chip. When the on-module data-rates start to exceed 3-5 Gbps, all the losses, reflections, and noise sources need to be well understood and considered in the design of high-performance applications.

Time-Domain Characterization and Correlation Simulation

Low-Frequency Measurements

The electrical properties of both the signal lines and the glass-ceramic insulator were analyzed on a specially designed test vehicle that had single lines very close to the top surface of a large 95-mm module. The test vehicle was designed to have representative product-level geometries and wiring configurations. The signal lines had reference mesh planes on a 200-µm pitch above and below and a very tight ground via array around the signal test pads as shown in Fig.2

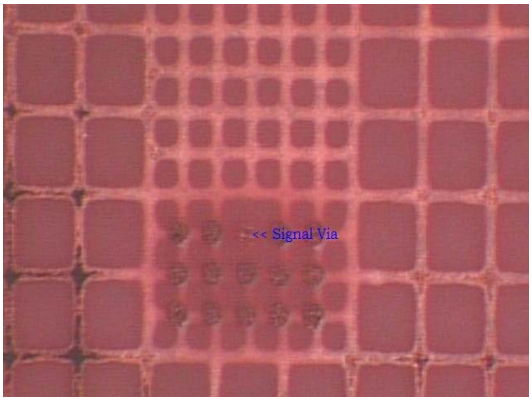

Fig. 2 Top-view of signal and ground test pads and mesh ground plane.

Line lengths ranging from 0.02 to 10.28 cm were included and after measurements were taken, very detailed cross sectioning for dimensional characterization was made both across the lines and along the lines. Typical mesh and line cross-sections are shown in Fig. 3.

Fig. 3a

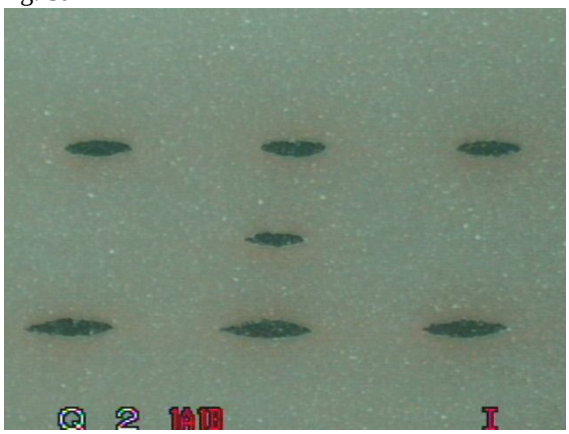

Fig. 3b

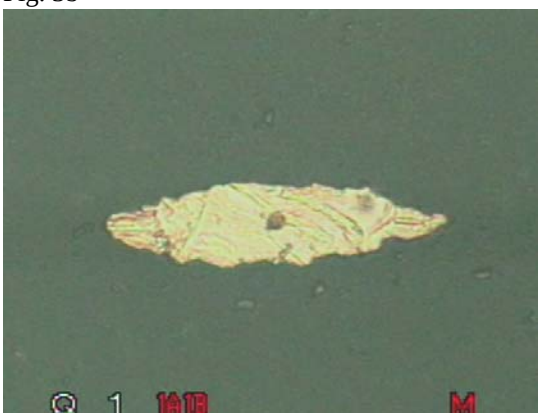

Fig. 3 a) Cross section of single-line site on layer six with mesh ground planes on layer five and seven. b) Closer view of the elliptical shape of the signal line.

The full characterization involves four-point resistance measurement, capacitance measurement using a low-frequency (1MHz) LCR meter, and time-domain measurement using the Agilent 86100 70GHz sampling oscilloscope. A set of lines is selected that have the same impedance and uniform cross section along the length. This screening is performed by using the 35-ps-risetime step excitation from the sampling oscilloscope and monitoring the TDR (time-domain-reflection) traces as shown in Fig. 4.

This is especially important given the elliptical cross sections shown in Fig. 3 with very irregular ridges. The per-unit-length resistance (*R)* and capacitance *(C)* are obtained by taking the difference in measured results and dividing by the difference in length. This technique eliminates the parasitic effect of vias, test pads and probes. Using the available cross sectional dimensions and measured *R* and *C*, the copper paste resistivity and dielectric constant at 1MHz are obtained. Copper paste resistivity was found to be $\rho = 2.2\ \mu\Omega$–cm. The four-point line resistance measurement was also made over the temperature range -150^0C to $+75^0$C. It was found that the temperature coefficient of resistance was $0.36\%/^0$C which is somewhat higher than anticipated for bulk copper (around $0.31\%/^0$C). The room-temperature line resistance was measured to be *R* = 0.29 Ω/cm. The 1MHz line capacitance measurement was also repeated over the same temperature range and it was found that the temperature variation of the glass-ceramic dielectric constant was extremely low, namely $0.01\%/^0$C. The dielectric constant was obtained by performing modeling of the line capacitance using the CZ2D and EMITPKG tools. The measured and calculated line capacitance values were 1.572 pF/cm and 1.573 pF/cm, respectively, for a dielectric constant of 5.4 at 1MHz. The difference is only 0.07%.

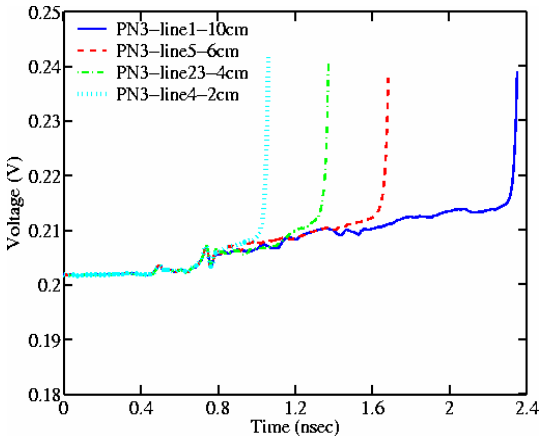

Fig. 4 TDR response on 2.016-cm, 4.012-cm, 6.008-cm, and 10.28-cm long single lines of the type shown in Fig. 3.

Modeling Methodology

The modeling involves the use of two IBM developed tools: CZ2D [5-6], a highly accurate, 2D, quasi-static code that captures the physically correct frequency dependencies between both *C* and *G*, and between *L* and *R*; and EMITPKG, an extraction tool that captures the 3D parametric effects caused by the mesh planes, crossing lines, and vias, but can also provide the per-unit-length *R*, *L*, *C*, and *G*. The transmission line parameters are taken from the 2D analysis, but corrected for 3D effects through the application of the extraction technique on the actual structure and a 2D companion structure.

The CZ2D code consists of a capacitance calculation routine based on the moment-method formulation described by Weeks [5], an inductance calculation routine based on another moment method formulation described by Weeks et al. [6], and a preprocessing routine that performs preliminary gridding to prepare the structure for subsequent analysis. The capacitance algorithm has been modified to include non-rectangular shapes, to include finite dielectrics through a novel technique based on boundary element and finite principles [7], and a powerful gridding algorithm that accounts for proximity and end effects. The inductance algorithm has also been modified to include non-rectangular shapes and a powerful gridding facility that accounts for proximity-, edge-, and skin-effects. The CZ2D program handles the loss tangent versus frequency for each dielectric in the structure through interpolation, and use of an analytic function with self-consistent real and imaginary parts, thus modeling the frequency dependent complex permittivity with real and imaginary parts that are related by a Hilbert transform. This

complex permittivity is then used to calculate frequency dependent conductance, $G_{CZ2D}(f)$, and capacitance, $C_{CZ2D}(f)$. The $L_{CZ2D}(f)$ and $R_{CZ2D}(f)$ are modeled in standard fashion by using the CZ2D moment-method code that effectively generates and solves a parallel network of inductances and resistances. By using the same sub-sectional grid at all frequencies, the parameters generated are calculated, in effect, by the same *L-R* network and so must be both physically consistent and causally related.

EMITPKG uses a full-wave analysis technique [8] to calculate the *Y* parameters seen between two appropriately chosen reference planes, and from the *Y* parameters, the *RLCG* parameters per-unit-length are obtained. The procedure involves setting up a signal-line structure that is driven by sources at sufficiently far distances from the port planes that their effect on the field between the port planes is negligible. Because the calculation of *Y* parameters involves voltages and currents on the port planes [9], the effects of the regions outside the port planes are removed. Thus, EMITPKG provides a powerful and unique method to extract the parameters of structures that resemble 2D uniform transmission lines but also include 3D effects (which precludes analysis by 2D analysis techniques). EMITPKG is run at a single appropriate frequency, f_0, on the actual 3D structure and on a companion structure obtained by removing all those conductors that give rise to 3D effects. The same sub-sectional grid is used for both structures to remove any grid-based errors; a correction factor is thus generated as a ratio between these two EMITPKG results on 3D and 2D structures. Because the same correction factor is subtracted at all frequencies, the derivatives of all the parameters against frequency remain the same, and thus the final parameters retain all their consistent and causal relationships. Fig. 5 shows a typical EMITPKG model and the elliptical shapes used in CZ2D.

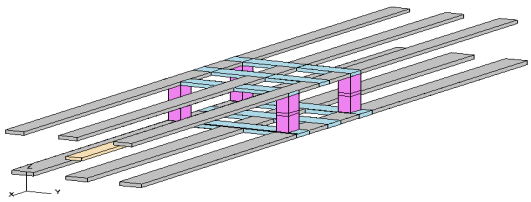

Fig. 5a

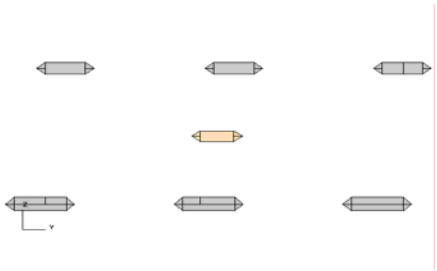

Fig. 5b

Fig. 5 a) Modeled 3D structure in EMITPKG and b) 2D modeling with CZ2D.

Resistivity calculated from DC measurement was used in the model.

Short-Pulse Propagation Measurement

The total loss and characteristic impedance of the lines were measured with a very simple time-domain technique. It employs a short, electrical pulse that is launched onto a transmission-line structure. The pulse is obtained by differentiating the step-source of the sampling oscilloscope using a passive impulse-forming network, 5206-205 manufactured by Picosecond Pulse Labs. In addition, the source risetime is improved by the use of the Picosecond Pulse Labs 4022 TDR/TDT source and 4020 pulse enhancer. The propagated pulse is recorded with the 70-GHz detector of the 86118A module of the Agilent oscilloscope. High-speed coaxial probes in ground-signal (GS) configuration (GGB Industries model 40-A-250LP) were used to connect to the transmission lines. The short pulse is launched on two identical lines with lengths l_1 and l_2 and digitized by the detector. Time windowing is performed on theses pulses in order to eliminate any unwanted reflections from probes, pads, vias, and cable connectors. Since amplitude resolution is more essential than spectral resolution for time-domain measurements, rectangular windowing is used with a smooth transition to the signal baseline steady-state level. These processed waveforms are Fourier transformed, and the ratio of the complex spectra yields the propagation constant

$$\Gamma(f) = \alpha(f) + j\beta(f) = \frac{1}{l_1 - l_2}\ln\frac{A_1(f)}{A_2(f)} + j\frac{\Phi_1(f) - \Phi_2(f)}{l_1 - l_2} \qquad (1)$$

where $\alpha(f)$ and $\beta(f)$ are the frequency-dependent attenuation coefficient and phase constant, respectively. $A_i(f)$ and $\Phi_i(f)$ (i=1,2) are the amplitude and phase of the transforms corresponding to lines of lengths l_1 and l_2, respectively, with $l_1 > l_2$. No de-embedding or calibration is required since the effects of interface discontinuities simply cancel out or are eliminated by the windowing process. This is why this technique is much simpler than network-analyzer based frequency-domain methodologies. The characteristic impedance can be obtained from

$$Z_0(\omega) = \Gamma(\omega) / [\, G(\omega) + j\omega C(\omega)] \qquad (2)$$

The implicit assumption is that the measured transmission lines of lengths l_1 and l_2 have very similar characteristics and are uniform over the entire length since this extraction obtains effective per-unit-length (p.u.l.) parameters. This is why it is important to perform the screening shown in Fig. 3. Based on the cross-sectional dimensions and copper resistivity, the p.u.l. $R(\omega)$ and $L(\omega)$ were also calculated using CZ2D and EMITPKG. An initial set of values was assumed for the loss tangent of the dielectric, $\tan\delta = \varepsilon_r'' / \varepsilon_r'$ along with the real ε_r' value measured at 1MHz of 5.4. An analytic function based on the Debye model for the complex permittivity [10] was used to interpolate between the specified $\tan\delta$ points.

$$\varepsilon(\omega) = \varepsilon_\infty + \sum_i \frac{\varepsilon_i}{1 + j\omega\tau_i} \qquad (3)$$

This interpolating function consists of a finite series of rational terms with self-consistent real and imaginary parts, with coefficients chosen to fit the measured total loss behavior over the desired frequency range [8]. Once an initial dielectric fit is obtained, the total measured and calculated attenuation are compared and parameters of the expansion (ε_∞, ε_i, τ_i) are adjusted to improve the fit. Two sets of short-pulse measurements were needed, namely with l_1 = 4.012 cm and l_2 = 1.008 cm, and with l_1 = 10.28 cm and l_2 = 2.016 cm. The spectral content of the two sets were 5.2 GHz – 37 GHz and 2.6 GHz - 5.3 GHz, respectively. Comparison of these two sets of data allowed us to compensate for inaccuracies caused by the imperfect cancellation of the effects of interface discontinuities when taking the ratio of the two Fourier transforms for the lines l_1 and l_2. The calculated $C(\omega)$ and $G(\omega)$ were also used to extract the frequency dependence shown in Fig. 5. Here $\varepsilon_r'(\omega) = C(\omega)/C_{1MHz}$ x 5.4 and $\tan\delta(\omega) = G(\omega)/\omega C(\omega)$. This allowed the extraction of $\varepsilon_r'(\omega)$ and tanδ(ω) over the frequency range 10 KHz to 50 GHz. The high frequency range was extrapolated from 37 GHz to 50 GHz based on the behavior predicted by equation (3). Fig. 7 shows the measured and calculated total attenuation.

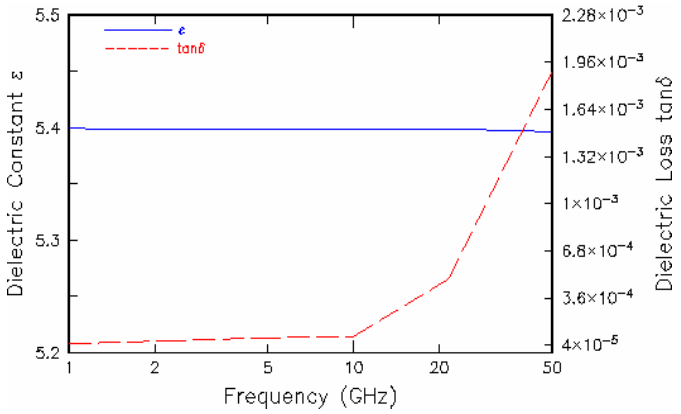

Fig. 6 Extracted dielectric constant and dielectric loss variation with frequency for glass-ceramic material.

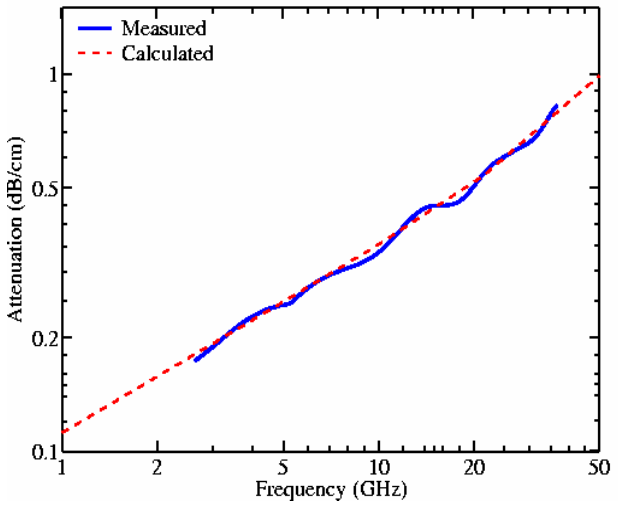

Fig. 7 Measured and calculated attenuation using the short-pulse propagation technique with 1.008-cm, 2.016-cm, 4.012-cm, and 10.28-cm long lines.

Frequency Domain Measurements

In order to compare the time domain and frequency domain measurements, a set of lines with different length (10.08 mm, 40.118 mm, 60.077 mm) were measured with a VNA Anritsu 37397 in the frequency range from 40 MHz to 65 GHz. The measurement setup was calibrated using the multi-line TRL calibration method as proposed by the National Institute for Standards and Technology (NIST) [11-14].

A set of reference lines on a special semi insulating GaAs (ε_r = 13) substrate, developed by NIST, was used for the first tier calibration. After the calibration, the reference planes of the measurements were moved into the contact points of the microwave probes. In order to determine the propagation constant, a second set of transmission lines was measured on the lines of Fig. 3 embedded in the regular power and ground mesh structure of the test vehicle. In principle two lines with different length would be enough to determine the propagation constant, but the multi-line TRL method improves the accuracy of the calculated propagation constant in special frequency ranges by measuring more than two lines (multiple lines). It was found that the very short lines (200 μm to 5 mm) did not improve the accuracy of the results as expected for higher frequencies. It is believed that this was due to the large, 200 μm pitch of the power and ground mesh. Therefore, the 10.08 mm long line was chosen for the shortest, the so called "thru" line.

The results for the attenuation and the phase constant are shown in Figs. 8 and 9 respectively and compared to results obtained from time-domain measurements as described in the previous section. Both the attenuation and especially the phase constant show a fairly good agreement for the extracted frequency range.

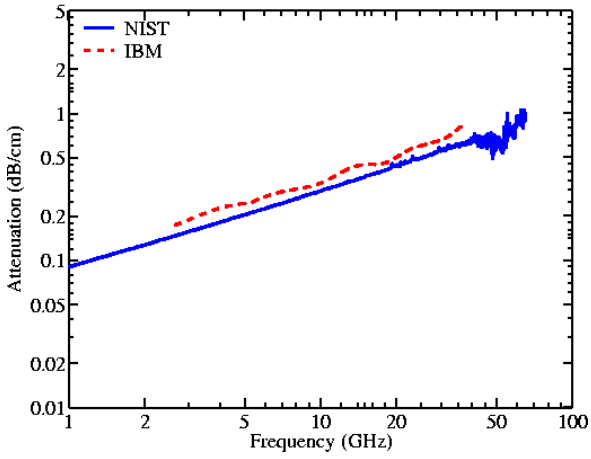

Fig. 8 Attenuation measured with the short-pulse propagation time-domain (dashed) and frequency-domain multi-TRL (solid) techniques.

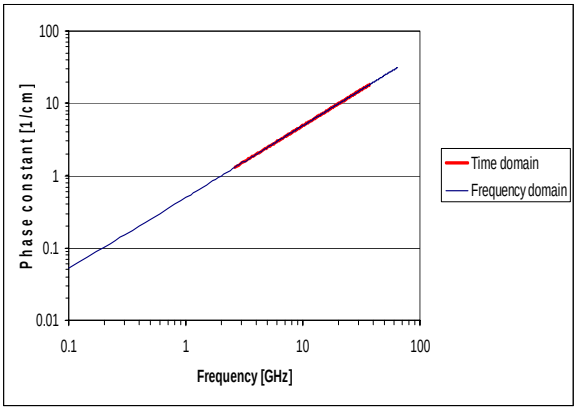

Fig. 9 Phase constant measured with the short-pulse propagation time-domain (red) and frequency-domain multi-line-TRL (blue) techniques.

Signal Propagation and Crosstalk Measurements

Validation of the extracted material parameters was made by comparing the simulated and measured TDT (time-domain-transmission) and TDR waveforms. The TDR traces were used to define an equivalent model for the test pads, probes, and via discontinuities and a typical response is shown in Fig. 9

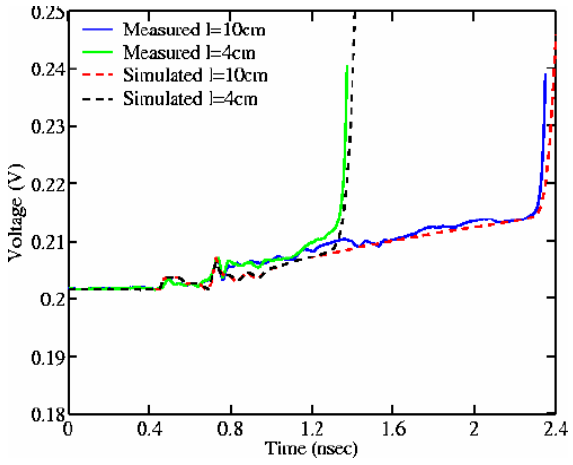

Fig. 9 Measured and simulated TDR response for 4.012-cm and 10.28-cm long lines of the type shown in Fig. 3

A 35-ps-risetime step excitation having 202.3mV amplitude was also launched through the coaxial probes and the propagated delay, risetime dispersion, and reflection signals were measured. The 86118A 70GHz detector provides a 70 Ω termination and the signal is detected across a 55.5 Ω termination. This is why there are various steps seen in the TDT signals shown in Fig. 9.

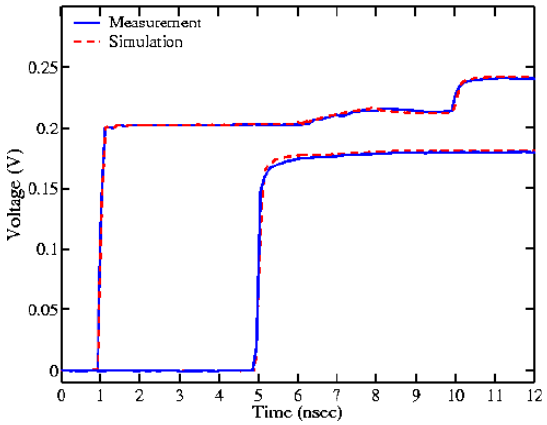

Fig. 10 Measured and simulated propagated step response for the 10.28-cm long lines of the type shown in Fig. 2.

Comparison of measured and simulated time-domain waveforms provides direct physical interpretation of the key transmission-line properties and verifies and validates the modeling technique. Fig. 11 shows the measurement set-up. TDT measurements are generally performed on several lengths of lines with an initial response taken on a 0.02016-cm lengths. The use of such a short line provides the needed reference for the longer lines to subtract the delay in the connecting cables and probes. The use of several lengths of lines is needed for both high-speed signal propagation and capacitance measurements. The propagated signal on the 0.02016cm line had 40.8 ps risetime and 186.7 mV amplitude. TABLE I shows the correlation for the 4.012 cm and 10.28 cm lines for the lines of Fig. 2. The agreement is considered quite good.

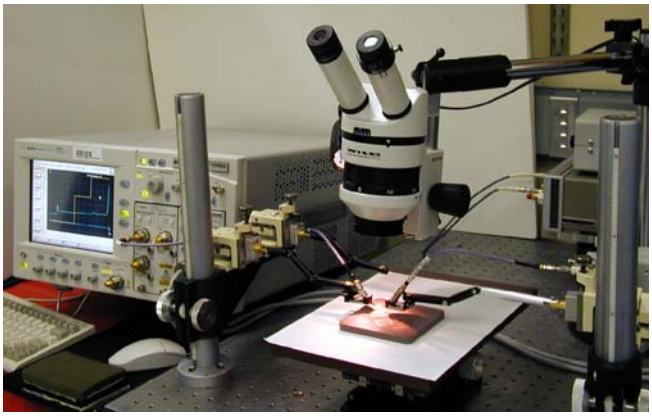

Fig. 11 Test measurement set-up showing the coaxial probes and cables connecting the test multi-chip module to the sampling oscilloscope.

TABLE II
Measured and Simulated Signal Propagation Results

	l = 4.012 cm		
	Voltage (mV)	Delay (ps)	Risetime (ps)
Measured	185.0	323.2	160.3
Simulated	185.2	324.8	177.0
Delta (%)	+0.1	+0.5	+10.4
	l = 10.28 cm		
	Voltage (mV)	Delay (ps)	Risetime (ps)
Measured	182.0	815.9	218.0
Simulated	181.8	823.5	240.0
Delta (%)	-0.1	+0.9	+10.0

Modeling Issues

It can be noted in Fig. 5 that the extracted tanδ for glass ceramic is quite low below 21.544 GHz (0.000098 at 10 GHz). Even at 21.544 GHz it is only 0.000488 while at 50 GHz it jumps to 0.00189. An investigation was made to assess whether the generated models omitted effects that were included in the total attenuation measured in Fig. 7. First, a model was built for the lines of Fig. 3 with a complete shielding box around it and no difference in the results was found when compared to the case without the shield. It was concluded that the structure was not radiating. The lines were modeled as equivalent rectangles, as ellipses similar to the ones in Fig. 3b, and as ellipses with ridges as shown in Fig.12. Fig. 13 shows that the difference between the three cases is quite small. Both the elliptical shape and the ridges contribute to a slight increase in attenuation but could not account for the sharp increase in attenuation above 21.544GHz as the tanδ value suggests in Fig.5. It was found that the difference between EMITPKG_2D and EMITPKG_3D results is less than 5% up to 50 GHz. There was also very good agreement between CZ2D and EMITPKG_2D which gave confidence in the methodology. In the range 50-70 GHz the difference in predicted loss between 2D and 3D modeling increases up to 23% while at 100 GHz there is a big jump. The height of the cross-section for the single line shown in Fig. 8 was 198 μm which approaches λ/15 for $\varepsilon_{r'}$ = 1 at 100 GHz (λ = 3mm). This means that the quasi-TEM assumption in the modeling could start to break down at 100 GHz and some components of the electric field could develop along the direction of propagation. The extrapolated tanδ values shown in Fig. 6 extended only to 50 GHz where the difference between 2D and 3D modeling was still less than 2%. Based on these results, it is believed that the extracted abrupt rise in tanδ above 21.544GHz is real and reflects the real properties of the glass-ceramic material.

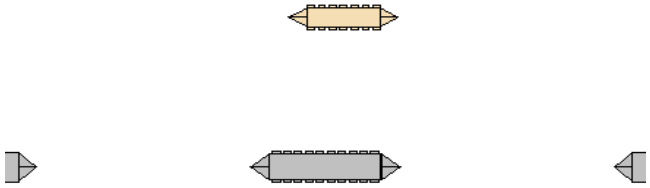

Fig. 12 Portion of model with elliptical shape and ridges shown on the signal line and the bottom mesh ground conductor.

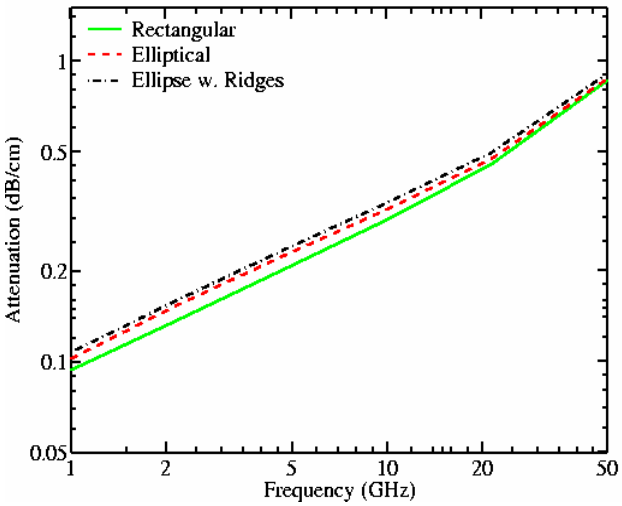

Fig. 13 Calculated attenuation with rectangular, elliptical, and elliptical with ridges (as shown in Fig. 12) cross section for the single lines of Fig. 3.

In the range 50-70 GHz the difference in predicted loss between 2D and 3D modeling increases up to 23% while at 100 GHz there is a big jump. The height of the cross-section for the single line shown in Fig. 9 was 198 μm which approaches λ/15 for $\varepsilon_{r'}$ = 1 at 100 GHz (λ = 3mm). This means that the quasi-TEM assumption in the modeling could start to break down at 100 GHz and some components of the electric field could develop along the direction of propagation.

Premium Performance Differential Transmission Line Structures in IBM HPGC

The discussion thus far has addressed primarily single ended stripline structures. As serial data rates exceed 4 Gbps and extend beyond 10Gbps it is clearly indicated that differential transmission structures are preferred over the single ended

forms. There are two prime factors driving the use of differential transmission and they are improved cross-talk and noise immunity. Similarly to the single ended stripline structure shown in Figure 5a the differential analog of this is shown in fig. 14.

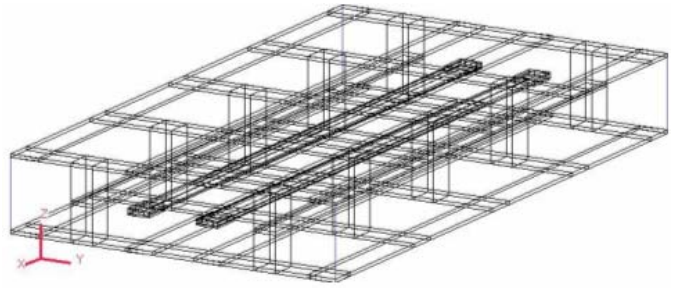

Fig. 14 Differential Triplate (Stripline) Shielded Structure for High Speed Serial Link Applications.

For a packaging application designed as a 32mm x 32mm Crosspoint switch operating at 12.5Gbps, the impedance design target for the high speed nets was 100Ω differential and 50Ω single ended. An IBM patented insertion loss reduction technique [15] is used in this example to minimize the losses due to conductor surface roughness and dielectric loss tangent and circuit path routing. The flip chip package design redistribution layer technique is shown in Fig. 15.

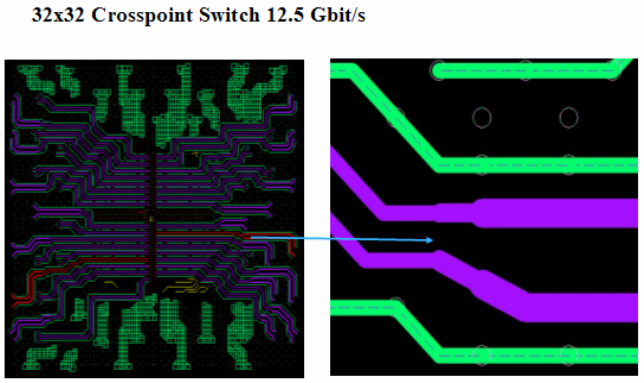

Fig. 15 3D Flare Net Structure design technique for reduced insertion loss at high gigabit data rates

The R2 distribution layer is shown on the left and the flare technique detail is shown on the right side of Fig. 15. The impedance is held constant by using thicker dielectric layering while adjusting the line width to form a broader conduction plane with significantly lower loss per unit length than the standard differential net geometry. The TDR data are shown in fig. 16 of a typical net the lower (green) trace is calibrated to 50Ω and the upper (blue) trace is calibrated to 100 Ω. The bumps on the beginning of the trace indicate the discontinuity of the BGA ball and the upward trace indicates the open circuit of the chip site on the substrate. We observed the impedance control using this technique to be very effective while reducing package transmission losses at high serial data rates.

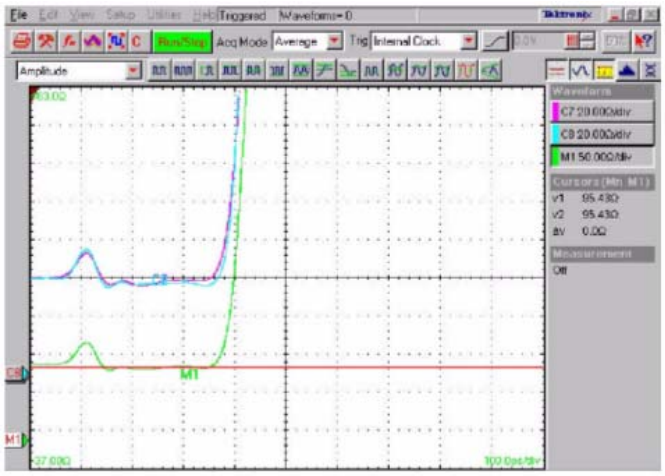

Fig. 16 TDR Plots of Single ended net (Green) and Differential net Blue

HPGC High Frequency Stripline Differential Pair Design and Analysis

CZ2D is used to determine frequency-dependent transmission line parameters such as inductance, capacitance, and impedance for general 2D cross-sections. AMOC is a scripting tool that calls IBM developed tools such as CZ2D in textual rather than graphical form, and simplifies multiple iterations. Combinations of line width, line spacing, layer thickness, via size and via pitch from AMOC iterations of CZ2D are used to determine the best structure for a 100 Ω differential wiring/net pair. The transmission line parameters are used in HSPICE to simulate return loss and coupling. Structure selections are then refined to meet return loss specifications and reduce spurious noise coupling.

With the right structures chosen based on modeling and specifications, the dimensions for via size, line width, and spacing are then implemented in the physical design using tools such as Cadence APD and/or Allegro.

Once the design is complete, the electrical performance of the lines as specifically designed in the package can be simulated. The Ansoft toolset is used to perform the high frequency 3D analysis for verification. ANSOFT LINKS serves as a bridge between the Ansoft GUI environment and design tools like Cadence. Signal lines and the corresponding power structures are extracted directly from the design file and imported into Ansoft.

There, the imported structure is set up for a high frequency analysis with Ansoft HFSS. HFSS calculates impedance, return loss, insertion loss, and coupling. It then creates data tables and plots the data versus frequency. ANSOFT DESIGNER combines Touchstone data results from separate HFSS simulations and performs time-domain analysis

An example of this analysis is shown in Figure 17 a and b using the HPGC package described above. The line pair is separated into two structures because of computational memory

and simulation speed limitations. The combined HFSS analysis results show an insertion loss of -2dB at 15.7 GHz and a return loss of -10 dB at 10.8 GHz in Fig 18.

C4 side

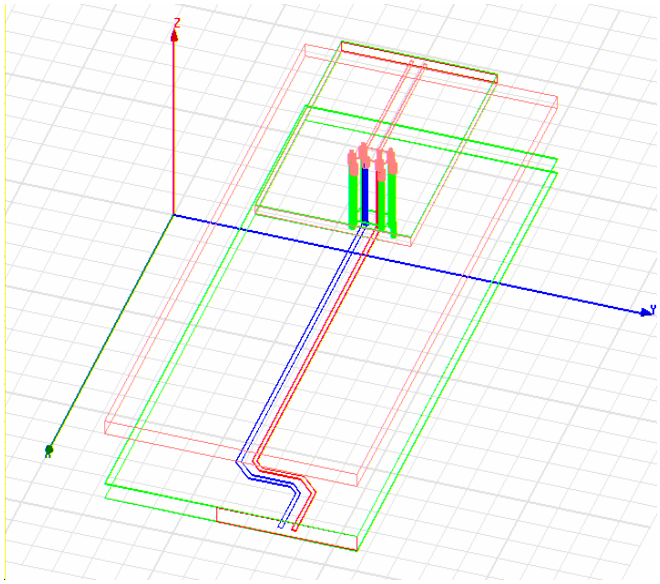

Fig. 17a

BGA Side

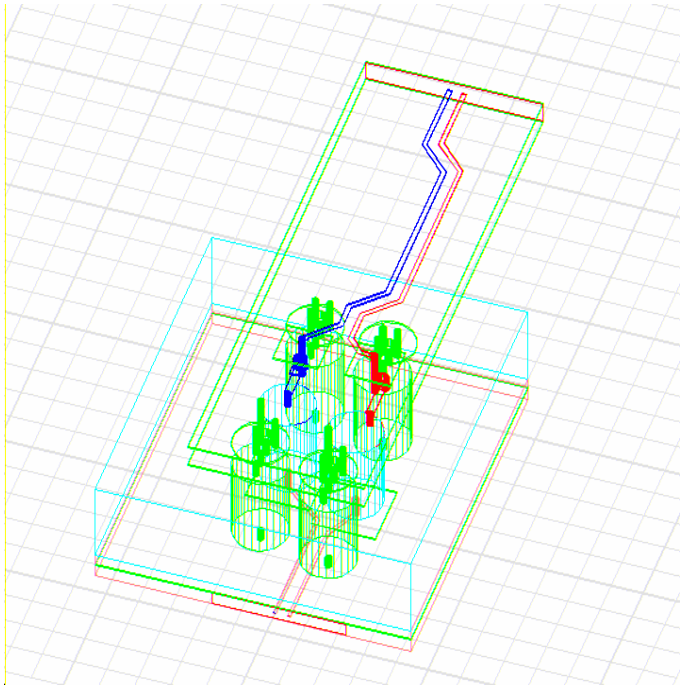

Figure 17 b

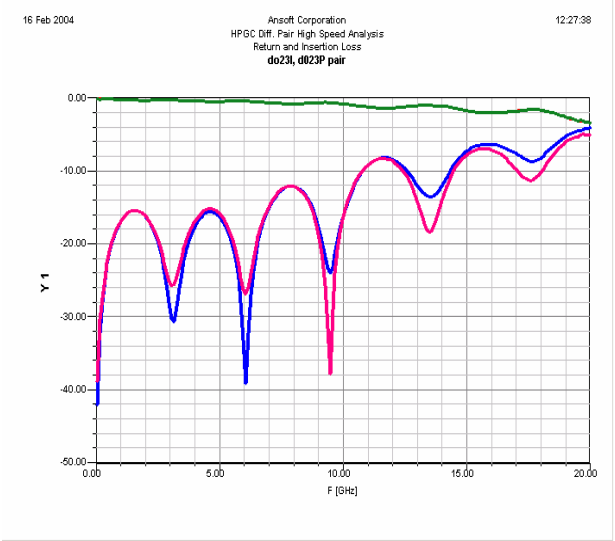

Fig. 18 The Return and Insertion Loss of the 2 HFSS Models Shown in Figs. 17a & b integrated into a single and complete signal path

Conclusions

In this paper, the characteristics of the HPGC glass-ceramic are highlighted.

HPGC's predictable planarity, very close TCE match to Silicon and mechanical strength makes it an ideal platform for current and future ultralow-K SCM and MCM applications. HPGC's electrical properties indicate that it can support serial data rates significantly exceeding 12.5 Gbps using the appropriate transmission line structure designs.

In addition, broadband dielectric constant and dielectric loss were extracted for the first time over the range 10 KHz to 50 GHz in representative multi-layer structures. The extraction was performed using a very simple time-domain technique unlike the general practice in the industry of frequency-domain extraction. The technique used allowed the generation of fully-causal transmission line models up to 50 GHz. This accurate and wide bandwidth model generation is essential to optimize the design of ceramic SCM and MCM chip carriers with multi-gigabit data-rate requirements.

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