RC23536 (W0502-129) February 24, 2005
Materials Science

IBM Research Report

Dislocation-Free Strained Silicon-on-Silicon by In-Place Bonding

G. M. Cohen, P. M. Mooney*, V. K. Paruchuri, H. J. Hovel
IBM Research Division
Thomas J. Watson Research Center
P.O. Box 218
Yorktown Heights, NY 10598

*Curently at Simon Fraser University, Burnaby, BC, Canada V5A 1S6

Research Division
Almaden - Austin - Beijing - Haifa - India - T. J. Watson - Tokyo - Zurich

Dislocation-free strained silicon-on-silicon by in-place bonding

G.M. Cohen, P.M. Mooney*, V.K. Paruchuri, and H.J. Hovel

IBM Semiconductor Research and Development Center (SRDC)

Research Division, T. J. Watson Research Center, Yorktown Heights, NY 10598 USA

Abstract

In-place bonding is a technique where silicon-on-insulator (SOI) slabs are bonded by hydrophobic attraction to the underlying silicon substrate when the buried oxide is undercut in dilute HF. The bonding between the exposed surfaces of the SOI slab and the substrate propagates simultaneously with the buried oxide etching. As a result the slabs maintain their registration and are referred to as "bonded in-place". We report the fabrication of dislocation-free strained silicon slabs from pseudomorphic tri-layer Si/SiGe/SOI by in-place bonding. Removal of the buried oxide allows the compressively strained SiGe film to relax elastically and induce tensile strain in the top and bottom silicon films. The slabs remain bonded to the substrate by van der Waals forces when the wafer is dried. Subsequent annealing forms a covalent bond such that when the upper Si and the SiGe layer are removed, the bonded silicon slab remains strained.

* Present address: Physics Department, Simon Fraser University, Burnaby, BC CANADA V5A 1S6

The performance of metal-oxide semiconductor field effect transistors (MOSFETs) in complementary metal-oxide-semiconductor (CMOS) technology is enhanced by the use of strained Si. Blanket Si layers under biaxial tensile strain are typically achieved by means of a strain-relaxed epitaxial SiGe layer grown on a Si(001) wafer as a "virtual substrate", on which an epitaxial strained silicon layer is subsequently grown [1]. When a SiGe layer underneath the strained Si film is undesirable, the relaxed-SiGe/strained-Si structures are further processed to fabricate strained-silicon-on-insulator (SSOI) [2] and strained-silicon-on-silicon (SSOS) [3] wafers by layer transfer and wafer bonding methods. This approach has several drawbacks: First, it requires the epitaxial growth of a relatively thick SiGe layer. Second, plastic strain relaxation of the SiGe film is achieved through nucleation and glide of 60^{o} misfit dislocations that results in a crosshatched rough surface. Chemical mechanical polishing (CMP) is typically done on the strain-relaxed SiGe layer prior to the growth of the strained silicon layer to reduce the surface roughness to a level suitable for device fabrication. CMP is also required to enable the fabrication of SSOI and SSOS by wafer bonding. Finally, the threading dislocation density in the strained Si layer is the same as that in the original underlying strain-relaxed SiGe layer.

Here we report the fabrication of dislocation-free strained silicon slabs on silicon by a new technique we call in-place bonding. We describe the principles of the in-place bonding technique and show how it can be applied to fabricate strained-silicon-on-silicon (SSOS).

Fig. 1 shows the main process steps of the in-place bonding method applied to a pseudomorphic tri-layer Si/SiGe/Si film stack. The Si/SiGe/Si film stack was fabricated by epitaxial growth of a 250 nm-thick metastable pseudomorphic compressively strained $Si_{0.8}Ge_{0.2}$ layer on a 20 nm-thick SOI film, followed by a 20 nm-thick epitaxial silicon cap layer. The SOI substrate was a commercially bonded wafer having a 145 nm-thick buried oxide, with the bonding interface being the oxide-substrate interface. The Si/SiGe/Si film was patterned into isolated slabs by conventional lithography and reactive ion etching (RIE) using HBr chemistry (Fig. 1(a)). The buried oxide layer was then undercut by etching in a 10:1 diluted hydrofluoric (HF) acid (Figs. 1(b)). As discussed later, the etching of the buried oxide allows the SiGe film to relax elastically and to induce tensile strain in the silicon films. The free-standing Si surface and the Si substrate surface are both hydrophobic and are therefore attracted to each other in the etchant bath. After sufficient etching the free-standing silicon surface is pulled to the substrate surface by hydrophobic attraction and bonds to the substrate surface (Fig. 1(c)). As additional oxide is removed, further bonding takes place between the slab and the substrate. The process terminates when all the buried oxide is removed and the slab lies flat on the substrate (Fig. 1d). When the substrate is dried as it is removed from the etching bath, the slabs remain bonded to the substrate by van der Waals forces. A covalent bond forms between the substrate and the bottom strained Si layer during subsequent annealing at 800°C for 3 hours in a N_2 ambient [4]. Thus, when the upper Si and SiGe films were removed, the remaining bonded Si layer (Fig. 1(e)) is firmly attached to the Si substrate. Removal of the upper Si and SiGe films was carried out in two steps. First the top silicon film was removed selectively with respect to the SiGe layer by etching with

tetramethylammonium hydroxide (TMAH) 25 wt. % at room temperature. Then the SiGe film was removed selectively with respect to the bottom strained-silicon layer by etching in a bath of aged 1 HF:2 H_2O_2:3 CH_3COOH solution.

Fig. 2(a) is an SEM image showing an array of in-place bonded Si/SiGe/Si slabs. This sample had not been annealed so the slabs are bonded to the substrate only by van der Waals forces. The SEM sample was prepared by cleaving a bar from a wafer. Slabs at the edge of the sample are not cleaved due to the weak bonding provided by the van der Walls force. They either overhang the edge or remain attached to the other part of the wafer. Subsequent annealing at 800 ^{o}C forms a covalent bond between the slabs and the substrate and in this is case the slabs are cleaved along with the substrate.

The bonded area of Si/SiGe/Si slabs with a partially etched buried oxide detached from the substrate when the wafer was dried, forming flat slabs supported by an oxide pedestal [5]. This suggests that the elastic restoring force of the slabs is sufficient to overcome the weak van der Waals bonding force in air but not the stronger attractive force between the slab and the substrate in the etching bath. In comparison, the edge of partially etched *thinner* 55 nm-thick Si slabs remained bonded to the substrate, as shown by Fig 2(b) and was illustrated in Fig. 1(c). To verify that the stronger attraction in the HF bath is due to hydrophobic forces we rendered the silicon surface more hydrophilic by adding a surfactant, sodium dodecyl sulfate, to the etching bath [6]. Silicon slabs that were undercut in an HF bath that contained the surfactant did not bond to the substrate but rather floated in the bath, with a few randomly deposited on the substrate.

The registration of the in-place bonded slabs with respect to their initial position as defined by lithography was tested. The gate line mask of a 90 nm CMOS process mask set was aligned to in-place bonded slabs that were defined by the shallow trench isolation (STI) mask. Overlay was measured with the Biorad Q7 tester using a box in a box test structure. The measured overlay error, less than 30 nm, was the same for wafers having in-place bonded slabs and for control wafers where the slabs were defined by RIE but the buried oxide layer was not removed. Excellent registration is maintained provided the slab edges bond to the substrate while the rest of the slab is still held in place by unetched buried oxide.

As has been previously demonstrated [5], elastic (dislocation-free) strain relaxation of the free-standing portion of the symmetric Si/SiGe/Si layer occurs as the buried oxide is etched away. The compressive strain in the SiGe layer is reduced and because no defects are introduced, the lattice mismatch strain between the SiGe and the Si is accommodated by inducing tensile strain in the upper and lower Si layers. The degree of strain transfer between the SiGe film and the top and bottom silicon films depends on the ratio of their thicknesses. To maximize the strain transfer from the SiGe film to the silicon films, the thickness of the SiGe film must be much greater than the total thickness of the Si films. For the structure employed in this work, the ratio was about 6:1. The strain in the bonded Si/SiGe/Si slabs was measured by x-ray diffraction measurements as described previously [7]. Fig. 3 shows the triple-axis diffraction map of an array of in-place bonded Si/SiGe/Si slabs. The offset in ω between the diffraction peaks from the SiGe and Si layers in the slabs and the Si substrate, is due to a slight misalignment

between the (001) lattice planes of the substrate and those of the bonded slabs [8]. This misalignment was present in the bonded SOI wafer on which the SiGe/Si films were epitaxially grown. The shift in the Bragg angle of the SiGe layer compared with the Bragg angle of the initial pseudomorphic SiGe film, indicates that the strain is reduced by 83%, in good agreement with a force balance model [7]. The diffraction peak corresponding to the Si layer has a higher Bragg angle than that of the Si substrate peak, indicating that the Si layers are under tensile strain with ε=0.0069. The appearance of pronounced thickness fringes in the diffraction map indicates that the strain relaxation of the slab was indeed elastic, i.e. without the introduction of defects.

Surface roughness was measured with a Digital Instruments Dimension 5000 Scanning Probe Microscope (AFM) using tapping mode. Elastic strain relaxation of the Si/SiGe/Si slabs was confirmed by the smooth (crosshatch free) surface measured by AFM. For comparison, we also imaged slabs for which the buried oxide layer was not etched but were also annealed at 800°C. As expected, these partially relaxed slabs exhibited a crosshatch pattern of surface steps formed by the glide of 60^{o} misfit dislocations during annealing [9].

Fig. 4 shows an AFM image of an in-place bonded 8.5×8.5 μm^2 slab following the 800°C anneal and removal of the top Si/SiGe layers (Fig.1(e)). The strained silicon surface is flat and smooth with a root mean square (RMS) roughness of 0.16 nm. The RMS surface roughness of the surrounding silicon substrate is 0.46 nm, because the wet

etching process is the major contributor to the roughness and the substrate was exposed to both the Si and SiGe etching solutions.

Raman spectroscopy measurements were used to measure strain in the bottom Si slab after removal of the upper Si and SiGe layers, and following an additional high-temperature anneal which simulated a dopant activation anneal that is routinely used in CMOS device fabrication. The dopant activation anneal was carried out by a rapid thermal anneal (RTA) peaking at 1000°C for 5 seconds, with a ramp rate of 50 ^{o}C/s in N_2 ambient. Raman spectroscopy measurements show that the 20 nm-thick Si layer remains strained after removal of the relaxed SiGe layer which originally induced the strain in the Si layer. This confirms that the slab-substrate bond is strong enough to maintain the strain after the 800°C anneal. The strain in the Si slabs was maintained after RTA anneal. Since the dopant activation anneal is typically the highest thermal treatment applied to a wafer during CMOS fabrication, the technique outlined in this paper can be used to fabricate strained silicon MOSFET devices.

The physics and chemistry of the in-place bonding technique requires further investigation. It is not clear why the etching of the buried oxide does not stop, or at least slow down, once the edges of the slab bond to the substrate and presumably stop the supply of fresh HF. During etching of the buried oxide, the bonded edges of the slabs must be able to slide, since the slabs are flat once all the oxide has been removed. This suggests that the bond between the slab and the substrate is weak enough to allow slippage of the slab and may also enable the transport of the etching solution. Questions about the nature of this bond and the magnitude of the various forces involved remain.

In conclusion we have fabricated dislocation-free strained-silicon-on-silicon by in-place bonding. In this method small Si slabs are bonded to a Si substrate in a liquid solution, whereas the usual wafer bonding is performed in air or in vacuum. The in-place bonding method vertically translates Si/SiGe/Si-on-insulator slabs onto the underlying substrate while preserving their registration. Since the slabs are released from the buried oxide, the Si/SiGe/Si structure relaxes elastically without introducing defects into the bonded strained Si layer. After annealing, the top Si and SiGe layers are removed by etching, and the covalently bonded bottom Si layer remains strained. The strained silicon slabs are flat and exhibit a smooth surface. The nature of the bonding forces was discussed briefly but further work is needed to address many remaining questions.

The epitaxial layer structures for this work were provided by H. Chen, IBM Microelectronics Division, Hopewell Junction, NY 12533 USA

References:

1. P.M. Mooney, International Journal of High Speed Electronics and Systems **12**, 305 (2002), and references therein.

2. K. Rim, K. Chan, L. Shi, D. Boyd, J. Ott, N. Klymko, F. Cardone, L. Tai, S. Koester, M. Cobb, D. Canaperi, B. To, E. Duch, I. Babich, R. Carruthers, P. Saunders. G. Walker, Y. Zhang, M. Steen and M. Ieong, IEDM Technical Digest, 49 (2003).

3. D.M. Isaacson, G. Taraschi, A.J. Pitera, N. Ariel, E.A. Fitzgerald, and T.A. Langdo, Adv. Mater. Micro- and Nano-Sys., online publication link: http://hdl.handle.net/1721.1/7373 (2005).

4. Q.-Y.Tong and U. Gosele, *Semiconductor Wafer Bonding*, (Wiley Interscience, New York, 1999) Ch. 5.

5. P.M. Mooney, G.M. Cohen, H. Chen, J.O. Chu and N. Klymko, Mat. Res. Soc. Symp. Proc. **809**, 27 (2004).

6. J. Israelachvili, *Intermolecular Surface Forces*, 2nd Ed., (Academic Press, New York, 1992) Ch. 16.

7. P.M. Mooney, G.M. Cohen, J.O. Chu and C.E. Murray, Appl. Phys. Lett. **84**, 1093 (2004).

8. G.M. Cohen. P.M. Mooney, E.C. Jones, K.K. Chan, P.M. Solomon and H-S. P. Wong, Appl. Phys. Lett. **75**, 787 (1999).

9. J. Cai, P. M. Mooney, S. H. Christiansen, H. Chen, J. O. Chu and J. A. Ott, J. Appl. Phys. **95**, 5347 (2004).

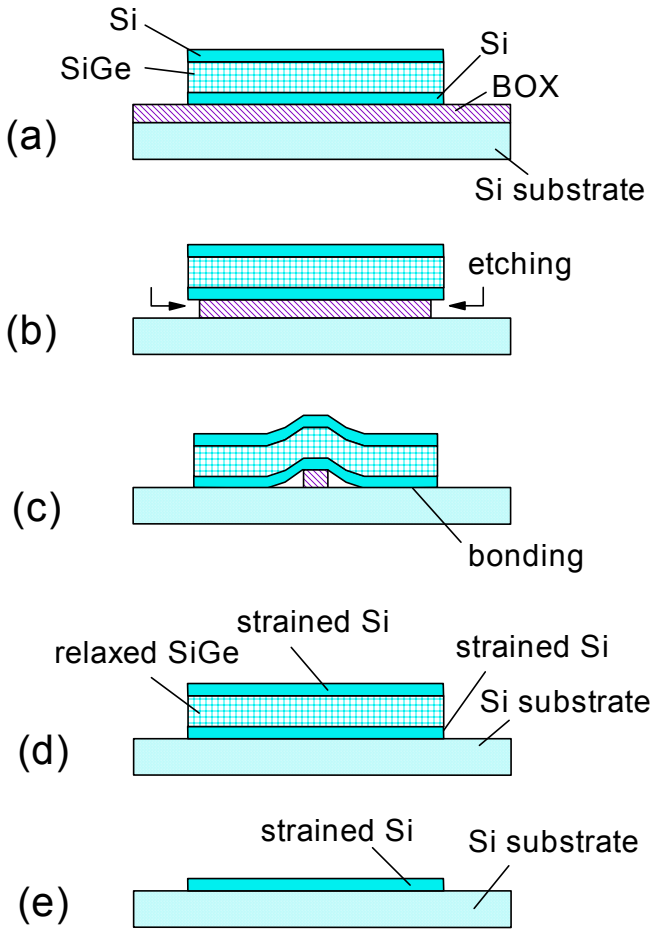

Fig. 1. Schematic diagram illustrating the in-place bonding method with tri-layer Si/SiGe/Si slabs.

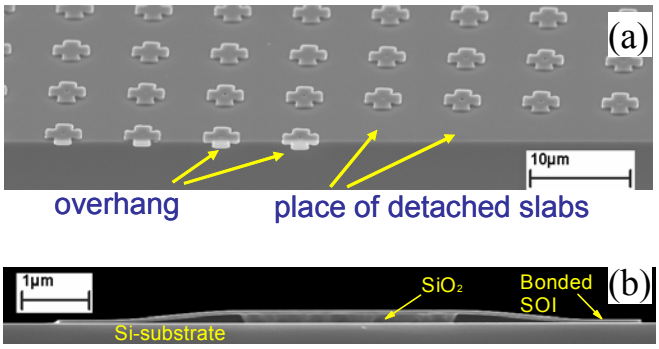

Fig. 2 SEM images showing (a) an array of in-place bonded slabs and (b) a cross section of a partially bonded Si slab.

.

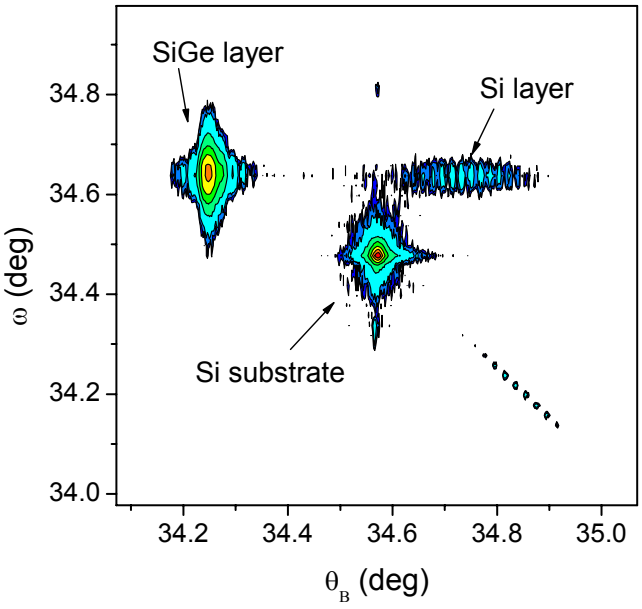

Fig. 3 High-resolution triple-axis x-ray diffraction map of bonded tri-layer Si/SiGe/Si slabs.

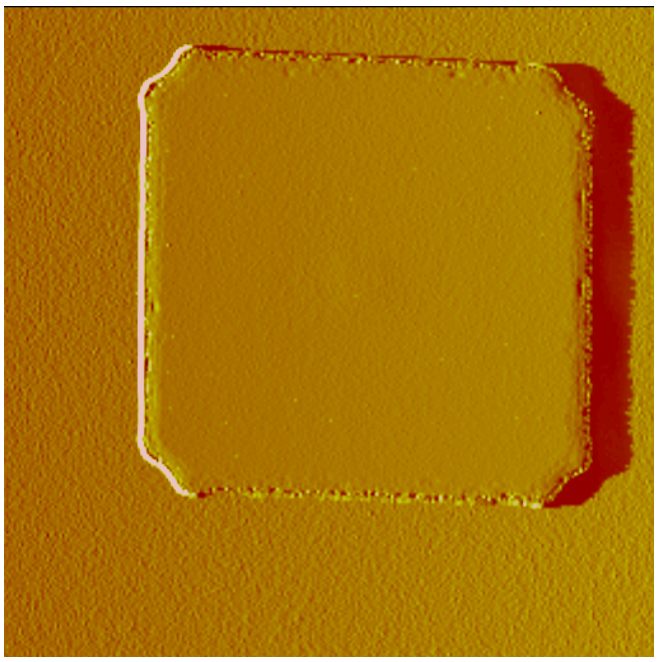

Fig. 4 Atomic force microscope image (amplitude) of a strained-Si-on-Si (SSOS) slab fabricated by in-place bonding. The slab size is 8.5×8.5 μm^2.