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MEMS FABRICATION FOR WIRELESS COMMUNICATIONS USING COPPER INTERCONNECT TECHNOLOGY

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ABSTRACT

Wireless communications technology is growing and becoming a key segment of the semiconductor industry. One potential technology advancement is the miniaturization and integration of the passive components that currently make up 70% of the components in a cell phone and contribute to 80% of their costs [1]. Some of these passive components include inductors, variable capacitors, resonators, filters and switches. Integrating some or all of these passives on a single chip promises to introduce new designs of the wireless transceiver with added functionality so that multiple bands, multiple protocols, and internet connection can be handled by a single wireless device. Additional perceived benefits of integration on a single chip are increased performance, lower power consumption, and lower cost. This paper reviews the application of electrochemical processing to the fabrication of miniaturized integrated passive and MEMS devices.

INTRODUCTION

Passive components currently make up approximately 70% of the components in a cell phone and as much as 80% of the cost [1]. It is well recognized that in most current transceiver architectures, it is these discrete, board-level connected devices that are the biggest limiters of advances in cellular phones and that a higher level of integration of these components would be desirable. Figure 1 shows a schematic of a typical super-heterodyne wireless transceiver with a number of components highlighted. Each of these components, which include resonators, filters, switches, and variable capacitors, could potentially be replaced by a MEMS passive device integrated on-chip [2]. Although reducing handset size is one potential benefit, a greater driver for this change is to increase the functionality within a given handset so that multiple bands and multiple protocols could be accommodated within a single handset. This would enable cell phones that truly function in a global environment.

A major thrust of university and industrial research in this area is investigating technologies that can integrate passive components on-chip [1]. It is believed that integration of miniaturized passives will improve performance since the signal doesn't need to be routed across the board. Other perceived enhancements are improved power consumption, better form factor and decreased cost. Cost seems to be one of the biggest drivers for this industry.

Microelectromechanical systems (MEMS) is a technology that holds the potential of integrating more sophisticated devices such as capacitive and resistive switches, variable

capacitors and resonators. Merging MEMS and ULSI fabrication technology [1, 3] could offer multiple devices at a fraction of the original cost. A common element of MEMS devices is the fact that each of these devices consists of a free standing beam or set of beams that is set in motion (actuated) with the use of a force. The most successful of these devices use electrostatic force to generate movement of a cantilever, fixed-fixed or free-free set of beams.

INTEGRATION

The level of integration that is *needed* drives the entire process for fabrication of such devices. For the purposes of this discussion, we will define 'integrated' components as those that need to 'talk' to one another or more accurately, disparate components between which signals must be routed. Currently, passive devices are primarily integrated at the board level today. A step higher in integration would be incorporating passive components in a package and this is done today in some instances. However, there is a great desire in the RF design community to integrate them directly on-chip since package-level integrated devices can still suffer from poor performance.

For on-chip integration, one can consider fabricating a passives 'chiplet' that can be either stacked or flip-chip bonded to the active IC. Alternatively, one can directly build the MEMS devices on the semiconductor wafer, which we will define as *monolithic* integration.

The ability to integrate different MEMS devices onto the same wafer is highly desirable since it could offer multiple devices at little additional cost. The fabrication of MEMS resonator–filter devices using Bi-CMOS compatible processes was reported previously [4]. That work used standard processes from interconnect technology to facilitate the introduction of MEMS devices into CMOS and Bi-CMOS IC manufacturing. The present work reports both switches and resonators produced on the same wafer using base copper interconnect processes demonstrating that different MEMS devices can fabricated is for the ground plane and is simply a patterned copper level imbedded in a dielectric made using a copper Damascene process flow.

Using copper-based processes to create free-standing MEMS devices does present several design challenges. Copper, unlike aluminum for example, easily oxidizes and must be encapsulated to prevent corrosion during many process steps. The resulting micromechanical beam tends to have a complicated multilayer cross-section and film stresses must be considered during fabrication to avoid overall compressive beam stress and severe stress gradients. Additionally, the resonator device performance is highly dependent on material properties such as a high Young's modulus, whereas the series switches are in need of a suitable contact material to ensure low insertion loss.

Cost considerations

Assuming that the performance differences for the two on-chip integration approaches are comparable, cost will then be the key driver to determine the preferred integration method. A cost analysis compares a stacked chip approach with monolithic integration [5]. The packaged stacked-chip cost estimation is based on a typical transceiver block

diagram in Figure 1. The cost per component for a typical board-level integrated system in use today is for a GSM phone. The active components can be satisfied with one power amplifier, two I/Q modulator/demodulators, and two PLL frequency synthesizers. These components may have more functions than what are needed for the active component coverage shown in the block diagram. These ICs, however, are the ones with cost information, which is why they are used. The effect of yield is calculated and compared to the estimated onboard cost and is shown for the stacked-chip and monolithic approaches. Profit margin is included. The relative cost of the on-chip integrated approaches as compared to the discrete approach. The standard board-level integrated (i.e. discrete passives + ICs) cost is set at 100%. The first thing that one can observe is that the discrete passives account for over 60% of the total cost for this transceiver configuration. At high yields, the monolithic and stacked-chip passives integration approaches have similar costs. The monolithic integration is very sensitive to the yield because of its cumulative nature. The IC and passives processes are distinct processes and therefore are to be considered as independent events, i.e. the yields multiply.

One therefore might conclude that in early manufacturing before the volumes have ramped, the stacked-chip approach might be preferable. This is reasonable since one is fabricating each chip (i.e. passives chiplet and active IC) independently and mating a lower yielding passives chiplet to a high yielding IC chip. This assumes that one can test the passives chiplet for yield before the stacking or flip-chip process. Monolithic integration is at a disadvantage in this case since one would be 'wasting' good IC chips that had poor yielding passives devices fabricated on them. Once full production (with yield learning) is achieved, the monolithic integration becomes more attractive and potentially preferable. As a result the best mode of integration will undoubtedly be linked to the volumes of passives being produced.

Integrated Inductors

The introduction of copper interconnect technology by IBM in 1997 [3, 6] prompted attempts to use copper plating in damascene lines to fabricate low resistivity copper inductors. However, full integration of inductors on chip in close proximity to the substrate result in losses which decreases the performance of the inductors. Placing inductors too close to a semiconducting substrate results in increased losses resulting from setting up eddy currents in the substrate. From this perspective while integration is good, integration too close to the substrate may be detrimental. It is an irony, that one of the drivers for improved CMOS performance (minimizing delays in the interconnect wiring) tends to shrink the thickness of interconnect metal-dielectric film stacks thereby *decreasing* the performance of on-chip inductors and other passives as well. Fabrication of these devices on GaAs substrates doesn't suffer from this problem since these substrates are insulating in nature. However, for technologies using more conventional conducting substrates, substrate losses can become a performance limiter.

In order to minimize capacitive losses, inductors are typically placed on the top of the interconnect metallurgy and above a ground plane in order to physically remove them from the substrate and isolate the electric field generated by the inductor from the lossy silicon substrate . Further improvements can be made by incorporating a 'dummy' layer of thick insulator between the interconnect and the inductor. Alternatively, one can

remove the substrate from underneath the area of the inductor by etching a cavity into the wafer.

Another loss mechanism for inductors are resistive losses. The inductor performance is typically improved if its coils consist of high conductivity copper metal with thickness between 20 μm and 30 μm. Figure 2 shows a 22μm thick copper inductor that we fabricated by electrodepostion through a thick photoresist mask with straight side walls. The improvement in inductor performance can be measured by the quality factor (Q) and thicker copper significantly improves the performance compared to more conventional devices. The quality factor of a 24 μm thick copper inductor is measured to be 40 at a frequency of 2.5GHz.

MEMS resonators/filters

A schematic for a MEMS resonator is shown in Figure 3. It consists of a free standing beam that is actuated by a lower metal electrode. A small DC voltage on the lower electrode displaces the upper beam by some finite amount. That DC signal is then modulated by an incoming RF signal. When the frequency of the RF signal matches the inherent resonant frequency of the free standing beam, resonance in the beam is induced and that resonance can be monitored at the output electrode. In this way, this device serves to filter out unwanted signals and pass only the frequency of interest to the output electrode.

For a resonator that vibrates at a high frequency (1-3GHz regime is typical for cellular phones), the material itself must be lightweight (low density) with a high Young's modulus and relatively small in size as show in Equation 1.

Fundamental resonant frequency = $f_0 = 1/2\pi * \text{sqrt}(k/m) = 1.03\kappa * \text{sqrt}(E/\rho) * t/L^2$ (1)

Where k = beam stiffness, m = beam mass, κ = scaling factor (surface topography effects), E = Young's modulus, ρ = density, t = beam thickness, and L = beam length. The equation is valid when the beam length is longer than the beam thickness ($L > 8t$), and the width of the beam is not disproportionate (i.e. it is not a plate). To maximize the beam frequency, the beam material must have a low density and a high Young's modulus.

Dimensions for resonator beams typically measure in the few micron range in width by tens of microns in length. The gap between the free standing beam and lower electrode is ideally kept small in order to help ensure that the actuation voltage is low [7], consistent with the specifications of a cellular handset and is typically on the order of a few microns to submicron. The beam must also have uniform stress across the beam thickness in order to ensure that the free standing beam doesn't bend. Finally the beam must be electrically conducting in order to be actuated electrostatically.

From a performance point of view, mechanical resonators have inherently very high quality factors (Q) due to the limited loses inherent in a mechanical device of this type. This is extremely desirable to meet filter performance specifications. More importantly, since these devices are small and can be integrated on-chip, given their high performance they can be combined in unique ways that fundamentally improve and simplify the

architecture of an RF front end. For example, it has been proposed [7] that an array of MEMS filters that are switched on and off by a bank of switches could be used to do channel select directly after the antenna greatly reducing the number of components in this design. This approach also eliminates the need for many of the other passive devices that are used in the typical superheterodyne architecture RF transceiver today.

MEMS Switches

MEMS switches are devices that use mechanical movement to achieve a short circuit or an open circuit in a radio frequency transmission line. The most successful of these devices have used electrostatic force to generate mechanical movement. Some electrostatically actuated switches have demonstrated exceedingly high reliability (100 million to 10 billion cycles) and wafer-scale fabrication techniques. The performance of MEMS switches when compared to p-i-n diodes and FET switches used in RF transceivers today is truly excellent. MEMS technology has enabled the fabrication of contact switches with very low losses of less than -0.5 dB up to 40 GHz. This loss corresponds to a contact resistance of less than a 1 ohm. In addition, because MEMS switches rely on the movement of a cantilever or fixed-fixed beam over an air gap, have a very low off-state capacitance resulting in a high isolation. Furthermore, electrostatically actuated MEMS switches have near zero power consumption because the mechanical beams utilize a DC voltage at extremely low currents to generate vertical or lateral movement of beams with respect to the underlying substrate electrodes [8].

A MEMS series switch fabricated with the copper Damascene method is shown in Figure 4. The switch is actuated by a lower electrode in order to pull the free standing beam down to touch a lower contact electrode through which the RF signal passes in the case of an ohmic metal contact or gets interrupted in the case of a contact using a dielectric material. The holes in the beam are needed to ensure clean removal of the sacrificial material underneath the beam that is utilized during the fabrication process. Metals are ideal materials from both an electrical conductivity point of view as well as its capability to effectively dissipate the generated heat at the contacts during passage of the RF signal. While a cross section of this switch looks similar to the resonators mentioned above, its characteristics are very different. The freestanding electrode must be much more electrically and thermally conducting than a resonator since it must pass a significant amount of power and dissipate a significant amount of heat generated. As a result, it is typically fabricated out of metal.

MEMS Fabrication

We have fabricated integrated resonators and switches (Figure 5) with the free standing electrode made of copper and silicon dioxide insulating material. Shown in Figures 5a and 5b are cross-section schematics and plan view optical photographs of the directly integrated MEMS switch device and resonator, respectively. The unique cross section is produced using Chemical Mechanical Polishing (CMP) to form almost all of the patterned layers shown. Additionally, to further improve the device performance, the design incorporates a ground plane (M1) that eliminates RF losses to the conductive substrate. In order to maximize the resonant frequency of the resonator, the M3 copper layer was removed or minimized within the micro-mechanical beam area.

The fabrication process we have used to build MEMS devices follows to a great extend the single level or Dual Damascene process flow schemes [3, 6, 9]. The first metal level fabricated is a ground plane and is connected to the first MEMS electrode level using a large via level. When fabricating MEMS switches, the first MEMS electrode level is an electroplated copper single Damascene capped with a dielectric material that has an electrode capped with the contact material. The electroplated copper metal due to its high conductivity allows passage of the radio frequency signal from the beam level to the lower electrodes with very small losses.

The contact level is also formed by a Damascene process, i.e. by blanket deposition and formation of the contact by CMP. Next, the organic sacrificial layer that defines the air gap of the MEMS device is deposited and planarized. The upper contact is formed next. The beam level and via level that connects the lower and upper MEMS device electrode are formed using a dual Damascene process. Interestingly, the MEMS device moving electrode is a composite beam composed by metal inlaid in dielectric. As a result, the beam fabrication and material set can be adjusted to fit the individual MEMS device requirements. For example, for the fabrication of RF resonators, a very stiff beam is required, and then the beam material is mainly dielectric. In the case of an RF MEMS switch, the beam material is either all metal or is a composite metal-dielectric with separate actuation and signal electrodes.

RESULTS AND DISCUSSION

All measurements were performed on-wafer, in vacuum for resonators or an ambient of nitrogen for switches, using microwave probes and an HP8753B network analyzer. The measured response of the cantilever beam resonator fabricated with tungsten electrodes (C1 and C2) is shown in Figure 6. The resonant frequency was measured to be 4.418 MHz at a bias of 2.0 V with a maximum Q of 1220. On the same wafer, the performance of the RF MEMS switches is shown in Figure 7(a). The actuation voltage for this switch device was 38 V and remained constant over 1×10^{7} switching cycles without failure. The high insertion loss of the switch device is attributed to the oxidation of the tungsten contacts during the oxygen-based release process. To improve the switch insertion loss, new devices were fabricated using an improved contact metallurgy for the contact electrodes (C1 and C2) able to withstand the aggressive oxidation step. Initial tests of switch devices fabricated with the improved contact metals are shown in Figure 7(b). The dramatic improvement in insertion loss, even without the lower ground plane (M1/V1), is evident when comparing Figures 7(a) and 7(b). The explanation may lie with the ease of oxidation of metals. Figure 8 shows the heat of formation of metal oxides for several refractory and noble metals [10]. The higher the tendency of the metal to form oxide, the worst the MEMS switch contact resistance will be. If the contact material is a refractory metal such as W, WN, Ta, TaN it results in a dielectric surface oxide such as WO_3 or Ta_2O_5 during the removal of the sacrificial layer. A change in capacitance between one (capacitance of air) and the dielectric constant of 10 or higher of the surface oxide yields a capacitive switch. To create an ohmic contact, a metal that does not readily oxidize is required [11,12]. A wide range of contacts have been evaluated. The development of MEMS fabrication technology offers new opportunities to develop novel electrochemical processes for electrolytic or electroless deposition and planarization (CMP) of contact materials compatible with copper interconnects.

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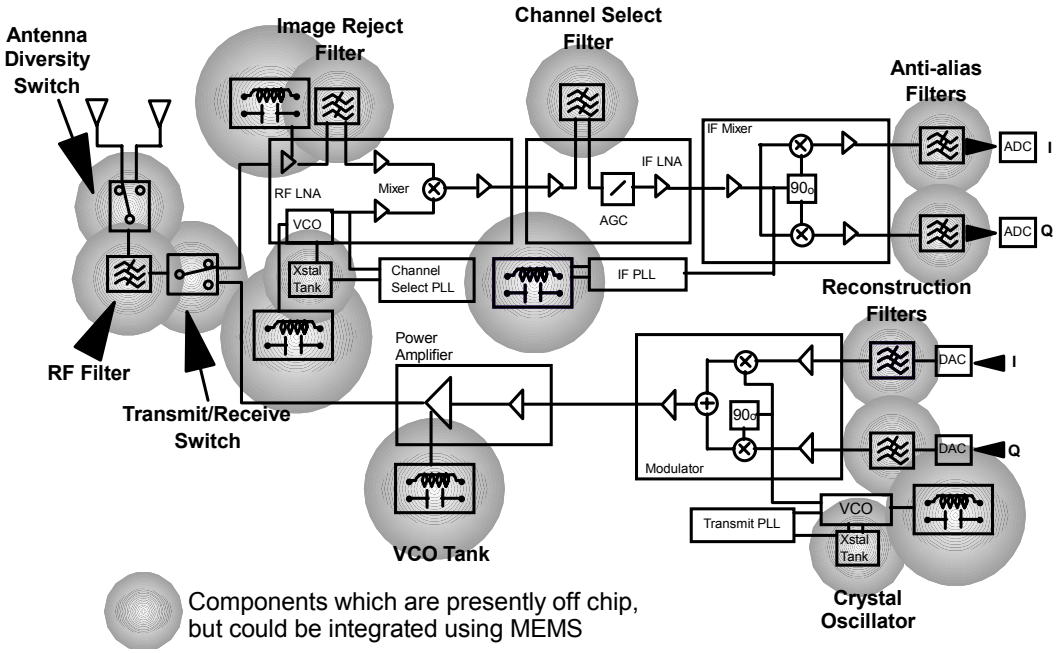


Figure 1. Block diagram of the front-end of a typical RF Tranceiver [1,2].

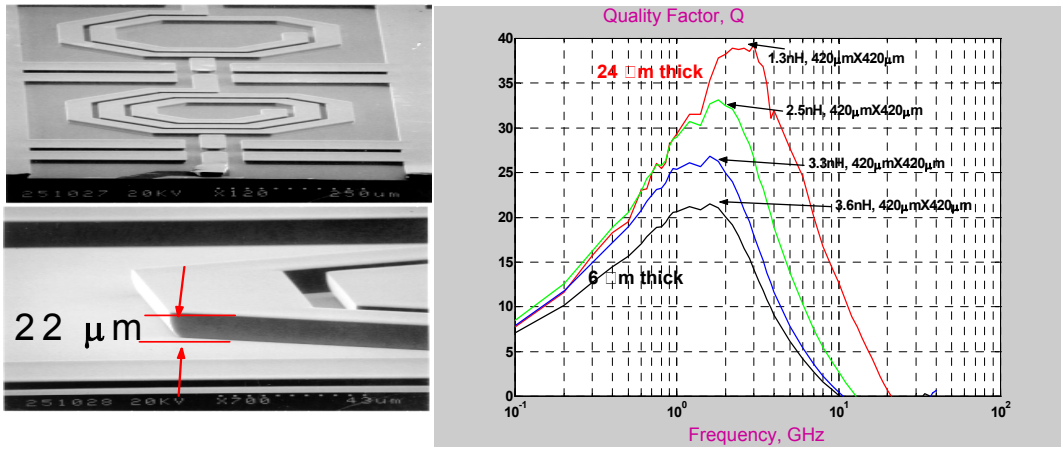


Figure 2. Thick copper inductor fabricated using electroplating through a photoresist mask approach and measurement of quality factor (Q) demonstrating Q of 40 [1].

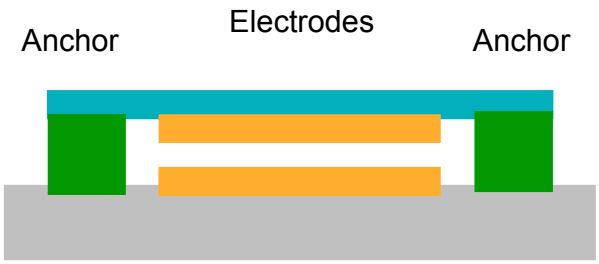


Figure 3. Schematic of a resonator beam

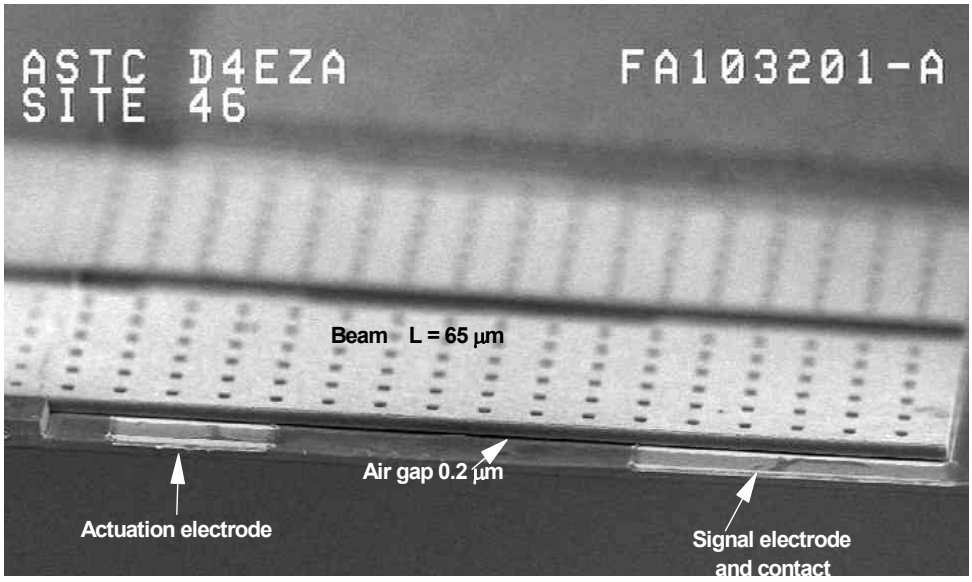


Figure 4. SEM cross section of MEMS switch. Note the lower actuation electrode and the signal electrode. The free standing beam is fabricated out of electroplated copper. The air gap between the beam level and the lower electrodes is 0.2 μm [1].

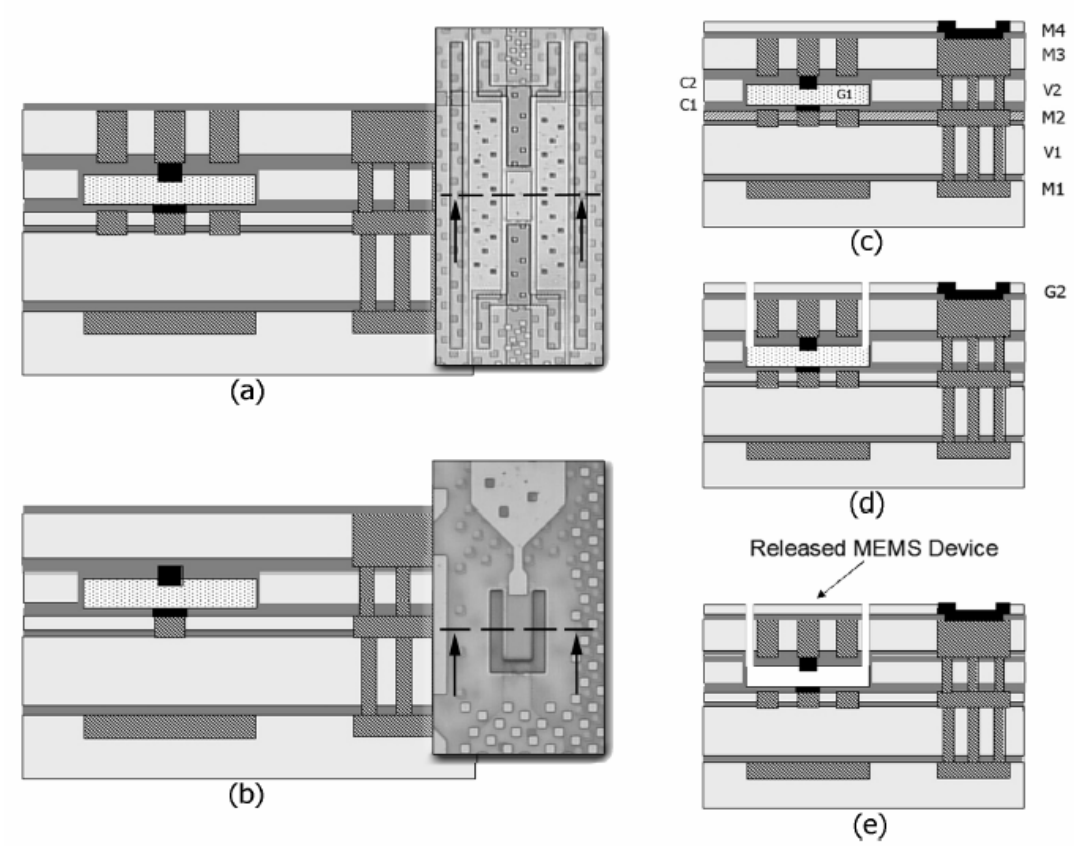


Figure 5. Cross-section schematics and plan view optical photographs of the directly integrated MEMS switch device (a) and resonator (b), respectively. Figure e shows a cross-section of all levels for a released MEMS devices with probe pad metallurgy on the right side [9].

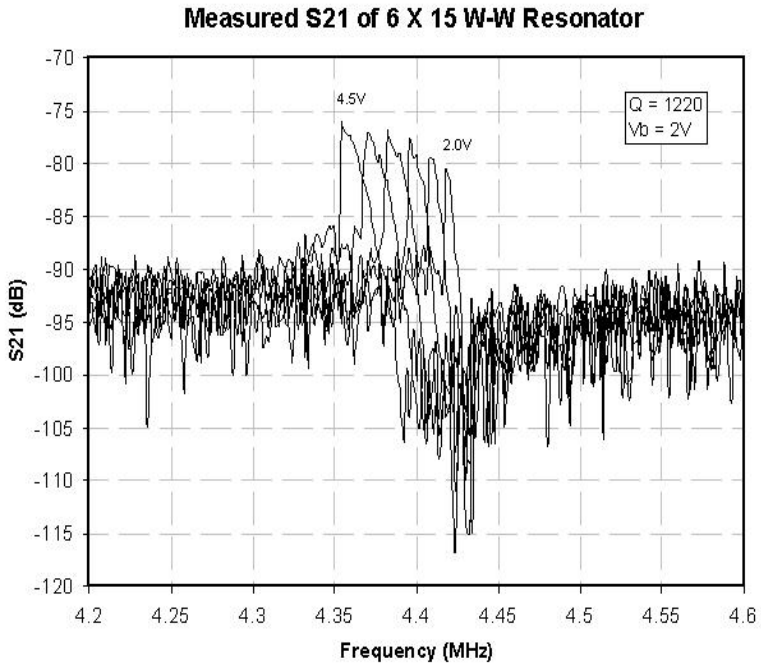
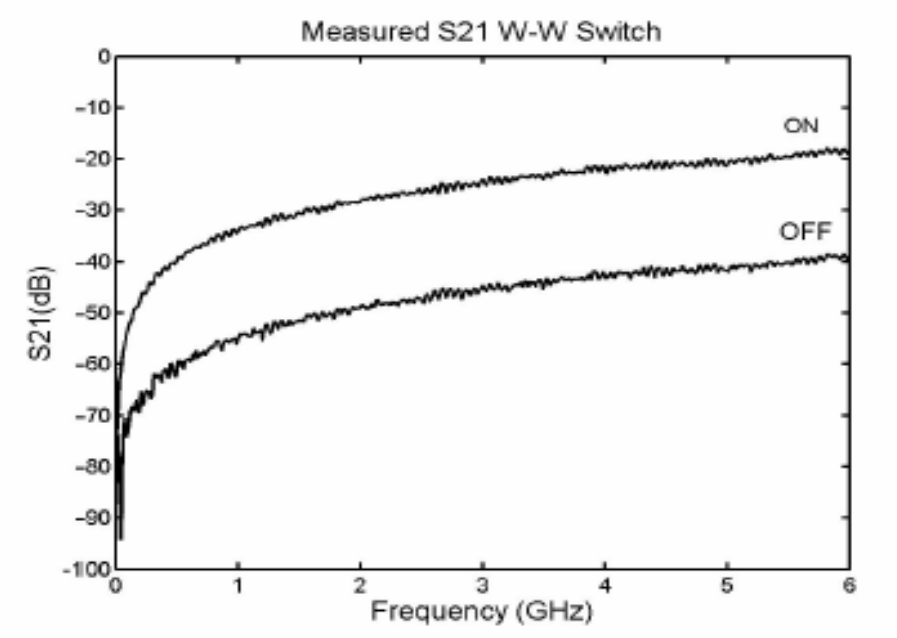
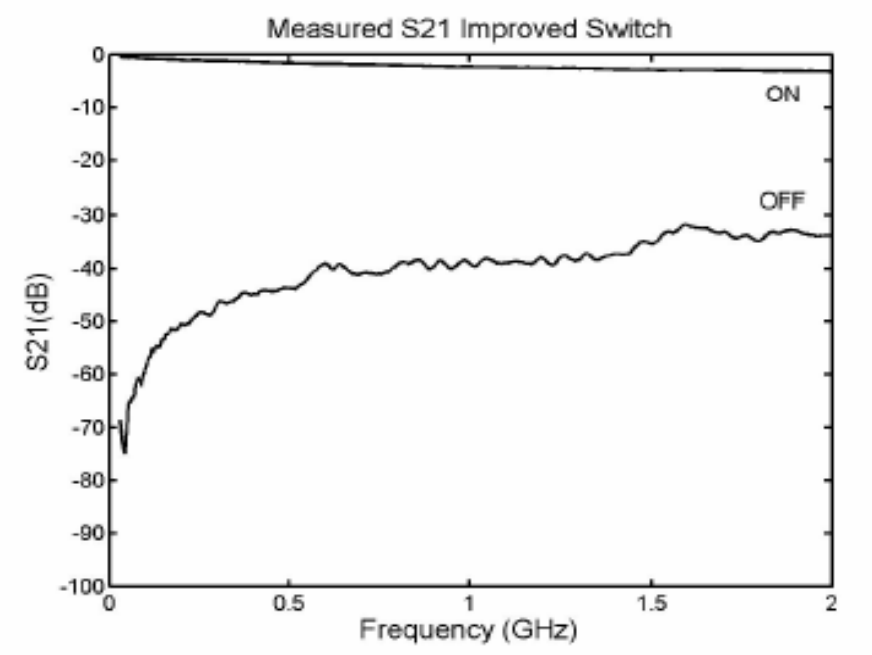


Figure 6. S21 transmission of resonator fabricated with tungsten and tested with applied bias ranging from 2V to 4.5V at 10mTorr pressure [9].



(a)



(b)

Figure 7. Measured S21 isolation in off position and insertion loss in on position for a series MEMS switch with tungsten contacts (a) and improved contact metal (b). Actuation voltage is about 40V in both cases [9].

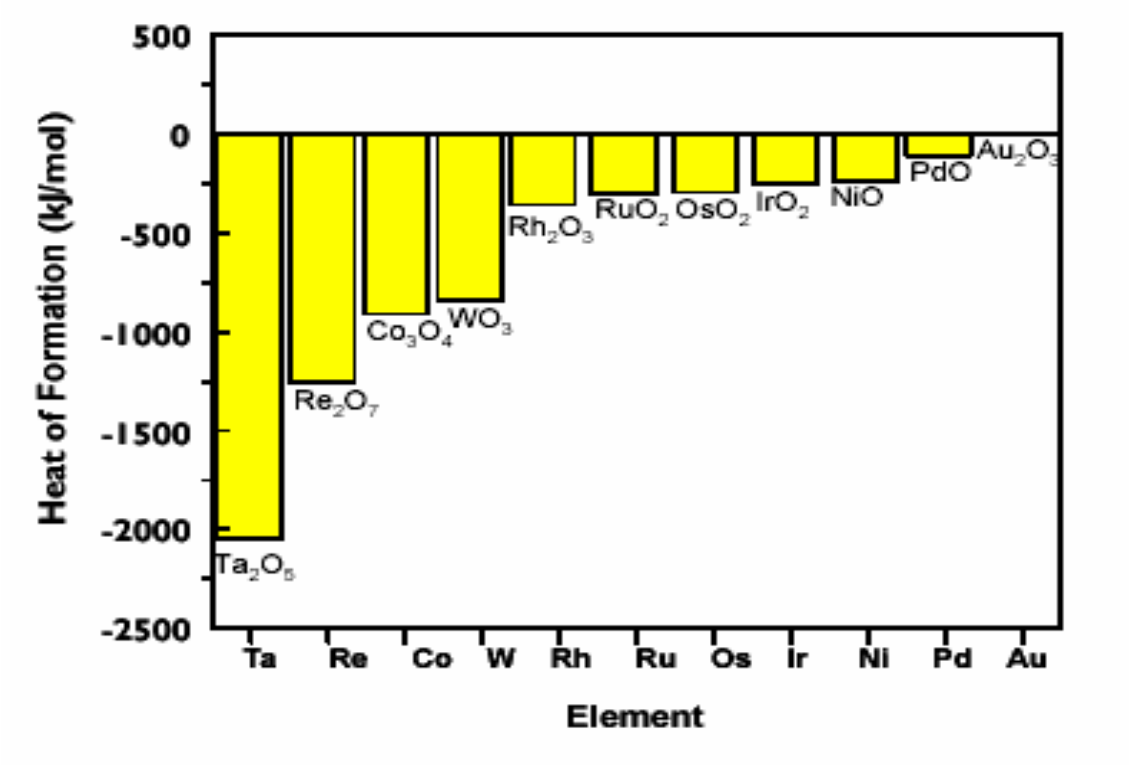


Figure 8. Heat of oxide formation for selected metals [10].