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IBM Research Report

Impact of Ultra Thin Oxide Breakdown on Circuits

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1. Introduction

CMOS scaling with SiO_2 or oxynitride gate dielectrics for advanced high-performance logic and memory has reached a point where one or several oxide breakdown (BD) events are expected over the life of a chip. [1,2] Previous oxide reliability projections were based on the assumption that a single breakdown (soft or hard) on a chip would cause circuit failure, which is no longer believed to be correct. For accurate reliability projections it is necessary to better understand the nature of the BD event and the effect of BD on circuits.

2. Progressive breakdown

Several groups [3-5] have pointed out that "hard" BD is not a sudden, catastrophic process, as previously thought. BD occurs gradually over a measurable time scale. The growth of the gate leakage though the BD spot can be very slow at low stress voltage. This phenomenon has been labeled "progressive" breakdown. [3] Progressive BD is a *gradual* hard BD, and is distinct from "soft" BD, which is a stable, low current that is typically not observed in small devices. Examples of current-vs.-time time traces are shown in Fig. 1. [4]

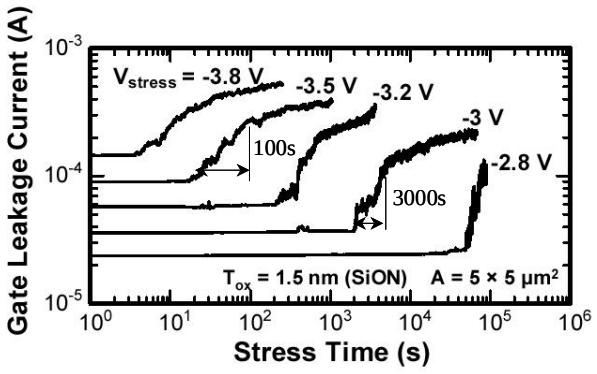

Fig. 1. Example of progressive BD, showing the slow, voltage-dependent growth of leakage current after oxide BD. After ref. [4].

The post-BD growth can be quantified in various ways. [3-8] Fig. 2 shows the voltage dependence of the progressive breakdown rate, R_D, for t_{ox}=1.5nm. [5] This is similar to the voltage dependence of the trap generation leading breakdown, suggesting that the same defect generation process that controls the initial breakdown time also drives the growth of the BD spot.

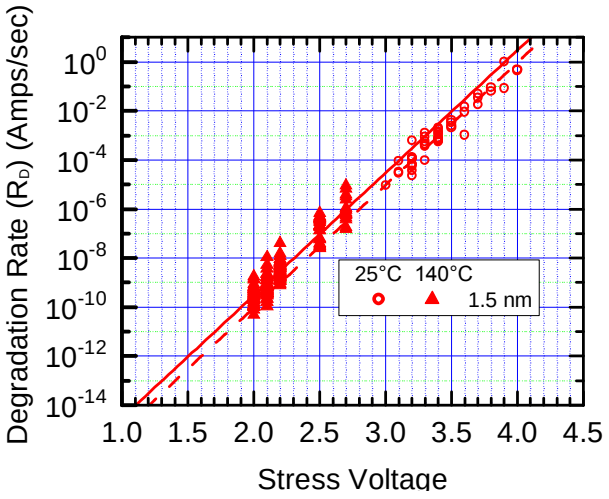

Fig. 2. The rate of increase of stress current for a 1.5 nm oxide after the beginning of breakdown, showing an exponential dependence for 10 orders of magnitude over a wide range of voltages. The degradation rate RD is defined as the average rate of increase from 10μA to 100μA. After ref. [5].

3. Effect on circuits

The effect of progressive BD has been studied experimentally using inverters in a 0.13μm technology (t_{ox} = 1.5nm). [9,10] Constant voltage stress at 2.6–3.9 V of either polarity was applied from input to output, with V_{dd} and ground terminals floating. In this way a BD was made to occur at the drain side of either the n-FET or p-FET. Progressive BD was stopped at various stages by a current compliance. [11]

The transfer characteristics of the broken inverters (Fig. 3) exhibit a combination of V_t shifts due to the voltage stress and reduced output swing due to post-BD leakage. The characteristics of the BD spot are different depending on stress polarity and whether the inverter output voltage is higher or lower than the input. In this figure the transfer curves show additional shift in switching point due to threshold voltage shifts in the n-FET and p-FET. These shifts occur already prior to the BD event.

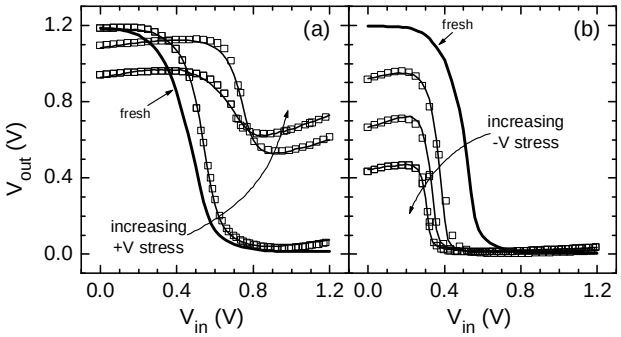

Fig. 3. Transfer curves of inverters after BD to various levels. (a) Positive stress on inverter input. (b) Negative stress on inverter input. Lines are experiment, symbols are model. For positive/negative stress, the leakage is highest when the input is higher/lower than the output. After ref. [10].

The main effect of BD is to introduce additional gate-to-source or gate-to-drain leakage. To include the effect of gate oxide BD in a circuit simulation, simple voltage-dependent current sources can be added between gate and drain or gate and source (Fig. 4). [10]

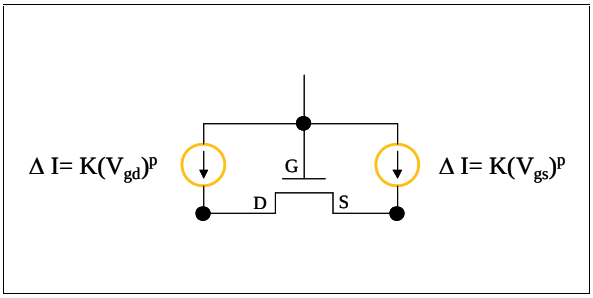

Fig. 4. Circuit model of gate-to-diffusion breakdown. A voltage dependent resistance is placed at either the gate-drain or the gate-source location. After ref. [9].

Calculated transfer characteristics using the same gate-to-drain leakage current model but without the V_t shift (Fig. 5) illustrate the influence of the oxide BD leakage current alone in the inverter transfer curve, to more accurately represent the effect of early BD under circuit operation conditions. The inverter transfer curves shown in Fig. 5 are the expected characteristics for chips in the field, where the earliest oxide breakdown may occur prior to significant V_t shift.

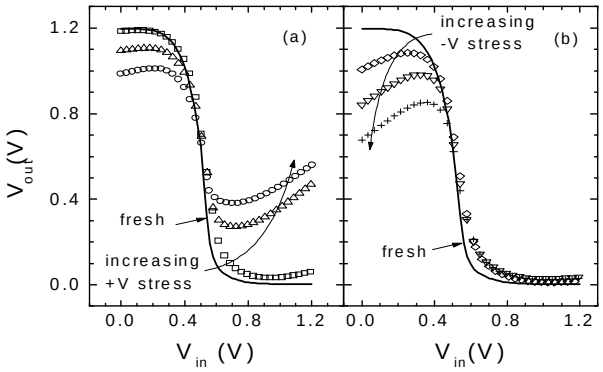

Fig. 5. Simulated inverter transfer curves with oxide leakage currents between the inverter input and output using same leakage as in Fig. 3, but with no V_t shifts (a) positive stress on the inverter input, (b) negative stress. After ref. [10].

Fig. 6 shows calculated transfer curves for two inverters in series with a drain (input-output) breakdown in the second inverter. The output of the first inverter is degraded, even though there is no breakdown in this stage. This is because the BD leakage in the second stage loads the first stage. Subsequent logic stages will restore the correct logical "1" and "0" states as long as the output of the broken stage is on the correct side of the crossover voltage Vco.

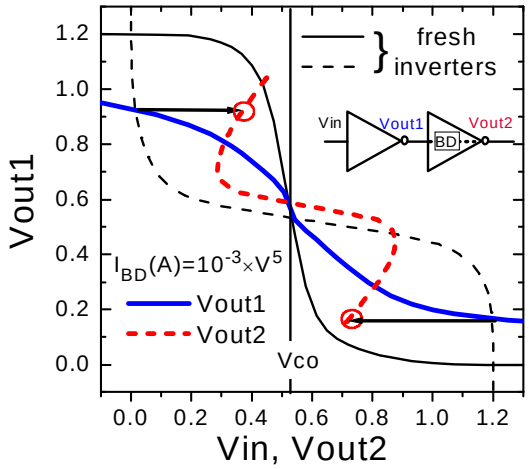

Fig. 6. Transfer curves for two inverters in series, with a drain (input-output) breakdown in the second stage. Small circles indicate the output states of the second inverter. Inverter chains transmit the correct logic state as long as output of broken stage is on the correct side of the crossover voltage. Thin (solid and dash) black lines represent Vout1 and Vout2 respectively without BD. After ref. [10].

In an SRAM cell (Fig. 7, inset) oxide BD in either inverter of the cell loads the other inverter. Gate-to-source BD does not affect the transfer curve of an inverter, to first order. However, it does perturb the voltage at the output of the opposite inverter. A p-(n-)

source BD raises (lowers) the voltage at the output of the opposite inverter, which must then supply current through the channel resistance of the on-state n-(p-)FET of the intact inverter. In order to quantify the cell stability we extract the worst-case static noise margin (SNM). This is the minimum DC noise voltage necessary to flip the state of the cell during a "read" operation, where the word line is pulled high while the bitlines are pre-charged high.

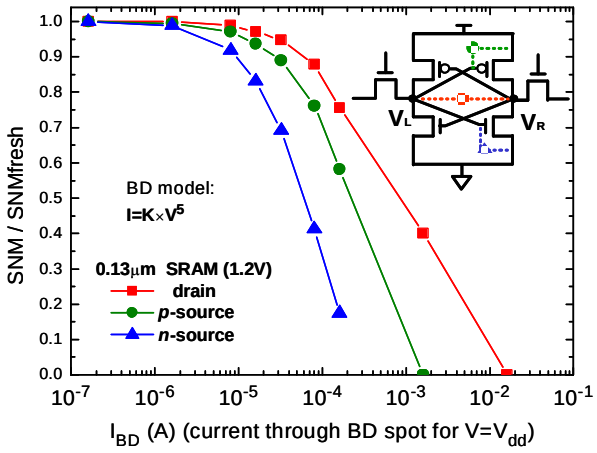

Fig. 7. Normalized SNM from circuit simulations as a function of BD leakage at V_{dd}, for 6-T SRAM cells with various BD locations. Symbols indicate BD locations. After ref. [12].

For fixed leakage, BD at p-source has less effect than n-source, because the opposing n-FET is stronger (relative to the p-FET). Fig. 7 shows the SNM, normalized to the SNM of the fresh cell, as a function of I_{BD} in a 0.13μm technology. [12]. These results were obtained from circuit simulations. For the cells considered in this work, a 50% degradation in SNM results from oxide BD when the current through the BD spot reaches ~20–50 μA for the worst-case n-source breakdown. [13] Pass-gate or p-source breakdown may tolerate higher leakage, up to ~500 μA. These values are comparable with the on-currents of the fresh p-FET and n-FET respectively used in this SRAM cell, and may decrease with device widths, *e.g.*, for smaller SRAM cells.

4. An Improved Terminology

Oxide breakdown events are usually described as "soft" or "hard" (SBD and HBD, respectively) depending on the magnitude of the post-breakdown conduction. Various schemes have been devised to characterize the BD "hardness," *e.g.*, the post-breakdown resistance (V_{dd}/I_{BD}) or conductance (dI_{BD}/dV), [14-17] however this designation is often ambiguous because there is no universally accepted criterion. The result is that one author may refer to a given BD current as SBD while another might characterize the same event as HBD. For example, when testing a very thin oxide where the initial tunneling current is larger than the current through the BD spot, a "hard" breakdown could be interpreted as soft. When testing a large area structure, the spreading resistance to the BD spot can cause the PBD growth to saturate, making a "hard" BD appear as "soft", and the possibility of multiple BD spots may further confuse the interpretation. Many if not all reported SBD phenomena (earlier called "quasi" breakdown or QB) in oxides may be attributed to the saturation effect caused by parasitic and spreading resistances.

While such issues can be overcome with careful experimental design, the recent understanding of the *progressive* BD phenomenon (PBD) has made these earlier terminologies less satisfactory, and has spawned a new set of terms such as "progressive HBD" and "unstable SBD". [18,19] In addition, the realization that the initial breakdown event ("first BD") may not disrupt circuit functionality has led to a further redefinition of the terms SBD and BBD depending on the intended operation conditions of the MOSFET. [18] This *operational* definition obscures the *physical* nature of the BD. Here we attempt a new view of BD characterization and propose a simpler, more physically meaningful terminology.

The steep voltage dependence of the post-breakdown degradation rate leads to an important implication for the BD characterization. As earlier pointed out by Monsieur , [3] if the oxide is stressed at a high voltage where the post-breakdown degradation rate is fast compared to the experimental sampling time (typically longer than ~tens of milliseconds) then the breakdown will appear as "hard" according to the typical usage of this term. Likewise, if the oxide is stressed at a low voltage where the degradation rate is slow compared to the experimental sampling time, then the breakdown will appear as "soft".

This implies that there is no distinct physical characteristic which we can use to classify HBD vs. SBD. Rather, it is the exponential voltage and thickness dependence of the PBD growth time τ_D which causes a BD to appear as HBD for thick oxides and/or higher voltage and as SBD for thin oxides and/or lower voltages. This is illustrated schematically in Fig 8, where the dashed line corresponds to a constant value of τ_D on the order of the experimental sampling time. Below this line the BD appears soft, while above the line the BD appears hard in a typical experiment. The hatched region corresponds to the domain which is accessible to experiment, *i.e.* within this band the time to first BD is of order seconds to hours. As oxide thickness is reduced the time to BD decreases rapidly because of the rapid increase in tunneling current, [20] which requires the use of lower V_{stress} to keep the BD time within measurable range.

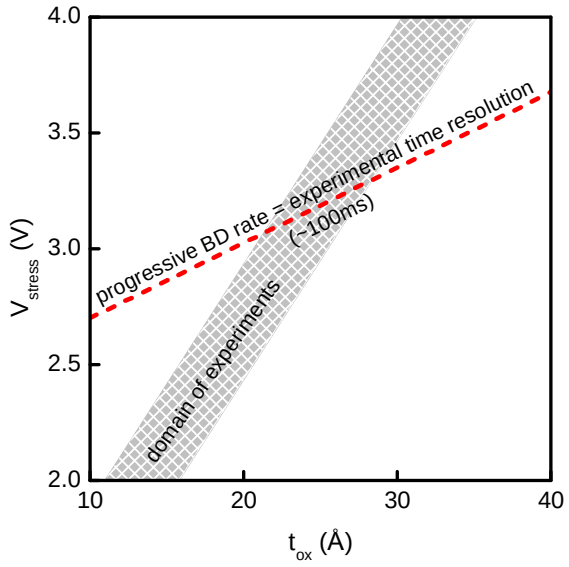

Fig. 8. The dashed line corresponds to a constant value of τ_D on the order of the experimental time resolution, for oxides of thickness t_{ox} stressed at voltage V_{stress}. Below this line the BD appears soft, while above the line the BD appears hard in a typical experiment. The hatched region corresponds to the domain which is accessible to experiment. After a similar figure by Monsieur. [3]

This figure explains the observed trend that HBD is more prevalent in thicker oxides, *i.e.* this is really an effect of the changing V_{stress}, more so than t_{ox}. This also provides an explanation for the so-called HBD prevalence ratio which shows a rapid transition from ~0% to ~100% over a narrow voltage range, moving to higher voltage with increasing thickness [7]. The transition from SBD-like to HBD-like is not completely abrupt because of the existence of a statistical distribution in τ_D.

Thus, HBD and SBD are really just different manifestations of the same PBD mode, and the distinction between HBD and SBD depends mostly on measurement conditions. Only the degradation rate, if accurately measured as described in the previous section, is fundamental. The BD can be described as *fast progressive* (FP) or *slow progressive* (SP), depending whether τ_D is less or greater than the experimental time resolution, or more generally, whether τ_D is less than or greater than the median time-to breakdown T_{BD} for the sample under study. The terms "soft" and "hard" should be avoided, because of their vague meaning. A more accurate term to describe the case of moderate or low post-breakdown conduction, such as results from removing the stress during the BD transient (either intentionally, *e.g.* by a compliance limit, or unintentionally, *e.g.* by series resistance) is *arrested* BD.

A different terminology should be used to describe the impact of breakdown on device and circuit functionality, to clearly distinguish this from the physical phenomenology. A BD which disrupts device or circuit functionality can be called *destructive*. It must be recognized, of course, that this is an application-specific description. For example, a BD with ~ 50μA leakage at operation condition may be destructive in an SRAM application [12] but not in logic. [6,21,22] It is important to realize also that a less severe BD (*i.e.* non-destructive) cannot be assumed to be completely innocuous, since the initial BD spot may grow progressively into a destructive one.

5. Conclusions

Oxide breakdown evolves in a continuous, voltage-driven manner from initial BD to higher conductance. This permits a redefinition of the oxide failure criterion. Instead of the time to first (soft) BD, the appropriate failure criterion is a critical leakage current that disrupts circuit operation. Lifetime estimates may be increased by one or more orders of magnitude over traditional first-BD projections. [2] This new oxide failure criterion has two key elements: Understanding and characterizing the post-breakdown defect growth and conduction, and understanding and characterizing the circuit sensitivity to leakage currents in gates that have experienced BD. Circuit simulations can be used to estimate circuit sensitivity to BD, by adding a voltage-dependent current source between the gate and one diffusion of a transistor.

Acknowledgements

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