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Recent Progress on Pb-free Electronics in IBM

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Lead (Pb)-containing solders have been extensively used in microelectronic interconnect structures between various packaging levels. Since the RoHS enforcement date of July 1st, 2006 by European Union [1] is rapidly approaching, the transition from Pb-containing solders to Pb-free solders is accelerating in the electronic industry.

In IBM, considerable R&D efforts on Pb-free solders technology were conducted well before the RoHS and WEEE directives[2] were enacted by the European Union, as noticed in the early publication and patent literature [3-5]. An example of the application of Pb-free technology within IBM is the usage of Bi-Sn eutectic solder for low temperature wave soldering of PTH (plated through holes) in advanced multilayer printed circuit boards (PCB) since early 1970's [6, 7]. IBM's early work had led to the NCMS(National Center for Manufacturing Sciences) Pb-free solder project, the first industry-wide joint efforts to search for Pb-free solders. When the final report of the NCMS Pb-free project was published in 1997, it was dedicated to the memory of Roger Wild (former IBMer) for his pioneering work on Pb-free soldering technology in IBM[8].

Fundamentals

Recently, the world-wide R&D efforts on Pb-free solder alloys have identified several promising candidates for different soldering applications as listed in Table I. Two major Pb-containing solders, eutectic 63Sn-37Pb and Pb-rich solders used for SMT and flip chip or C4 (Controlled Collapse Chip Connection) solder bumps are also included in Table I. It should be noted that the compositions of most of the Pb-free solder candidates are Sn-rich solders that

contain more than 90% Sn. This suggests that the physical, chemical and mechanical properties of the proposed Pb-free solders are heavily influenced by the properties of pure Sn, as opposed to eutectic Sn-Pb which microstructure consists of a mixture of Sn-rich and Pb-rich lamellar phases. Pure Sn is polymorphic, capable of existing as three different crystal structures (α, β, γ) depending on temperature and pressure [9]. Since the white tin phase (β-Sn) has a body-centered tetragonal (BCT) crystal structure in contrast to the face-centered cubic (FCC) structure of Pb, the physical and mechanical properties of white tin are less isotropic and more difficult to mechanically deform in comparison to Pb. Since the white Sn crystal is optically birefringent, polarized light microscopy can be used to distinguish the orientation of β-Sn dendrite structures in Pb-free solders [10].

The melting point of most Pb-free commercial solders is within the range of 208ºC to 227ºC, which is about 30ºC higher than the melting point of eutectic Sn-Pb at 183ºC. The higher melting point has serious implications on the performance of packaging materials and assembly processes, and can affect the integrity and/or reliability of Pb-free microelectronic packages. Another important issue associated with the proposed Pb-free solders is the difficulty of maintaining solder melting-point hierarchy, which has been well established with Pb-containing solders. With the proposed Pb-free solders, the maximum differentiation in solder melting temperatures between any two package levels is less than 30ºC. Hence, the process control, during successive multiple soldering processes with Pb-free solders, becomes more challenging and its impact on solder joint and package reliability is not yet well understood.

Among the several Pb-free solder candidates, the near-ternary eutectic Sn-Ag-Cu (SAC) alloy compositions with melting temperatures around 217ºC is the concensus solder alloy [11, 12] for SMT card assembly, including BGA solder joints, while the eutectic Sn-Cu or Sn-Ag-Cu alloy is a promising choice for Pb-free flip chip applications [13, 14].

Pb-free CBGA (Ceramic Ball Grid Array)

The IBM development team conducted several evaluations, using a number of criteria, in the early phase. Sn-3.8Ag-0.7Cu (SAC in wt %) was selected based on its excellent wettability to I/O pads, stable microstructure of solder joints, superior ball shear strength, and last but not least, the excellent thermal-mechanical fatigue (TMF) behavior of assembled modules subjected to

accelerated thermal cycling [15]. Further work with SAC confirmed that it was an optimal replacement alloy for Sn-Pb CBGAs for both 1.27mm and 1.00mm pitch [16].

Reliability evaluation was performed with co-fired multi-layer 9211 (alumina-based) ceramic test vehicles (32.5 mm square to 42.5mm square with thickness ranging from 1.50mm to 3.70mm). Five ceramic modules were attached by using SAC solder balls to a FR4 test card (6S4P, 229 mm x 279 mm). A typical cross-section of a CBGA solder joint connecting a ceramic module to a Cu pad on a PCB (as-joined) is shown in Figure 1. Standard accelerated thermal cycle (ATC) testing (from 0 to 100°C, with 2 cycles per hour) was used on the assemblies with a periodic, four-point resistance measurement. An increase in resistance of 10 ohms or greater was used to define a failure. Table II summarizes the MTF data of Pb-free CBGA modules in comparison with the Sn-Pb, IBM dual-melt structure as a benchmark. The N50s were calculated by fitting a lognormal distribution to the fatigue data. All the SAC alloy test vehicles produced well-controlled fatigue life as indicated by the small sigma. The SAC alloy has almost twice the fatigue life of the dual alloy Sn/Pb structure, for the same form factor. The full melting of SAC balls during assembly causes a smaller joint height with the SAC structure than the Sn-Pb structure. In spite of the unfavorable ratio of joint heights (1:2), the SAC alloy demonstrates the superior fatigue properties over the Sn-Pb for the same form factor. The excellent TMF performance of SAC, combined with the relative lack of complexity in manufacturing these assemblies, makes the Pb-free, CBGA technology a winner on all fronts

Pb-free PBGA

The transition to Pb-free soldering technology has been juxtaposed on other market forces driving PBGA packaging toward high performance, higher I/O and high reliability applications. The confluence of all of these factors in time has made the development of Pb-free organic packaging technology a challenging watershed to cross. The higher reflow temperatures associated with Pb-free packaging technology have mandated the use of new organic packaging materials with improved water absorption characteristics, reduced CTE's and improved thermal stability. The higher reflow temperatures and the accompanying evolution toward higher I/O and larger chip sizes result in higher package stresses and place more stringent requirements on interfacial adhesion within electronic package structures. The stresses fostering package delamination derive from CTE mismatch, from increased steam pressurization within the

packages, due to the presence of absorbed moisture, and in the case of flip chip packaging from the full melting of the C4 bumps within the underfill encapsulation. The choice of solderable surface finish and its bearing on solder joint fragility is a significant concern across the industry at this time. In this regard IBM has chosen Cu pad structures as the surface finish for most of its packaging requirements. Successful Pb-free packaging, capable of passing stringent reliability testing, has mandated improved materials and significant interfacial adhesion augmentation.

1) Wire-Bond, PBGA Packaging

IBM has produced Pb-free wire-bond PBGA packages since early 2002 in both glob-top and overmolded configurations. IBM expects to be qualified to produce Pb-free and halogen-free products by the end of 2005. Package sizes range from 15 to 45 mm with 1.27 and 1.0 mm BGA pitch, available . To achieve these results, new glob-top and overmold materials were developed in close working relationships with materials suppliers. The new materials have improved adhesion and moisture absorption characteristics, together with improved wire sweep processing characteristic, capable of accommodating complex wire-bond trajectories.

2) Flip Chip, PBGA Packaging

Flip chip packaging is associated with a broader range on packaging challenges in achieving a successful transition to Pb-free soldering technology. New BLM (Ball Limiting Metallurgy or UBM) structures are required to accommodate the use of high Sn, Pb-free, solders. The full melting, Pb-free, C4 structures provide for higher internal package stresses, during reflow, because the bump volume increase associated with the melting process is constrained by the underfill encapsulant. The use of new underfill materials was required to meet the Pb-free reflow requirements. In addition new thermal solutions and lower CTE laminate materials were incorporated to improve package reliability, as the simultaneous evolutionary transition was made toward higher performance modules. Package qualifications have been successful with the new organic material set and solder alloys. Flip chip PBGA products are now qualified from 15 to 42.5 mm for both 225 and 200 μm C4 pitch with 1.27 and 1.0 mm BGA pitch. Future extension to 55 mm package size is anticipated in the near future.

Pb-free Flip Chip Solder Plating

IBM has been developing a Pb-free C4 solder bumping process for flip chip applications in response to customer requirements and environmental regulations. IBM has been plating C4

solder (97Pb-3Sn) for over 9 years using a TiW/CrCu/Cu BLM structure. This has proven to be a very reliable and production capable process.

The development approach for Pb-free C4 plating incorporated several key ground rules. A multi-functional team including development, process, equipment, quality, reliability and product engineering, analysis, research and manufacturing was formed. Minimal changes to the existing successful BLM structure were desired. The new Pb-free process was designed to maximize use of the existing production line capital infrastructure and process for ease of manufacturing.

The two key components of the Pb-free C4 structure are the BLM and the C4 metallurgy. It is well known that the Pb-free, Sn-rich solders are highly reactive and, therefore, require a robust barrier metallurgy in the BLM in order to withstand aggressive high-temperature-storage (HTS) and electromigration requirements. IBM has been using a Ni barrier for other products, and chose to incorporate Ni as the barrier for Pb-free C4. For the solder metallurgy, we evaluated Sn-Cu as well as Sn-Ag-Cu (SAC) constructions. The evaluation criteria included ease of manufacturing, quality and reliability. From a reliability standpoint, the SAC and Sn-Cu solders performed equivalently. With our current tool set, the greater ease of manufacturing and better bump quality of Sn-Cu resulted in our choice of Sn-Cu over SAC. The construction IBM subsequently qualified for production is a TiW/CrCu/Cu/Ni BLM with Sn-Cu solder metallurgy, as shown in Figure 2.

The first Pb-free C4 application that IBM qualified and put into production is a chip-on-flex application. We completed a production line qualification as well as a reliability assessment. There were no C4 fails in deep-thermal-cycling (DTC), HTS, low-temperature-storage (LTS), temperature/humidity & bias (THB), high-temperature-operating-life (HTOL) or ATC stresses. Electromigration performance of this Pb-free C4 was better than expected, between eutectic Sn-Pb solder and 97Pb-3Sn solder in performance. This application is now in production at IBM.

The key challenge for the future will be to provide Pb-free C4 bumps at 150 μm pitch and below. IBM is currently developing solutions for that application space. In summary, IBM has developed, qualified and is in production for Pb-free C4 bumps. Qualification for additional applications is in progress, with a good prognosis for continued success.

C4NP for Pb-free Wafer Bumping

Multiple transitions are presently occurring in the wafer bumping industry. Among these are increased wafer size from 200 to 300mm, decreased bump size and pitch, alloy change from eutectic Pb-Sn to Pb-free and the continued growth of flip chip vs. wire bond. At the same time, the demand for lower costs, finer pitch and higher quality is unrelenting. In September of 2004, IBM and SUSS MicroTech announced a new wafer bumping technology called C4NP (Controlled Collapse Chip Connect New Process) to address these challenges. SUSS has been developing the manufacturing infrastructure while IBM has been qualifying the technology and continuing advanced development.

C4NP grew out of earlier work at IBM Research in which a new injection molded solder (IMS) process produced advanced thermal interfaces. It was quickly realized that IMS could readily be applied for making solder interconnect structures. A parallel process, C4NP fills molten solder into small cavities in a bump template that matches the I/O footprint of a silicon wafer. After the solder is solidified, an inspection step assures that all the cavities are properly filled. Separately, wafers are prepared with the appropriate BLM compatible with the desired solder alloy. The last step actually bumps the wafer, namely aligning the filled bump template and joining it in mirror image fashion to the silicon wafer above the solder reflow temperature. This transfers the solder volumes from the cavities to the wafer. The bump templates are reusable, thus keeping costs low. Several important advantages can be listed for C4NP:

- alloy flexibility including multi-component Pb-free alloys
- no volume change from deposition to final bump; extendible to fine bump size & pitch
- same tool set for both 200 & 300mm wafers
- low material costs in comparison to paste, preform or chemical solution
- optimal yields by bump template inspection before transfer to wafer
- rapid turn-around time by prefilling bump templates ahead of wafer completion
- efficient solder usage for environmental and economic benefits
- extendability to finer pitch
- process simplicity similar to stencil printing

As seen in Table III, a comparison of other established bumping processes explains why C4NP is creating excitement in the industry. Some time ago, Gail Flowers, editor-in-chief of 'Advanced Packaging' asked: *"When will we see standardization in flip-chip processes? ..... What are the long shots in flip chips that could bring about major changes?"* Considering the

challenges ahead, the timing of a new bumping technology that combines high-end capabilities with low-end costs may be considered auspicious. Over 40 years ago IBM first introduced C4 technology. C4NP, as the latest version, should provide a cost-effective solution to meet present and future Pb-free wafer bumping needs.

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Table I. Some Pb-Free and Pb-Containing Solders

Composition (wt %)	Melting point (°C)	Applications	Concerns
Sn-3.5Ag	221 (eutectic)	SMT, flip chip	Cu dissolution, Excessive IMCs, Voids
Sn-3.8Ag-0.7Cu	217	SMT, PTH, BGA	Cu dissolution, Excessive IMCs, Voids
Sn-3.5Ag-3Bi	208-215	SMT	Cu dissolution Fillet lift, low mp phase
Sn-0.7Cu	227 (eutectic)	PTH, flip chp	Cu dissolution, Wetting, excessive IMCs
Sn-8Zn-3Bi	190-194	SMT, BGA	Wetting, Oxidation
63Sn-37Pb	183 (eutectic)	PTH, SMT, BGA	Pb toxicity
97Pb-3Sn	317	Flip chip, C4	Pb toxicity

Table II. Summary of 1.00mm Pitch BGA Lifetimes in ATC

Alloy	**Substrate Size (mm)**	**Life N50 (cycle)**	**Sigma**	**Comments**
SAC	42x42x1.50	1628	0.08	Actual
SAC	42x42x2.55	946	0.12	Actual
SAC	42x42x3.70	653	0.16	Actual
SAC	32x32x1.50	1860	0.12	Actual
SAC	32x32x2.40	1310	0.14	Actual
Sn-Pb	32x32x2.40	740	0.16	Reference Database

Table III. Comparison of Wafer Bumping Processes (Color key: **POOR** **FAIR** **GOOD**)

	Evaporation	**Plating**	**Screening**	***C4NP***
Cost				
Reliability				
Yield				
Alloy Flexibility				
Extendibility to 300mm				
Very fine bump				
Process complexity				
Industry proven				

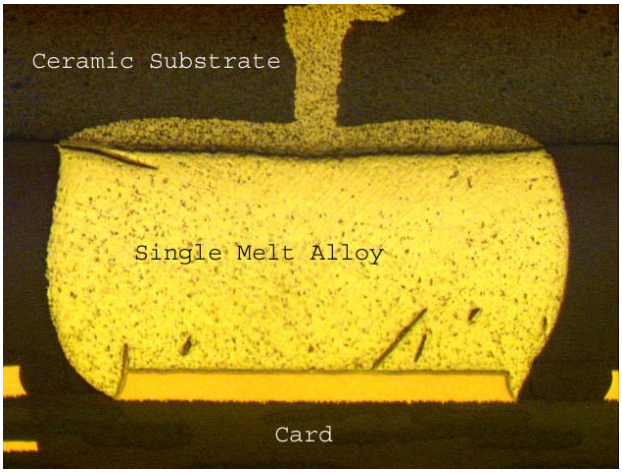

Figure 1: Cross-section of a typical SAC CBGA assembly

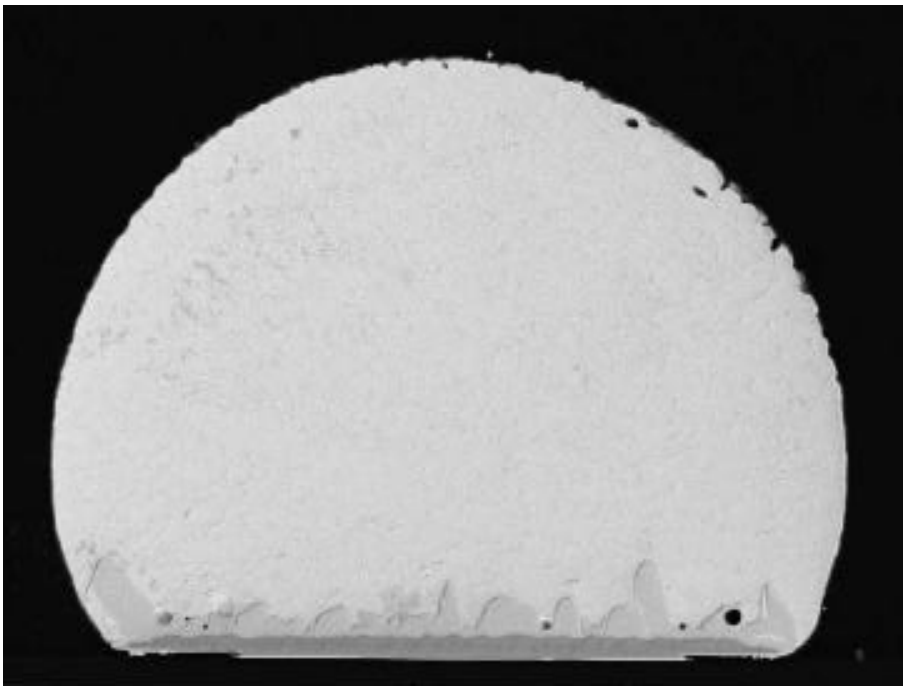

Figure 2: IBM Pb-free C4 bump, (courtesy of C. Goldsmith).