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On-chip Bus Interleaving Revisited

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On-Chip Bus Interleaving Revisited

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Abstract: Repeater interleaving is used to reduce the impact of capacitive coupling noise on the worst-case delay in local on-chip RC buses. In this paper, we revisit this interconnect design practice to evaluate it from the viewpoint of signal integrity of global on-chip interconnect used in on-chip high-speed signaling as between a cache and a CPU. Using accurate $R(f)L(f)C$ electrical models of the global bus, we show that the peak crosstalk noise exhibits both monotonic and convex dependence on the interleaving ratio. Furthermore, we show that the worst-case switching pattern used in quantifying the common-mode noise (CMN) on the bus depends on the repeater interleaving ratio. This dependence makes the search of the optimal ratio that minimizes bus CMN quite challenging. The conclusions of this paper are valid for both unidirectional and bidirectional buses.

1 Interleaving of Local Buses

To illustrate the advantages of bus interleaving in on-chip interconnect design, consider the 3-line, 3-stage buses of Figure 1. The stage length is l, and so the total length of the bus is $3l$. Figure 1(a) is the typical layout of a unidirectional bus with the repeater banks aligned across the wires. In Figure 1(c), the repeaters of the middle wire are placed midway between the repeaters of the wires adjacent to it. The interleaving ratio, ρ, is defined as the ratio of the wire length between two successive repeaters on two adjacent lines and the wire length of the stage. The interleaved layout in Figure 1(b) is for $\rho = 0.5$ in the case of a unidirectional bus. In Figure 1(c), the same ratio is used but for a bidirectional bus. These three buses are run on the next to the top metal layer of a back-end-of-the-line cross section whose dimensions are given in Figure 2. The supply voltage of the process is $V_{dd} = 0.9$V. The bus per-unit-length (PUL) parameters have been extracted, and an RC electrical model has been synthesized and analyzed using SPICE-level simulation. In the analysis, the repeaters have been sized so as to guarantee a slew rate of $30ps$ or better at the near end of all the active wire segments. The length of each stage was set to $1mm$. The main results of the RC bus analysis are shown in Figure 3.

The waveforms of Figure 3(a) show that the use of an interleaved bus results in the reduction of 50% worst-case delay by 31% (from 61ps to 43ps). The peak crosstalk noise (active middle line, quiet adjacent lines) is similarly reduced by 46% (from 40mV to 21 mV) for the near-end node (NEN) and by 63% (from 59mV to 22mV) for the far-end node (FEN) as seen in Figure 3(b). The worst-case noise peak for the bus (quiet middle line with adjacent lines switching in the same direction) is also reduced by 52% for the NEN and by 63% for the FEN as seen in Figure 3(c). It is not difficult to intuitively understand the way these reductions come about in the interleaved bus. In Figure 3(d) where the middle line is the victim and the adjacent lines are switching in the same direction, every segment of the victim line is always subject to two opposing influences, the one upstream of the repeaters adjacent to the segment and the one downstream of them. These two opposing influences tend to cancel each other's effect on the victim line. One interesting feature of the noise waveforms of Figures 3(b) and (c) for the interleaved bus is that the noise is not a pulse as for the uniform bus but a dipole with one positive peak and a negative valley. This means that for realistic interleaved buses, the integral of the noise waveform is not a good metric for noise *even* for RC buses. This integral is sometimes used to estimate the noise pulse width and the noise pulse peak in linear RC networks [1]. These observations are also valid for bidirectional buses. Recently, a method for finding the optimal interleaving ratio for a bidirectional RC bus was developed in [2]. The authors of [2] have shown that if the Elmore delay formula is used to estimate the worst-case delay of the bus, then there is an optimum value of the interleaving ratio at which the worst-case delay is minimized. They have also shown that an optimal ratio also exists for minimizing the peak crosstalk noise. The objective of this paper is to explore the interplay between the interleaving ratio and the signal integrity behavior of a *global* on-chip bus. It is well known [3] that the accurate modeling of these global buses requires the use of $R(f)L(f)C$ multiconductor transmission line models. Because the time-domain waveforms generated by these models may exhibit non-monotonic behavior, formulas based on the monotonicity of the step response (e.g., Elmore delay) or the positivity of the crosstalk response (e.g., noise area) cannot be used, and a methodology involving accurate $R(f)L(f)C$ extraction and simulation must be adopted for the evaluation of the bus interleaving options.

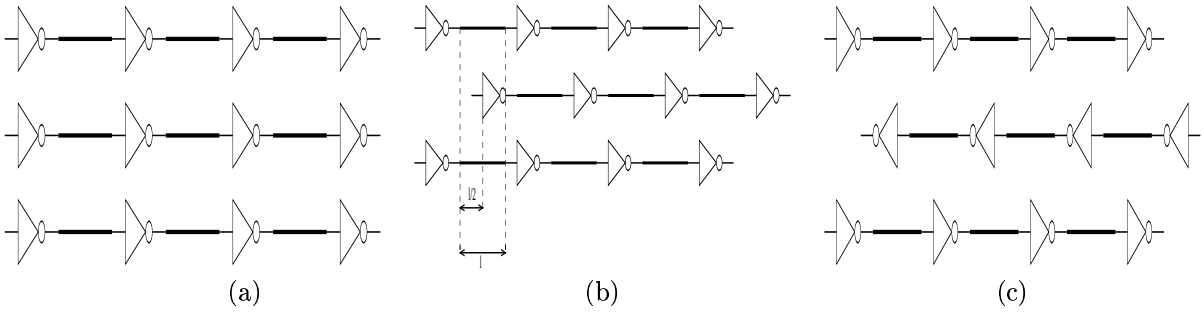

Figure 1: Three multistage bus layouts (a) Unidirectional uniform bus. (b) Unidirectional interleaved bus. (c) Bidirectional interleaved bus.

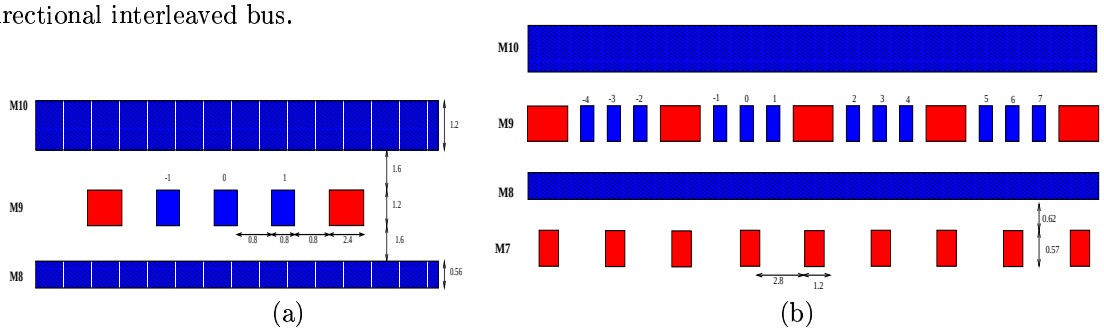

Figure 2: (a) Cross section of the 3-line bus for capacitance extraction. (b) Cross section of a 12-line bus for $R(f)L(f)$ extraction.

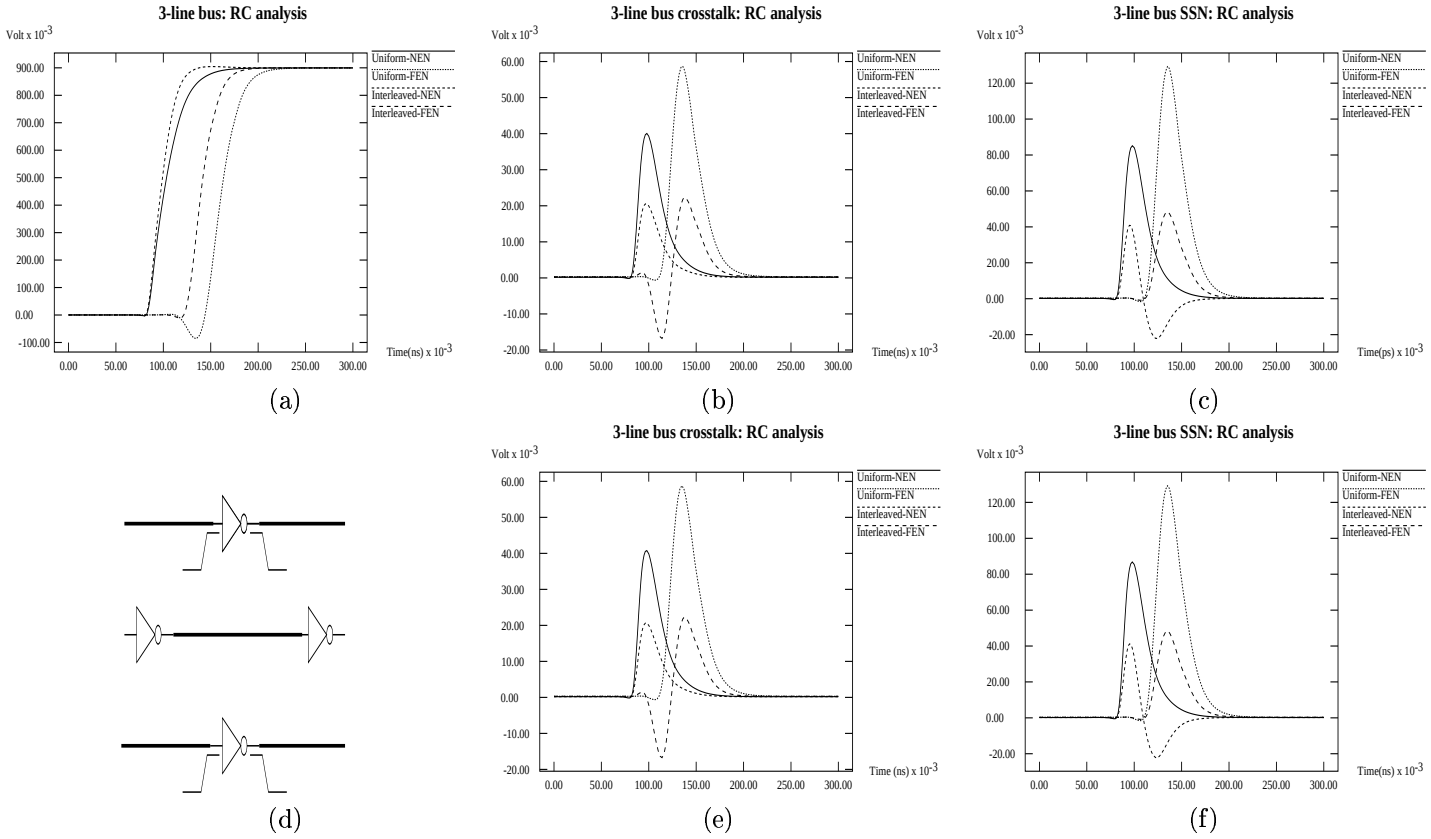

Figure 3: (a) NEN and FEN waveforms to compute the 50% worst-case delay in unidirectional uniform and interleaved buses. (b) NEN and FEN crosstalk waveforms for unidirectional uniform and interleaved buses. (c) NEN and FEN worst-case noise waveforms for uniform and unidirectional interleaved buses. (d) Explaining the impact of interleaving. (e) NEN and FEN crosstalk waveforms for bidirectional uniform and interleaved buses. (f) NEN and FEN worst-case noise waveforms for bidirectional uniform and interleaved buses.

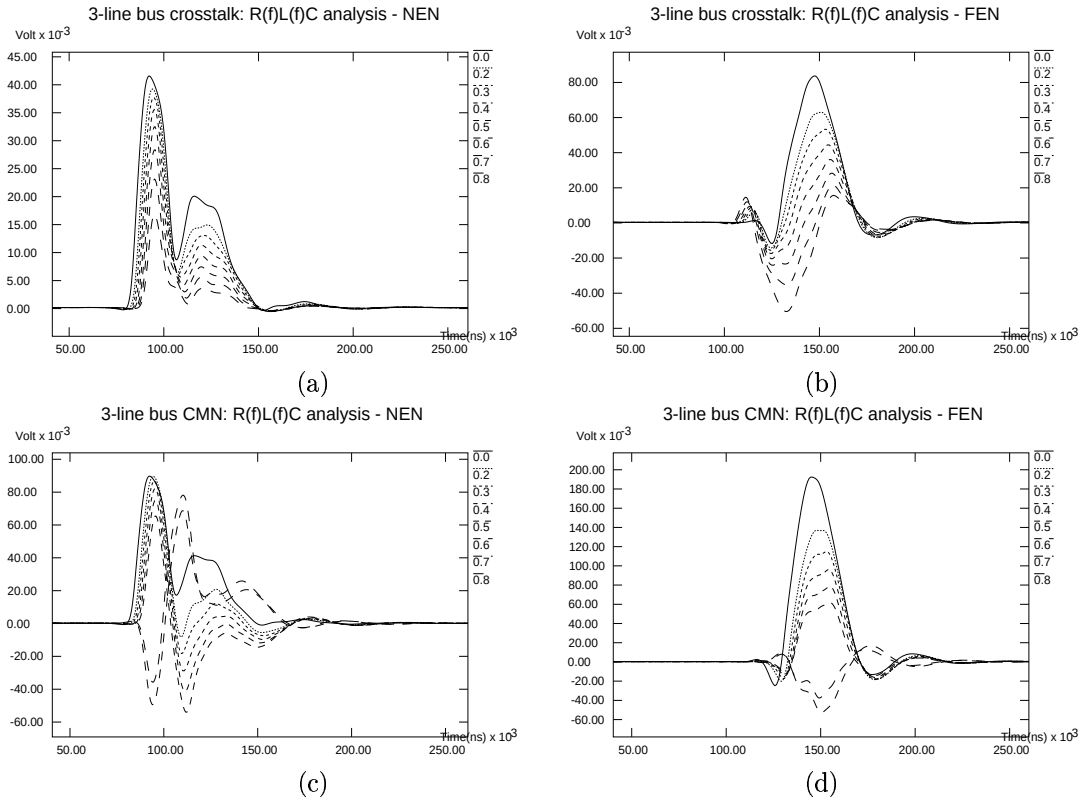

Figure 4: Crosstalk and CMN for the 3-line, 3-stage, unidirectional $R(f)L(f)C$ bus. The waveforms are parameterized with the interleaving ratio from 0.0 (no interleaving) to 0.8 (a) NEN crosstalk (b) FEN crosstalk (c) NEN CMNoise (d) FEN CMNoise.

2 Interleaving of Global Buses

The methodology described in [4] is used to extract the electrical $R(f)L(f)C$ model of the global bus. An example of a typical geometry used for the extraction of the $R(f)$ and $L(f)$ frequency-dependent tables of a 12-bit bus is given in Figure 2. The impact of interleaving on crosstalk in $R(f)L(f)C$ buses is given in Figures 4(a) and (b) for the 3-line bus of the previous section. In Figures 4(c) and (d), the result of CMN are given. The sizes of the drivers, receivers, and repeaters were kept the same as in the RC analysis case. The most important result of the $R(f)L(f)C$ crosstalk analysis is that the polarity of the peak for the FEN noise (i.e., at the input of the receiver) depends on the interleaving ratio. When the interleaving ratio is high ($\rho > 0.6$), the peak-noise becomes negative. Its arrival time is also earlier than the arrival time of the noise peak when the interleaving ratio is small ($\rho < 0.4$). Of course, the polarity change and the arrival time jitter of the peak noise will greatly impact the worst-case delay of a victim net as well as the bus CMN. For the latter, the worst-case switching pattern that maximizes CMN at the far end will be dependent on the interleaving ratio. When the interleaving ratio is large ($\rho > 0.6$), the two lines adjacent to the middle line should switch negatively. If they are switched positively as in the case for small interleaving ratios, the peak CMN on FEN will be underestimated by about 15%. This is shown in Figures 4(e) and (f). The need to change the polarity of the active signals to get the worst-case CMN is an indication of the fact that the capacitive coupling is being damped out by the interleaving as explained in the Figure 3 and that the inductive and return-path resistive couplings are becoming the dominant modes of interference between the adjacent lines. An interesting observation in the $R(f)L(f)C$ analysis is that for FEN, the crosstalk peak noise has a minimum (28.3mV) at the interleaving ratio $\rho = 0.6$. Note however that the peak crosstalk at the NEN is monotonically decreasing from 41.5mV to 16.8mV as the interleaving ratio increases from 0.0 to 0.8. If worst-case switching patterns are used, the CMN at the FEN will decrease monotonically with ρ from 136mV to 37mV while the CMN at the NEN will have a minimum of 65mV at $\rho = 0.6$. These results are still under investigation but seem to be compatible with the findings of [2]. Finally, Figures 5(a), (b), (c) and (d) show the crosstalk and CMN waveforms for the bidirectional bus. As in the unidirectional case, there is an inversion of the polarity of the FEN crosstalk peak noise as the interleaving ratio increases from 0.0 to 0.8. For

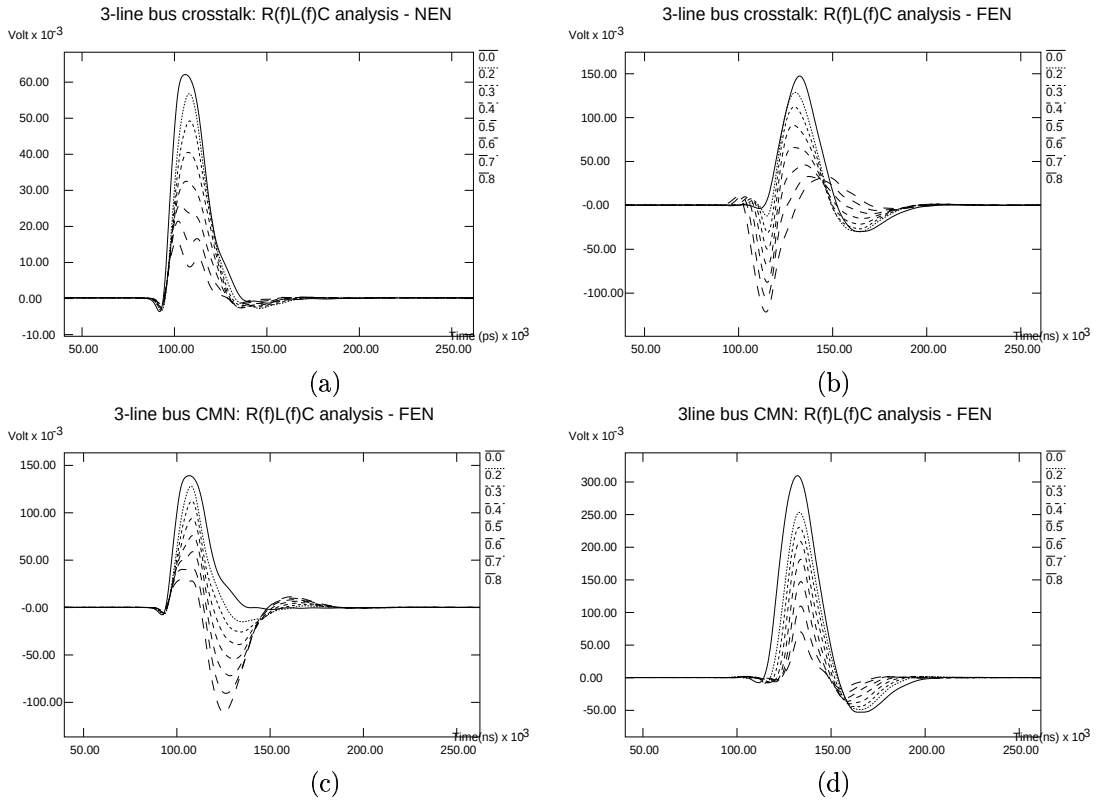

Figure 5: Crosstalk and CMN for the 3-line, 3-stage, bidirectional $R(f)L(f)C$ bus. The waveforms are parameterized with the interleaving ratio from 0.0 (no interleaving) to 0.8 (a) NEN crosstalk (b) FEN crosstalk (c) NEN CMNoise (d) FEN CMNoise.

CMN on bidirectional buses, the problematic node is the NEN. In this case, the peak CMN of the NEN has a minimum of 72mV at $\rho = 0.6$.

3 Discussion and Conclusions

Improving global bus signal integrity using repeater interleaving has been explored for both unidirectional and bidirectional buses. Accurate $R(f)L(f)C$ electrical models have been used to analyze the impact of the interleaving ratio on crosstalk and common-mode noise. Both monotonic and convex behavior for peak noise as function of interleaving ratio were found through simulation. Performance requirements impose that the global buses have as few stages as possible [3] (preferably only one!) in contrast to the local buses which can have as many as needed. We have seen in this paper that signal integrity requirements might require the insertion of interleaved repeaters *even* in global buses. When shielding and direction patterns are added to the interleaved structures, it becomes quite clear that the design space of on-chip global buses is quite large. Clearly, fast, accurate and robust CAD tools that allow the exploration of such large design space are needed.

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