RC23700 (W0508-110) August 19, 2005
Electrical Engineering

IBM Research Report

Electron Mobility Temperature Dependence of W/HfO_2 Gate Stacks: The Role of the Interfacial Layer

A. Callegari, P. Jamison, D. Neumayer, F. McFeely
IBM Research Division
Thomas J. Watson Research Center
P.O. Box 218
Yorktown Heights, NY 10598

J. Shepard
IBM Semiconductor Research and Development Center
2070 Route 52
Hopewell Junction, NY 12533

W. Andreoni, A. Curioni, C. Pignedoli
IBM Research Division
Zurich Research Laboratory
8803 Rueschlikon
Switzerland

Research Division
Almaden - Austin - Beijing - Haifa - India - T. J. Watson - Tokyo - Zurich

Electron mobility temperature dependence of W/HfO_2 gate stacks: the role of the interfacial layer

A. Callegari[1], P. Jamison[1], D. Neumayer, F. Mc. Feely[1], J. Shepard[2], W. Andreoni[3], A. Curioni[3], and C. Pignedoli[3]

IBM Semiconductor Research and Development Center (SRDC)
1) IBM T. J. Watson Research Center, P.O. Box 218, Yorktown Heights, NY 10598
2) 2070 Route 52, Hopewell Junction, NY 12533
[3]IBM Research GmbH - Zurich Research Lab, 8803 Rueschlikon, Switzerland

Abstract

Interfacial layers between the high-k dielectric and Si surface play a very important role to achieve the high electron mobilities required in the next generations of CMOS technologies. W/HfO_2 gate stacks formed on SiO_2/SiON interfacial layers subjected to various process conditions were characterized by electrical measurements such as electron mobility, inversion layer thickness and leakage reduction with respect to standard SiO_2 technology. The required high electron mobilities were obtained only when the W/HfO_2 gate stack was annealed at high temperature. Electrical data and physical analysis of the stack suggest intermixing of the HfO_2 with the interfacial layer and formation of a silicate layer which may lessen the effects of phonon scattering. Densification of the interfacial layer by spike annealing or interfacial layer stabilization by nitrogen plasma inhibits such reactions and lower electron mobilities were obtained. Also, no electrical performance advantages are seen by thinning the HfO_2 down to 1.5nm.

Introduction

Electron mobility degradation remains one of the main issues for implementing metal/high-k dielectric in CMOS technology[1,2,3]. Remote phonon scattering[4] and remote charge scattering[5] have been predicted to severely degrade mobility in NMOS fabricated with high–k materials, especially for HfO_2. Here, we review some of the work done on W/HfO_2 gate stacks. We show how mobility is largely dependent on interfacial layer preparation and stack annealing temperature. A high temperature anneal was found to be necessary to achieve high electron mobility on W/HfO_2 gate stacks. At the same time interfacial layer preparation played a crucial role to achieve these high peak mobilities. A reaction between the HfO_2 and interfacial layer rather than interfacial layer re-growth appears to be the main reason for mobility enhancement. Also, thinning of the HfO_2 to about 1.5nm did not yield to any electrical improvement.

For all these stacks, independently of mobility, charge trapping was low[6,7] and this topic will be not covered here. Mostly, we will review process-electrical data and their relation to electron mobility.

Experimental

W/HfO_2 (W~ 30 nm and HfO_2 ~25nm) gate stacks were formed by metal organic chemical vapor deposition (MOCVD) on thin (~1 nm) SiO_2 /SiON interfacial layers on bulk Si substrates. N-FETs were fabricated by using a simple non self-aligned gate process[2] to decouple the influence of process integration on mobility. 20 x 5 μm^2 FETs with channel doping of ~4 x 10^{17} B/cm^3 were used for this study. Inversion charge used in mobility measurement was determined by split capacitance-voltage (CV) method. The FETs were characterized by measurements of electron mobilities, inversion layer thickness (T_{inv}), and leakage reduction and compared to a SiON base line.

Temperature annealing of gate stack

In this first set of experiments N-FETs were fabricated using a $W/HfO_2/SiO_2$ stack. The stack was then annealed at different temperatures ranging from a low T1~400 ^oC to a high T9~1000 ^oC temperature. Electrical data are summarized in the three charts in Fig. 1. In the first chart, peak mobilities as a function of annealing temperature are compared against a poly-Si reference at about the same T_{inv}~2 nm. Electron mobilities are found to increase with annealing temperature[8]. At the highest annealing temperature peak mobility degradation is about 8% when compared with poly-Si. At high field ~1 Mv/cm no electron mobility degradation was found[8]. The second chart shows that inversion layer thickness increases with annealing temperature. So at a first instance, it appears that interfacial layer re-growth is responsible for the higher electron mobilities observed at higher annealing temperature[9,10]. This appears to be not consistent with the third chart which shows that leakage reduction also decreases with increasing annealing temperature suggesting that a reaction is likely to occur between the HfO_2 and the thin SiO_2 interfacial layer. Hf was found to diffuse in the interfacial layer by electron energy loss spectroscopy (EELS) on similar stacks[8]. Also, *"ab initio"* calculations are consistent with a silicate formation at the interface[8,11]. This is shown in Fig. 2. In the center, the dielectric constant of HfOSi is plotted against Hf content[11]. At low Hf content (left side) a stable SiO_2 structure with Hf embedded is formed and at high Hf content (right side) the stable structure is HfO_2 with Si embedded. Thus, at high annealing temperature a low Hf content stable interfacial HfSiO layer may form on the Si surface.

This silicate formation may reduce the effect of phonon scattering[4] and enabling higher electron mobilities. We should mention that a reduction of interface states was found after annealing the stack at high temperature which is consistent with the higher mobilities values. On the other hand, at low stack annealing temperatures interface states alone could not explain the severely degraded mobilities[8]. At low annealing temperatures interfacial silicates may not form. Phonon scattering or remote charge scattering rather than interface states may better explain mobility degradation[4,5].

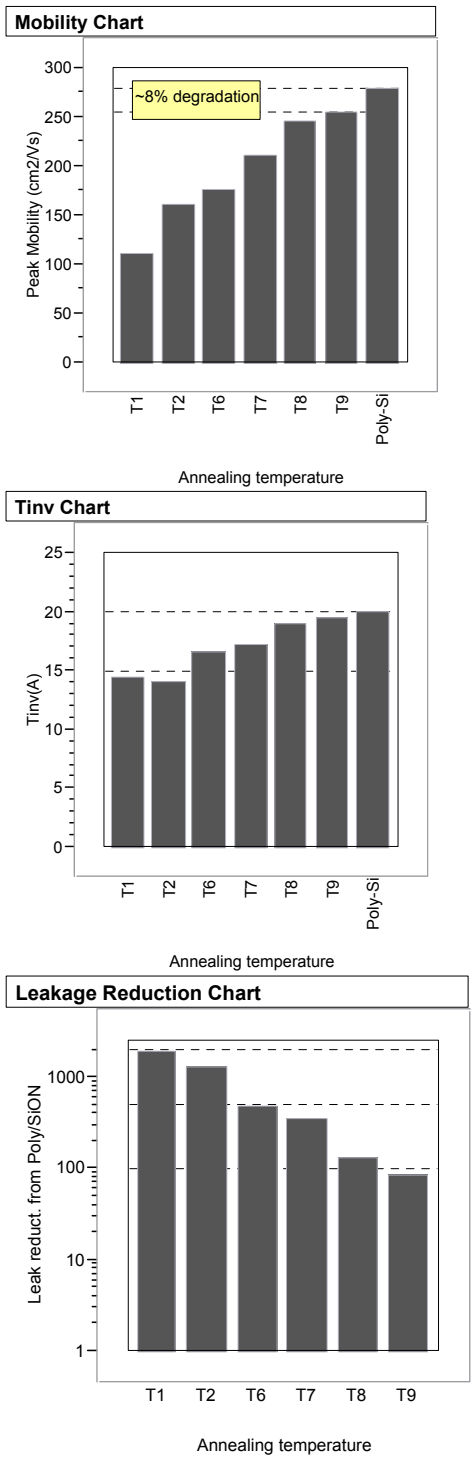

Fig. 1. Electron mobility, inversion layer thickness and leakage reduction charts of a W(=20μm) x L(=5μm) N-FET as a function of annealing temperature; T1~400 ^oC, T9~1000 ^oC. Gate stack is $W/HfO_2/SiO_2$.

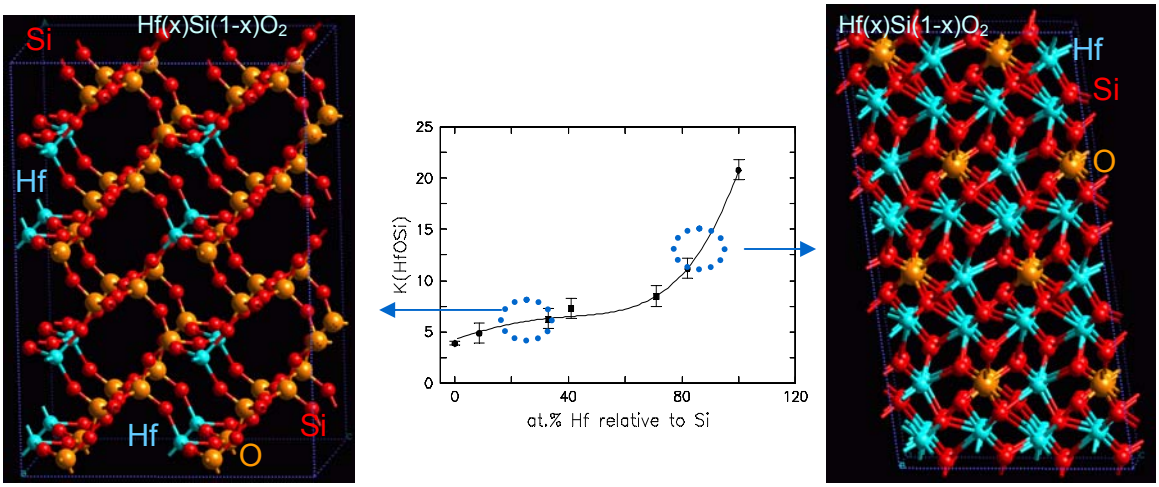

Fig. 2. Hf silicate structures which may form after a high temperature annealing of W/HfO_2/SiO_2. Center is a plot of silicate dielectric constant as a function of Hf at. % relative to Si[11]. At low Hf content the silicate structure is a SiO2 matrix with Hf embedded (left). At high Hf content the silicate structure is a HfO_2 matrix with Si embedded (right).

It can also be speculated that the reduction in leakage reduction with temperature is due to an increased HfO_2 crystallinity, thus, enhancing leakage paths through the grain boundaries. This, as it will be shown below, is not consistent with high temperature processes where the HfO_2 and interfacial layer reactions were inhibited and leakage reduction was preserved despite high-k grain growth.

Spike anneal of interfacial layer

To better understand the relation between the HfO_2 and interfacial layer on electron mobility an experiment was performed where the interfacial layer only was spike annealed at 1100 ^oC before HfO_2 deposition[12]. This was compared with a monitor wafer which did not receive the spike anneal. The spike anneal should improve interfacial layer and therefore gate stack electrical properties[12]. The interfacial layer was SiO_2 about 1.3nm thick and it was lightly nitridized.

The electrical-process summary is shown in Figs. 3 and 4. In experiment 1 (Ex1) the interfacial layer was not spike annealed, in experiment 2 (Ex2) it was spike annealed. Low T1 and T2 refer to temperatures below ~800 ^oC and high T is about 1000 ^oC. At low stack annealing temperatures peak mobilities are severely degraded (Fig. 3) as shown in the previous paragraph. Only after the stack is annealed at about 1000 ^oC a large mobility improvement is observed. There is no difference in peak mobility for Ex1 when compared with Ex2 at low annealing temperatures. Only after annealing the stack at high temperature significant differences can be observed. The sample where the interfacial layer was spike annealed showed a 28% degradation in peak mobility. T_{inv} increase from 2.0nm to 2.4 nm with annealing temperature was the same for both Ex1 and Ex2, indicating that interfacial layer re-growth was the same for both experiments. Thus, this again shows that some reaction must occur at the HfO_2/SiON interface, just not only re-growth, which is responsible for the differences in electron mobility. Leakage reduction form a poly-SiON reference also follows the same pattern as described in the previous paragraph, as the annealing temperature increases, leakage reduction decreases.

On the contrary of our expectations, peak mobility was found to be degraded when compared with a monitor where the interfacial layer was not spike annealed[12]. We can speculate that a denser and less reactive interfacial layer is formed after spike annealing which limits the intermixing with the HfO_2 and therefore the formation of the silicate layer.

To complete the electrical-process matrix threshold voltages and sub-threshold slopes are shown in Fig. 4. Note that Vt decreases for both Ex1 and Ex2 with annealing temperature. In general, in Ex2 threshold voltages are higher than in Ex1.

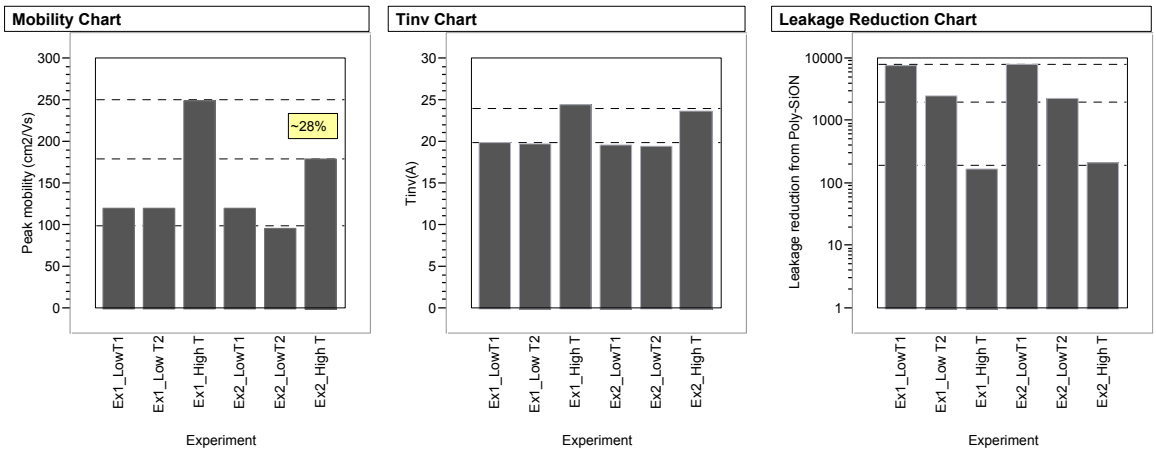

Fig. 3. Electron mobility, inversion layer thickness and leakage reduction charts of a W(=20μm) x L(=5μm) N-FET as a function of annealing temperature; LowT1~500 ^{o}C, High T~1000 ^{o}C. Gate stack is W/HfO_2/SiON. In Ex2 the SiON layer was spike annealed at 1100 ^{o}C, in Ex1 the SiON was not spike annealed.

At low annealing temperatures, Vt appears to be higher for Ex2 than for Ex1, suggesting that the differences in Vt shifts between the two experiments are due to charges located at the HfO_2 bottom interfaces since the W/HfO_2 is the same for both experiments.

Similarly, at high annealing temperature, Vt decreases in both experiments. Again, the Vt shift appears associated with the bottom interfaces (HfO_2/SiON and/or SiON/Si) since the sub-threshold slopes are also decreasing with annealing temperature indicating a reduction of interface states. Both Vt and sub-threshold slope are higher for Ex2 than for Ex1 suggesting again that the reaction between the HfO_2 and the interfacial layer is inhibited by the spike anneal of the interfacial layer. It should be noted that if mobility degradation shown in Fig. 3 (Ex2) after 1000 ^{o}C anneal is due to remote charge, this charge must be located at the bottom interfaces since the W/HfO_2 was deposited in similar fashion on both Ex1 and Ex2. This charge is also responsible the higher Vt~0.95V observed for Ex2 when compared with Ex1 (Vt~0.8V) after 1000 ^{o}C anneal (Fig. 4). Thus, attempts to use unpassivated and/or fixed charges to modulate threshold voltages can lead to significant mobility degradation. Here, charges in the HfO_2 appear not to affect mobility.

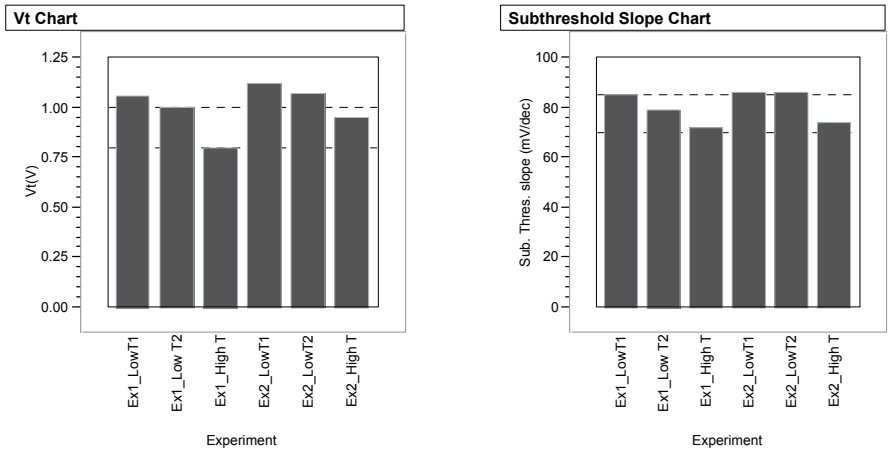

Fig. 4. Threshold voltage and sub-threshold slopes charts of a W(=20μm) x L(=5μm) N-FET as a function of annealing temperature; LowT1~500 ^{o}C, High T~1000 ^{o}C. Gate stack is W/HfO_2/SiON. In Ex2 the SiON layer was spike annealed at 1100 ^{o}C, in Ex1 the SiON was not spike annealed.

Plasma nitridation of interfacial layer

In this section will show again how important is the preparation of the interfacial layer on electron mobilities. We will also demonstrate that thinning the HfO_2 to about 1.5nm does not produce any electrical performance gain. Here, we compare a large process matrix where SiO_2 and SiON interfacial layers were radio frequency nitridized (RFN) using various plasma conditions labeled as 1_RFN, 2_RFN etch. Electrical-process results are summarized in Fig. 5. The RFN conditions were only applied to the interfacial layer and the HfO_2 oxide was not nitridized.

Two HfO_2 thicknesses, 1.5 and 2.5 nm, were investigated. All the samples shown in Fig. 5 were annealed at 1000 ^oC. Electron mobility chart shows that all the interfacial layers which received RFN conditions have reduced peak electron mobilities of about 100 cm^2/Vs despite the high temperature anneal. Only the interfacial layers which did not receive RFN (No N_15AHfO2 and No N_25A HfO2) have peak mobilities above 200 with the thinnest HfO_2 sample being ~10% degraded. The 0.4-0.5 nm interfacial layer re-growth seen in the previous sections is not observed for most of the RFN conditions (Fig. 5, T_{inv} chart). Also, there is no gain in T_{inv} by thinning the HfO_2 to 1.5nm. T_{inv} could not be sacaled below ~1.5nm for both HfO_2 thicknesses for the RFN processes used here. For the RFN_2.5nm HfO2 samples leakage reduction is about 100x higher when compared with RFN_1.5nm HfO2 samples.

Thus, there is no much gain in T_{inv} or electron mobility by thinning the HfO_2 below 2.5nm. Also, leakage reduction is much worse for the thin 1.5 nm HfO_2 film. Likely, thin HfO_2 films may not be continuous and therefore yielding to poor electrical properties.

We conclude that stabilization of the interfacial layer by RF nitridization inhibits the reaction between HfO_2 and interfacial layer, preserving low mobility, preventing interfacial layer re-growth and keeping higher leakage reduction. Note that after high temperature annealing, leakage reduction is much higher for interfacial layers which received RFN when compared with interfacial layers which did not receive RFN (Figs 1 and 5). Since the HfO_2 film is the same in both experiments, and likely grain formation, the difference in leakage reduction at high annealing temperature is probably related to different stack interfacial compositions and not to leakage paths through grain boundaries.

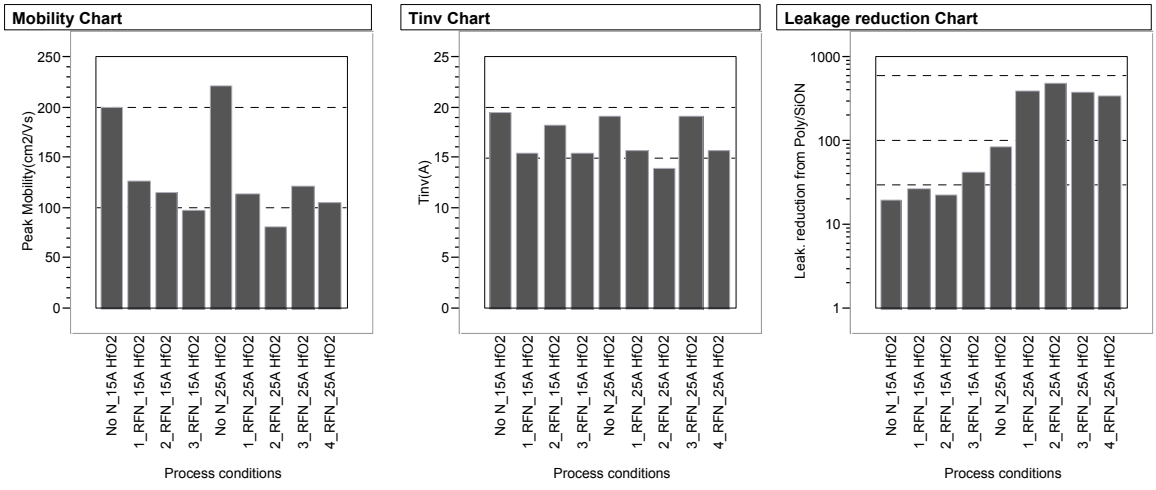

Fig. 5. Electron mobility, inversion layer thickness and leakage reduction charts of a W(=20μm) x L(=5μm) N-FET as a function of various RF nitridation processes of interfacial layer only. The gate stack was annealed at 1000 ^oC. Data are shown for two different HfO_2 thicknesses, 1.5 and 2.5 nm.

Summary

In summary, electron mobility degradation in W/HfO_2 gate stacks is largely dependent on interfacial layer formation on the Si surface. A reaction between the interfacial layer and the HfO_2 and the formation of a silicate layer adjacent the Si surface after high temperature annealing can explain the high electron mobilities. This silicate layer may lessen the effect of phonon scattering enabling high electron mobility. If such reaction is somewhat inhibited by stabilizing the interfacial layer by spike anneal or by plasma nitridation degraded electron mobilities are obtained.

References

1. V. Ku, R. Amos, A. Steegen, C. Cabral, V. Narayanan, P. Jamison, P. Nguyen, Y. Li, M. Gribelyuk, Y. Wang, J. Cai, A. Callegari, F. McFeely, F. Jamin, K. Wong, E. Wu, A. Chou, D. Boyd, H. Ng, M. Ieong, C. Wann, R. Jammy, and W. Haensch ", *Extended Abstracts, SSDM*, Tokyo Japan, (2003) 730.
2. A. Callegari, P. Jamison, B.H. Lee, D. Neumayer, V. Narayanan, S. Zafar, E. Gousev, C. D'Emic, D. Lacey, M. Gribelyuk, C. Cabral, A. Steegen, V. Ku, R. Amos, Y. Li, P. Nguyen, F. Mc. Feely, G. Singco, J. Cai, S-H Ku, Y.Y. Wang, C. Wajda, D. O'Meara, H. Shinriki, and T. Takahashi, *Extended Abstracts, SSDM*, Tokyo Japan, (2003) 808.
3. L. Ragnarson, W. Tsai, A. Kerber, P.J. Chen, E. Cartier, L. Pantisano, S. De Gendt, and M. Heyns, *Extended Abstracts, SSDM*, Tokyo Japan, (2003) 46.
4. M. V. Fischetti, D. Neumayer, and E. Cartier, *J. Appl. Phys.,* **90**, (2001) 4587.
5. M. Hiratani, S. Saito, Y. Shimamoto and K. Torii, *J. J. Appl.Phys.,* **41**, (2002) 4521.
6. A. Callegari, P. Jamison, D. Neumayer, V. Narayanan, S. Zafar, D. Lacey, M. Gribelyuk, R. Amos, F. Mc. Feely, C. Wajda, D. O' Meara, H. Shinriki, and T. Takahashi, *Proc. WoDiM 2002*, Edited by IMEP, Grenoble France, (2002) 57.
7. E. P. Gusev, V. Narayanan, S. Zafar, C. Cabral Jr., E. Cartier, N. Bojarczuk, A. Callegari, R. Carruthers, M. Chudzik, C. D'Emic, E. Duch, P. Jamison, P. Kozlowski, D. La Tulipe, K. Maitra, F. R. McFeely, J. Newbury, V. Paruchuri, and M. Steen, *IEDM 2004*, S. Francisco Ca., (2004) 729.
8. A. Callegari, P. Jamison, E. Cartier, S. Zafar, E. Gusev, V. Narayanan, C. D'Emic, D. Lacey, F. Mc. Feely, R. Jammy, M. Gribelyuk, J. Shepard, W. Andreoni, A. Curioni, C. Pignedoli, *IEDM 2004*, S. Francisco Ca., (2004) 825.
9. M. Hiratani, S. Saito, Y. Shimamoto, S. Tsujikawa, Y. Matsui, O. Tonomura, K. Torii, J. Yugami, and S. Kimura, *Extended Abstracts, SSDM*, Tokyo Japan, (2003) 700.
10. S. Zafar, *unpublished*.
11. A. Callegari, E. Cartier, M. Gribelyuk, H.F. Okorn-Schmidt and T. Zabel, "Physical and electrical characterization of Hafnium oxide and Hafnium silicate sputtered films", *J. Appl. Phys.* **90**, (2001) 6466.
12. A. Callegari, P. Jamison, S. Zafar, D. Lacey, F.R. McFeely, J. Shepard, E.P. Gusev, E. Cartier, and R. Jammy, "Electron mobility dependence ofW/HfO_2 gate stacks on interfacial layer preparation", to be published, *ECS,* Quebec City Ca, 2005