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Dynamic Circuit Techniques Using Independently Controlled Double-Gate Devices

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Introduction

Increased leakage in scaled technologies limits the robustness of dynamic circuits, especially the wide OR-style dynamic gates commonly used in high-speed designs. Strong keepers are needed for the precharge state or after the completion of evaluation to compensate for leakage and hold the correct state of the dynamic node. Strong keepers, however, cause aggravated contention and speed degradation during evaluation. Previously, a conditional keeper technique was proposed where only a fraction of the keeper strength is turned on at the onset of evaluation phase while the full strength is enabled after a delay time [1]. Alternatively, a programmable keeper technique where the effective keeper width tracked the on-die leakage was proposed to compensate for die-to-die variation [2]. Nevertheless, employment of extra devices increases the logic gate area as well as the capacitance at the dynamic node. Charge sharing is another concern which causes voltage droop in the dynamic node and degrades the noise margin. A common method to prevent the charge sharing effect consists of charging the intermediate node in a stacked configuration to full rail before evaluation. While the technique is effective, the intermediate node precharge device adds capacitance to that node and increases the circuit area. To address these issues with continued device scaling requires diligent technology circuit co-design efforts.

Circuit Design with Double-Gate Devices

Independent biasing of the front and back gate in double-gate (DG) technologies can be exploited to boost the performance and reduce the number of transistors in implementing logic functions [3-4]. In this paper, keeper schemes utilizing independent front and back gate control in DG devices are presented to achieve improved speed, noise margin, and reliability in dynamic circuits. These schemes provide the conditional keeper function with fewer devices, effectively reducing area and capacitance. Also introduced is a method that utilizes the back-gate device of a logic transistor as the precharge device for the intermediate stacked node, to prevent charge sharing, thereby reducing the capacitance and area of the intermediate node precharge device. Finally, a static keeper and footer method using the asymmetrical DG devices is described taking advantage of the unique front and back channel current characteristics.

Conditional Keepers

Fig. 1 shows the schematic diagram of a conditional keeper using independently biased DG PFET. The "slow mode" pin can be either a test mode signal that preserves the dynamic node state during low-frequency debug, or an at-speed delayed clock that turns on the front gate keeper after a successful evaluation. Figs 2 (a) and (b) depict the device structures for asymmetrical and symmetrical DG devices, respectively.

For symmetric DG devices, the strengths of the front and back gate are equal when only one gate is turned on. When both channels are on (DG mode), the total current in the front and back channel increases to more than two times higher, compared with the one-gate-on case due to the ideal subthreshold slope in the DG mode of operation. At lower V_{DD}'s, the DG mode current improvement becomes larger as the effect of gate-to-gate coupling becomes more significant [5]. Thus, this dynamic circuit technique is viable for voltage scaling, considering the timing, current drive, and device strength requirements. Two alternative circuit configurations are shown in Figs 3 (a) and (b), both of which delay the turn-on of the front gate keeper device. These schemes utilize a single DG PFET to perform the functions of both weak keeper and strong delayed-on keeper, thus reducing the capacitance and area associated with multiple keeper devices to reduce contention, improve speed, area, noise immunity, and circuit robustness.

The unique features (Fig. 4) of asymmetrical DG device structure can be preferentially utilized in circuit design. When only the back gate is biased and the front gate is grounded, the back channel current is more than one-order-of-magnitude lower than the predominant front-channel current due to the ~1V higher threshold voltage for p+ gate [5]. When both the front and back channel are turned on, the front-channel current is enhanced by approximately 2 times at V_{DD}=1V, due to gate-to-gate coupling, compared with the case when only the front gate is on. In the circuit of Fig. 1 for the asymmetrical DG devices, the front channel with the off back gate serves as a weak keeper. The back gate is turned on to increase the front channel current only when a strong keeper is desired. Thus, the circuit provides the keeper function with its strength conditionally modulated by the back gate. Figs 5 (a) and (b) show the MEDICI [6] simulation results for the fast and slow mode, with heavy and light output load, respectively. A significant slow-down of the evaluate edge in the slow mode operation is observed, thereby demonstrating the performance advantage of the proposed method. The difference between the slow and fast mode operation is larger in the case of light output load because of the more pronounced difference in effective drive current and hence the transitional slews.

Charge Sharing Mitigation

Fig. 6 depicts a scheme, using symmetric DG devices, where the back gate (BG) of transistor A1 is

used as the precharge device for the intermediate stacked node "int" to prevent charge sharing. The scheme reduces the capacitance and area of the intermediate node pre-charge device, thus effectively circumvents charge sharing and conserves area with the intervention of signal "clock_b". The insert of Fig. 6 compares the dynamic node "dyn" waveforms, under a severe charge sharing condition during evaluation, with and without the anti-charge sharing back gate device. The use of anti-charge sharing back gate device prevents the collapse of dynamic node voltage and catastrophic logic fault.

Static Keepers and Footers

If a dynamic stage uses a static keeper instead of the feedback half latch, the leakage current through the always-on keeper would be unacceptably high for conventional bulk silicon, PD/SOI, or symmetrical DG technologies. In contrast, the asymmetrical DG PFET incorporates the function of two PFETs: the front gate with a strong front channel current can be connected to the clock to perform the reset function while the weak back gate, at a 1/10th - 1/20th drive strength, can be used as a static keeper without excessive leakage current. Fig. 7 shows a domino stage using asymmetrical DG devices where p1 replaces both the precharge and keeper device. The front gate precharge device of p1 is connected to the clock with only half the gate loading and no performance penalty. The back gate keeper device of p1 is tied to constant (hard wired for all modes, Fig. 7) or conditional (only in active mode to further reduce leakage, Fig. 8) ground. When the front gate is off during evaluation, the back gate becomes a keeper. MEDICI simulation results showing well behaved state transitioning are presented in Fig. 9. It is observed that $I_{on(n1)}/I_{on\_strong(p1)}$=3.85; $I_{on\_strong(p1)}/I_{on\_weak(p1)}$=14.50; $I_{on\_weak(p1)}/I_{off(n1)}$=1.84x$10^4$. The circuit functions with a wide noise margin as shown in two examples of noise event simulations (Fig. 10) for both precharge and evaluate. The static keeper can maintain or restore the desired V_{DD} level. During burn-in and debug mode, there is an additional option of keeping clock high. Thus, the circuit functions as a pseudo-NMOS gate at low frequencies.

Similarly, when designing a footer device, we can exploit the asymmetrical DG device feature: the front gate with strong coupling to the front channel determines the on/off state; and the back gate with weak coupling to the channel controls the strength of the front channel. When the footer front and back gate are clock tied (Fig. 7), faster reset and lower leakage are achieved for the on and off state, respectively. Alternatively, the footer back gate can be tied to constant or conditional V_{DD} for clock load reduction (Fig. 8).

Conclusion

In summary, conditional keeper, charge sharing prevention, and clock load reduction techniques for symmetrical and asymmetrical DG devices have been presented. Performance benefit, noise immunity, area and power efficiency can be achieved when technology features are judiciously utilized in the design of dynamic circuits.

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[5] K. Kim and J. G. Fossum, "Double-gate CMOS: symmetrical versus asymmetrical gate devices," IEEE Trans. Electron Devices, vol. 48, 2001, pp. 294-299.
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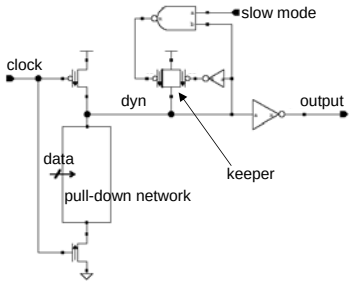

Fig. 1 Conditional keeper using independently controlled front and back gate double-gate PFET. The "slow mode" pin can be an at-speed clock or a low-frequency control signal.

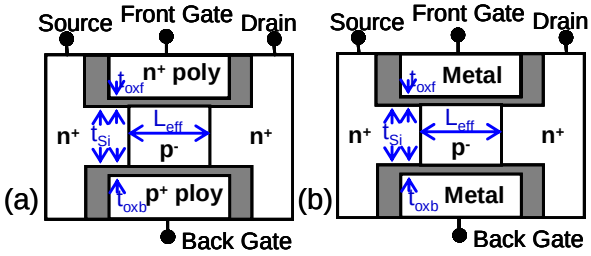

Fig. 2 Double-gate device cross sections (L_{eff} = 25 nm, t_{oxf} = toxb = 1 nm, t_{Si} = 10 nm): (a) asymmetrical double-gate NFET. For PFET, the front gate is p+ and the back gate is n+. (b) symmetrical double-gate NFET.

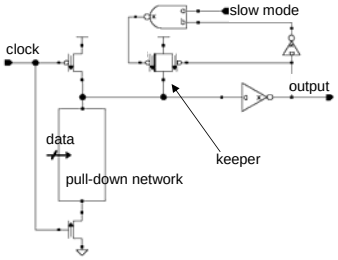

Fig. 3 (a) Alternative conditional keeper topology using a DG PFET

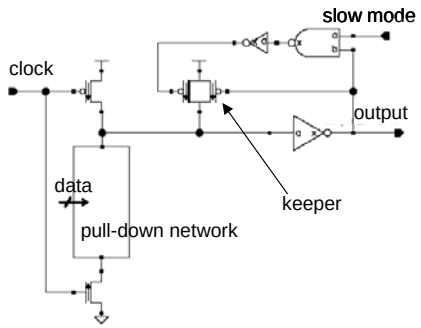

Fig. 3 (b) Alternative conditional keeper topology using a DG PFET

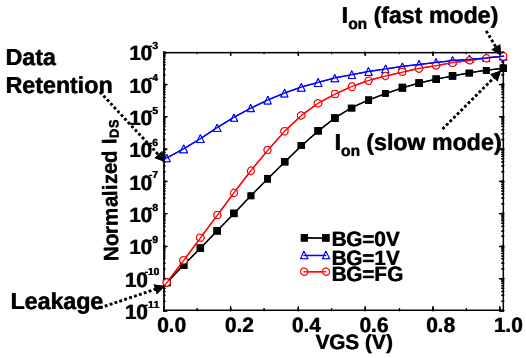

Fig. 4 MEDICI-predicted drain current versus front gate voltage for asymmetrical DG NFET for three different bias conditions. The gate terminal can be connected flexibly in design to meet the drive strength, leakage reduction, or data retention requirements.

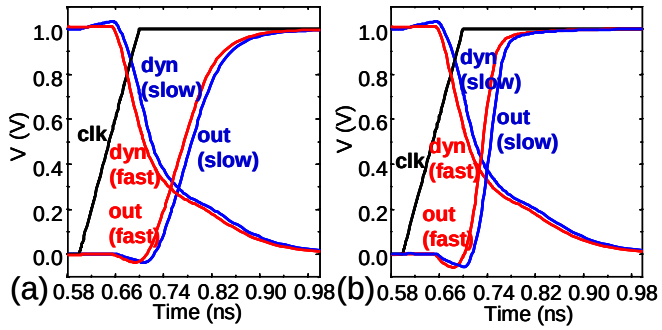

Fig. 5 MEDICI simulation for (a) heavily loaded output: clock-up to dyn-down = 55 ps (fast mode), 70 ps (slow mode), and clock-up to output-up = 123 ps (fast mode), 130 ps (slow mode), and (b) lightly loaded output: clock-up to output-up = 83 ps (fast mode), 100 ps (slow mode).

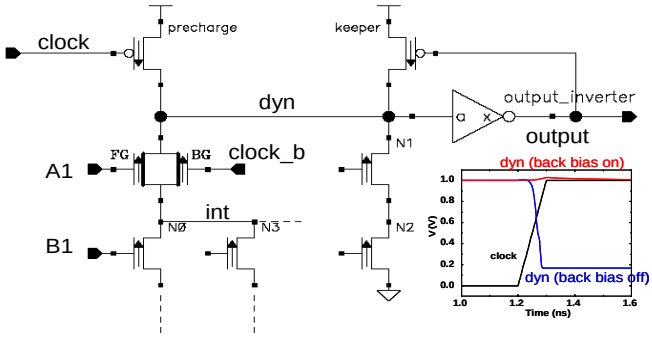

Fig. 6 Schematic diagram showing the precharge of internal stacked node "int" using back gate of the logic transistor A1. The insert shows the well behaved and collapsed dynamic node waveforms with and without the intervention of the back gate anti-charge sharing device, respectively.

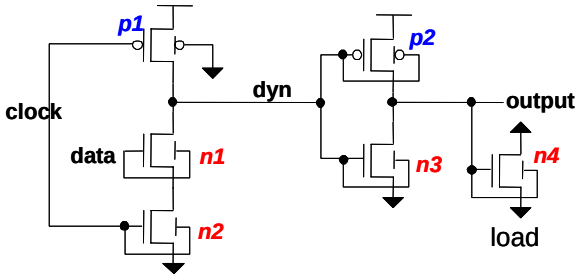

Fig. 7 Schematic diagram for a shared precharge/keeper implementation using asymmetric DG devices, where the front gate of p1 is the precharge device and back gate of p1 is the weak always-on static keeper

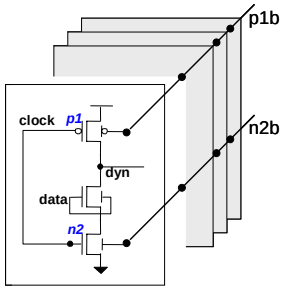

Fig. 8 Precharge/keeper device back gate control for leakage power and/or clock load reduction. The common node p1b is at ground and V_{DD} for active and standby mode, respectively. The common node n2b is at V_{DD} and ground for the active and standby mode, respectively.

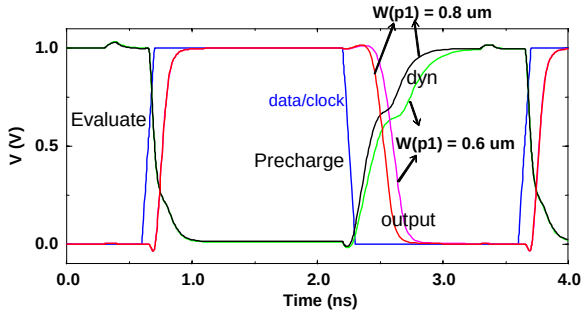

Fig. 9 MEDICI results showing the waveforms for data, clock, dyn, and output nodes for two precharge/keeper device (p1) widths of 0.6 and 0.8µm. Data and clock arrival times are assumed to be perfectly aligned in simulation.

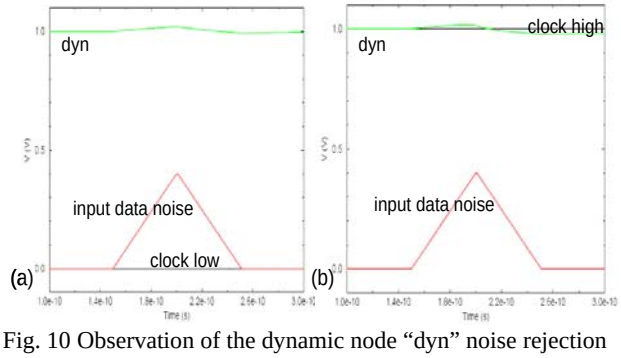

Fig. 10 Observation of the dynamic node "dyn" noise rejection behavior for the circuit of Fig. 7 during the (a) precharge and (b) evaluate interval, respectively. Node "dyn" recovers to V_{DD} in both cases in the presence of the precharge/static keeper device.