RC23737 (W0510-023) October 7, 2005
Other

IBM Research Report

Silicon Microchannel Cooling for High Power Chips*

Evan G. Colgan, Bruce Furman, Mike Gaynes, Nancy LaBianca, John Magerlein, Robert Polastre
IBM Research Division
Thomas J. Watson Research Center
P.O. Box 218
Yorktown Heights, NY 10598

R. J. Bezama, Rehan Choudhary, Ken Marston, Hilton Toy, Jamil A. Wakil
IBM East Fishkill
Hopewell Junction, NY

Roger Schmidt
IBM Poughkeepsie
Poughkeepsie, NY

Research Division
Almaden - Austin - Beijing - Haifa - India - T. J. Watson - Tokyo - Zurich

Silicon Microchannel Cooling for High Power Chips

Evan G. Colgan, PhD **Bruce Furman, PhD** **Mike Gaynes** **Nancy LaBianca**

John Magerlein, PhD **Robert Polastre** **R.J. Bezama, PhD** **Rehan Choudhary**

Ken Marston, PE **Hilton Toy** **Jamil A. Wakil, PE** **Roger Schmidt, PhD, PE**
Member ASHRAE

Received October 7, 2005; accepted June 6, 2006

In this work, single-phase Si microchannel coolers have been designed and characterized for cooling very high power density chips in single-chip modules (SCMs) in a laboratory environment. The average heat transfer coefficient was determined for a wide range of microchannel designs. Through the use of multiple heat exchanger zones and optimized cooler fin design, an average unit thermal resistance of 16.2°C·mm^2/W between the chip surface and the inlet cooling water was demonstrated for an Si microchannel cooler attached to a chip with Ag epoxy in an SCM. Very good uniformity from SCM to SCM (±2%) and within an SCM (±5%) was achieved. Further, cooling of a thermal test chip with a microchannel cooler bonded to it and packaged in an SCM was also demonstrated for a chip power density greater than 400 W/cm^2. Coolers of this design should be able to cool chips with average power densities of 500 W/cm^2 or more.

INTRODUCTION

More than twenty years ago, Tuckerman and Pease (1981) first described the use of microchannel cooling for very high power densities of about 800 W/cm^2. However, the coolers could not be fabricated easily and the pressure drops were very high. As chip power densities are now increasing beyond air cooling limits, it is necessary to address a number of practical issues for implementing microchannel cooling. Recent progress in high-rate deep reactive ion etching (DRIE) of Si (Laermer and Urban 2003) has greatly simplified the fabrication of microchannel coolers from silicon. Also, a number of methods for reducing the pressure drop have been reported, including subdividing the flow into multiple heat exchanger zones with shorter channel lengths (Harpole and Eninger 1991) and manifold designs with large cross-sectional areas (i.e., areas equal to or larger than the channel cross-sectional area) (Webb 2003). In addition, staggered fins (i.e., fins that are offset or staggered fin segments) in microchannel coolers have been found to increase the heat transfer coefficient compared to continuous fins (Kishimoto and Sasaki 1987; Colgan et al. 2005).

For practical implementation of microchannel cooling, it is essential that the cooler be easy to integrate with the chip packaging. An earlier study (Colgan et al. 2005) that described results from the testing of individual Si microchannel coolers with both staggered and continuous fins

Evan G. Colgan, **Bruce Furman**, and **John Magerlein** are research staff members, **Mike Gaynes** is a senior technical staff member, and **Nancy LaBianca** and **Robert Polastre** are advisory engineers with IBM T.J. Watson Research Center, Yorktown Heights, NY. **R.J. Bezama** is a distinguished engineer, **Rehan Choudhary** is a staff engineer, and **Ken Marston**, **Hilton Toy**, and **Jamil A. Wakil** are advisory engineers with IBM East Fishkill, Hopewell Junction, NY. **Roger Schmidt** is a distinguished engineer with IBM Poughkeepsie, Poughkeepsie, NY.

demonstrated a practical integration method for packaging microchannel coolers into single-chip modules (SCMs) and presented measurement results for these packaged coolers demonstrating a repeatable cooling capability of 300 W/cm^2. A cross-sectional image of such SCM structures is shown in Figure 1. This structure consists of a two-piece manifold block, molded from high-temperature plastic, that transforms a single inlet and outlet into alternating inlet and outlet zones. A flexible gasket between the manifold block and the Si microchannel cooler provides mechanical decoupling. In the detailed image of the microchannel cooler, the channels along with a fluid via are visible. The 18.5 × 18.6 mm thermal test chip was mounted with solder balls onto a ceramic module and underfilled. The microchannel cooler was bonded to the thermal chip using an Ag epoxy (white in Figure 1). The bottom perimeter of the manifold block was bonded to the ceramic package with an adhesive.

High-performance chips are typically mounted active side down on a first-level package substrate using an area array of solder balls. The assembly is subsequently attached to a printed circuit board or second-level package by a solder ball grid array (BGA). For normal BGA assembly processes, the microchannel cooler and associated manifold are designed to be compatible with a eutectic (~225°C) or Pb-free (~245°C–260°C) reflow and the total weight low enough to permit self-alignment during reflow. With chips mounted active side down, the back sides of the chips are available for the cooling solution. Due to the high cost of high-performance processor chips, it is not practical to form the microchannels directly on the back surface of the chip. Instead, a separate microchannel cooler is bonded to the back of the chip with materials having as low a thermal resistance as possible. If the microchannel cooler is fabricated from silicon, a low thermal resistance, rigid bonding means such as silver-filled epoxy or solder can be used. If a copper microchannel cooler were used (Prechtl and Kurtz 2004), accommodating the different thermal expansion coefficients of Si and Cu would require a compliant thermal interface material, possibly limiting the overall thermal performance.

This work demonstrates the feasibility of extending the thermal capability of Si microchannel coolers to 400 W/cm^2 or higher in a laboratory environment while preserving the integration method of the previously described assembly (Colgan et al. 2005). The following section describes the design, fabrication, and testing of a wide variety of individual Si microchannel coolers and microchannels packaged in SCMs designed for high thermal performance. The test results for the individual Si microchannel coolers are then analyzed in detail to determine the average heat transfer coefficient and verify consistency between the measured thermal performance of a given microchannel design and the expected thermal performance from theory. The

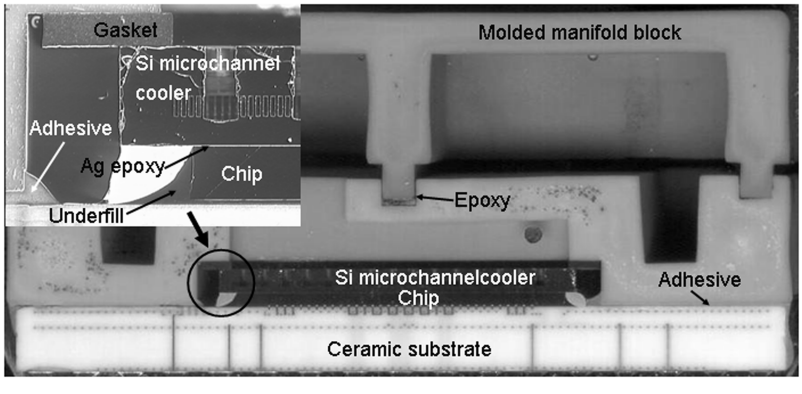

Figure 1. Cross-sectional images of a complete microchannel single-chip module (SCM).

variation in performance within a group of 55 SCMs is then evaluated. Next, results are presented on higher performance microchannel designs where cooling a power density of > 400 W/cm^2 was demonstrated for a thinned thermal chip packaged with a microchannel cooler in an SCM. The detailed analysis was only performed for the individual microchannel coolers because for the SCMs the measured thermal resistance also includes contributions from the Ag epoxy and the thermal chip, which are difficult to separate in a consistent manner.

MICROCHANNEL COOLER DESIGN, FABRICATION, AND TESTING

The microchannel coolers used in this work were made by bonding together a manifold and a channel chip, each 20 × 20 mm in size with a 0.7 mm wide seal region around the perimeter (see detail in Figure 1). The manifold chip contained zigzagged rows of fluid through vias, and distribution channels were etched ~0.25 mm deep on the side of manifold chip that was bonded to the channel chip to help redistribute the flow. Also, the microchannel fin segments were removed from the regions under the fluid vias to aid further in the redistribution of the flow.

A three-dimensional rendering of part of an assembled microchannel cooler is shown in Figure 2, where the manifold chip is on top and is shown semi-transparent. In operation, alternate zigzagged rows of fluid vias are used as inlets and outlets (see Figure 2), where the distance between the corresponding inlet and outlet fluid vias is about 3.1 mm. In operation, there were four rows of inlet and three rows of outlet fluid vias that alternated and extended across the active area of the cooler. This configuration divided the microchannel cooler into six parallel-fed heat exchanger (HE) zones, which reduces the pressure drop. The fluid vias in the manifold chip were formed as zigzagged arrays of circular openings instead of elongated slots to reduce the likelihood of the manifold chips breaking during fabrication and assembly.

All the microchannel coolers were fabricated using photolithography and Si DRIE. The unpackaged microchannel coolers with resistors on the backs of the channel chips, described in the "Microchannel Cooler Results and Discussion" section, were fabricated from 200 mm wafers ~0.725 mm thick and were bonded together with an adhesive. The microchannel coolers packaged in SCMs, described in the "Single-Chip Module Results" section, were fabricated from 150 mm wafers and were fusion bonded together. For the results described in the "Microchannel Cooler Results and Discussion" section, a large range of different fin and channel configurations were fabricated. The general features of the microchannel coolers used in both sections are summarized in Table 1. Figures 3a–3d illustrate some of the designs used for the

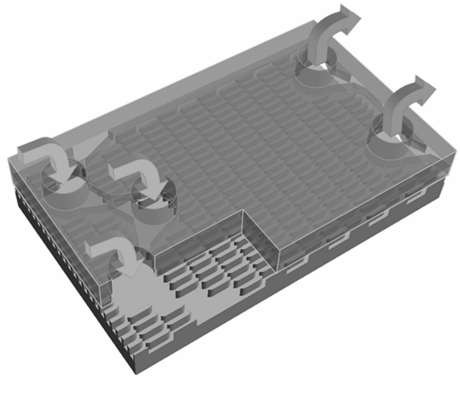

Figure 2. Three-dimensional rendering of a portion of an assembled microchannel cooler having six heat exchanger zones.

Table 1. Configuration of Si Micochannel Coolers Used in This Work

I.D.	Pitch (μm)	Channel Width (μm)	Fin Type	# HE Zones
Unpackaged Si Microchannels				
P50/C20/Cont	50	20	Continuous	6
P50/C20/Stag	50	20	Staggered	6
P50/C25/Cont	50	25	Continuous	6
P50/C25/Stag	50	25	Staggered	6
P60/C25/Cont	60	25	Continuous	6
P60/C25/Stag	60	25	Staggered	6
P60/C30/Cont	60	30	Continuous	6
P60/C30/Stag	60	30	Staggered	6
P75/C35/Stag	75	35	Staggered	6
P75/C40/Stag	75	40	Staggered	6
P75/C45/Stag	75	45	Staggered	6
P100/C50/Stag	100	50	Staggered	6
P100/C60/Stag	100	60	Staggered	6
Si Microchannels Packaged in SCMs				
P50/C20/Stag	50	20	Staggered	31
P60/C35/Stag	60	35	Staggered	6
P75/C45/Cont	75	45	Continuous	6
P75/C45/Stag	75	45	Staggered	6
P100/C60/Cont	100	60	Continuous	6
P100/C60/Stag	100	60	Staggered	6

unpackaged microchannel coolers. Throughout the paper, microchannel coolers will be referred to in terms of their dimensions, such as by "P50/C20/Cont.," which indicates a cooler with a 50 micron channel pitch, a nominal channel width of 20 microns, and continuous fins, or by "P75/C40/F500" for a 75 micron pitch cooler with a nominal channel width of 40 microns and 500 micron long staggered fins. In some cases, the fin length will not be indicated but "Stag" will be used to indicate staggered fins.

For the unpackaged microchannel coolers, due to process bias, the actual channel width was greater than the nominal width and the process bias systematically increased with the nominal channel width. For example, the process bias was about 7 microns with a 20 micron nominal channel width and about 14 microns with a 60 micron nominal channel width. The manifold and channel chips were joined together using a very thin (5–15 micron average thickness) adhesive layer applied to the manifold chip. The depth of the etched channels ranged from 150 to 220 microns and was systematically shallower for the narrower channels than for the wider channels. The deviation of the channel sidewall from vertical increased as the channel width increased. In some cases, this could have reduced the fin efficiency due to the reduced width at the base of the fin. For evaluating the microchannel cooler performance, the channel width was measured halfway between the top and the bottom of the channel and the depth of the channel was adjusted to allow for the average adhesive layer thickness.

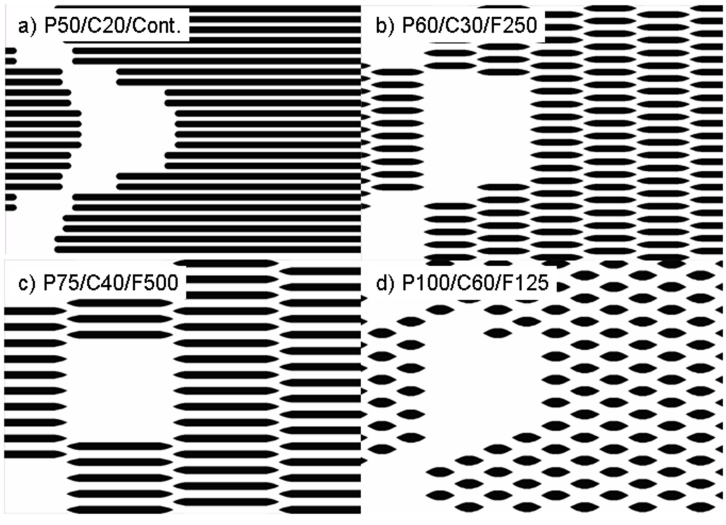

Figure 3. Examples of some of the microchannel designs tested with pitches between 50 and 100 microns.

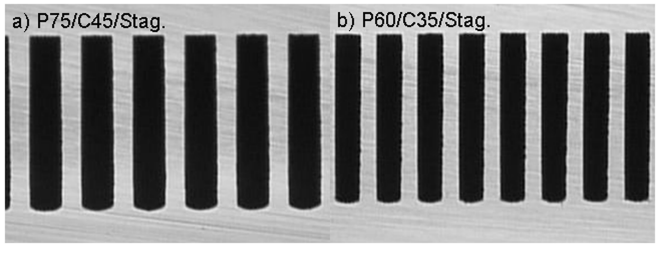

Figure 4. Cross-sectional images of some fusion-bonded microchannel coolers of the type used in SCMs.

The microchannel coolers that were integrated into SCMs were very similar to those just described but were fabricated on 150 mm wafers between 0.450 and 0.675 mm thick, and the manifold and channel chips were fusion bonded together rather than joined with adhesive. Most of the work used four different cooler designs, either continuous or staggered fins with either a 75 micron pitch and a 45 micron actual channel width or a 100 micron pitch and a 60 micron actual channel width. The channel depths were about 254 and 262 microns for the two different pitches.

Cross-sectional images of some representative fusion-bonded coolers are shown in Figure 4, where the manifold chip is located above the channel chip. Note that the sidewalls are nearly perfectly vertical. The depth in both cases was close to 250 microns, though the wider channels were slightly deeper. The dimensions in the cooler identifiers for the packaged microchannel coolers are actual dimensions, not nominal dimensions.

For thermal testing of the unpackaged microchannel coolers, a heater and a temperature sensor resistor were formed by etching a 0.5–1.5 micron thick copper film on a thin insulator layer on the back surface of the channel chip. Two contact pads were used for powering the heater

resistor, and two other contact pads were used for connecting to the sensor resistor. The heater resistor was designed to cover as much of the 20 × 20 mm channel chip area as possible. The sensor resistor was located within the 0.2 mm wide gaps between the serpentines of the heater resistor. Additional details of the structure can be found in Colgan et al. (2005).

The samples were measured using a test station where the water flow could be varied while measuring the differential pressure across the microchannel cooler, the inlet and outlet water temperatures, the sensor resistor value, and the power applied to the heater resistor. The sensor resistor was calibrated by varying the water inlet temperature while measuring the sensor resistor value. The calibration was used to determine the heater plane average temperature T_j. A similar test station was used for testing the SCMs. For the SCM measurements, the differential pressure measurements were not corrected for the ~4 kPa pressure drop measured in the test station when the SCM was replaced with a short hose segment. The thermal test chip in the SCM was 18.5 × 18.6 mm in size and the powered area was 3 cm^2. For both test stations, the uncertainty in the flow measurements was about ±0.05 lpm, the uncertainty in the pressure measurements was about ±0.15 kPa, and the uncertainty in the inlet and outlet temperature measurements was about 0.5°C. The uncertainty in the measured thermal performance in both sections is ≤5% and is due mainly to the uncertainty in the sensor calibration and the small amount of heat that does not flow through the microchannel cooler.

MICROCHANNEL COOLER RESULTS AND DISCUSSION

Figure 5 shows the thermal resistance versus flow results for a number of microchannel coolers with pitches between 50 and 100 microns, nominal channel widths of 20 to 60 microns, and continuous or staggered fins. The total thermal resistance, in °C/W, of each cooler was calculated as

$$R_t = (T_j - T_i)/Q_t \,, \tag{1}$$

where Q_t was the total power applied to the heater. Note that this value includes the thermal resistance of the 0.5 mm thick microchannel chip substrate, where $R_{sub} \approx 0.01$°C/W.

In Figure 5, the symbol type indicates the pitch; solid symbols are used for staggered fins and open symbols are used for continuous fins. The symbol darkness was varied for different nomi-

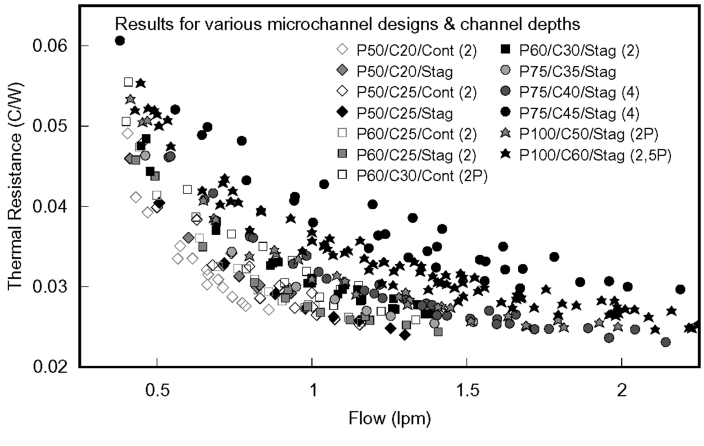

Figure 5. Plot of thermal resistance versus flow for a number of microchannel cooler designs.

nal channel widths having the same pitch. The number after the sample description indicates the number of unique samples represented; "P" is used for results reproduced from Colgan et al. (2005). For the staggered results, the results for different fin lengths were all grouped together for a given pitch and nominal channel width. As expected, for a given pitch and flow, the thermal resistance was lower for a smaller nominal channel width. Also, lower thermal resistance values were achieved at lower flows with finer pitch designs.

The corresponding differential pressure versus flow results are shown in Figure 6, which uses the same symbol conventions as used in Figure 5. As expected, the finer pitch designs, which also have shallower etch depths because the nominal channel width is smaller, had much higher pressure drops than the coarser pitch designs. For the few 50 and 60 micron pitch cases where there were continuous and staggered fins with the same pitch and nominal channel width, the pressure drop for a constant flow was higher with continuous fins than with staggered fins. The measured differential pressure drop includes some contribution from the manifolds to which the microchannel coolers were connected.

To display all the differential pressure results on a single curve, the measured differential pressure, ΔP, was converted into an apparent friction factor, f_{app}, using the wetted fin length L_w, fluid density ρ_f, channel average fluid velocity V, and channel hydraulic diameter D_h, using the expression

$$\Delta P = 2 f_{app} (\rho_f V^2)(L_w / D_h) \, . \tag{2}$$

Figure 7 shows the pressure data collected for both continuous and staggered fins, normalized to the form (f_{app}Re) as a function of the inverse of the normalized dimensionless wetted fin length (L_w/D_h)/Re. With an aspect ratio around 5, f_{app}Re for developed flow should converge to about 19 (Kays 1966). The data, when viewed on a linear plot, suggest that (f_{app}Re) approaches 41 as the normalized channel length increases. This higher-than-expected value is probably due to the fact that the experimentally measured differential pressure values include contributions from both the microchannels and the inlet and outlet manifolds. Thus, the contribution of the microchannels alone cannot easily be determined. The increased scatter in Figure 7 at low Rey-

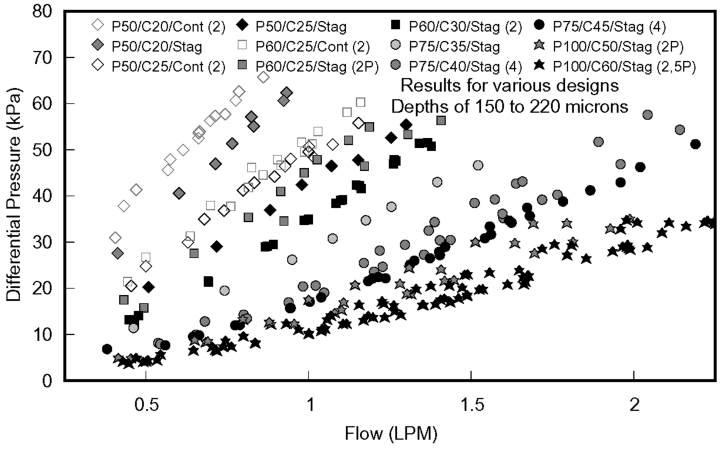

Figure 6. Plot of differential pressure versus flow for a number of microchannel cooler designs.

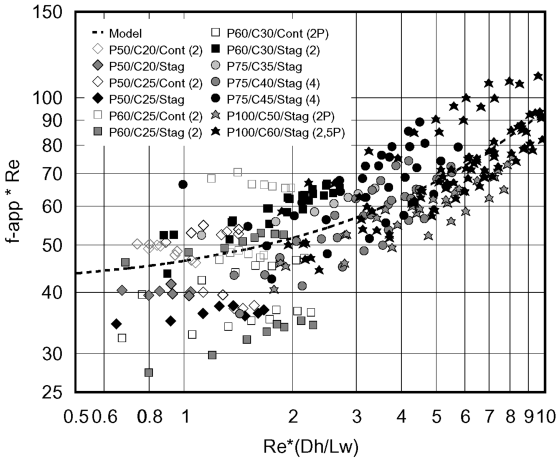

Figure 7. Friction coefficient for microchannel coolers with different designs.

nolds number is probably due to increased experimental uncertainty at low flow velocity and/or low channel hydraulic diameter.

To provide a generalized design methodology for microchannel coolers such as those described in this paper, it is useful to evaluate the dependency of the average heat transfer coefficient, h_c, on the cooler design and operating parameters. The advantage of such an approach is that it separates the channel geometric parameters, such as channel pitch, width, height, and length, from operating parameters, such as fluid type and flow velocity. The procedure used here to extract the average heat transfer coefficient assumes that the thermal conduction along the axial axis (channel length) is small. To verify this assumption, we used the approach described by Maranzana et al. (2004) where a factor M, representing the ratio between thermal conduction and thermal convection heat flux rates, must be evaluated. Axial conduction cannot be neglected when $M > 0.05$, but it can be safely neglected when $M < 0.01$. The following equation is given to evaluate this factor:

$$M = (\lambda_w W_w)/(L_w \rho_f Cp_f W_f V) \tag{3}$$

The data presented here have an average value of $M = 0.005$, with most of the data falling in the range of $M < 0.01$, hence, validating our assumption.

The thermal performance of the cooler can be characterized by extracting the overall heat transfer coefficient, U_t, from the experimental data. Here we used a generic heat exchanger model with a constant wall temperature (at the heater location), represented by the following equation:

$$Q_t = U_t A_t \Delta T_{lm} \tag{4}$$

where ΔT_{lm} is the log mean temperature difference between the heater and the fluid and A_t is the total chip area. Note that this generic equation is independent of the number of heat exchange zones used in the cooler. This equation also enables us to factor in the dependency between the cooler thermal performance and the fluid flow rate and inlet temperature.

This overall heat transfer coefficient includes two main thermal resistances, namely, the resistance of the silicon substrate and the composite resistance of the microfins and fluid above the

silicon substrate. Since the objective here is to evaluate the thermal characteristics of the cooler section above the silicon base, we can calculate an apparent heat transfer coefficient for the cooler, h_{app}, by subtracting the substrate resistance from the overall heat transfer coefficient:

$$1/h_{app} = 1/U_t - R_{sub} \tag{5}$$

The microchannel average heat transfer coefficient h_c was extracted from the experimental data using the following set of equations and a suitable iterative process.

An energy balance above the microchannel fin-section base, assuming constant base temperature, becomes

$$A_t h_{app} \Delta T_{lm} = A_w h_c \eta_w (T_{wf} - T_{af}) , \tag{6}$$

where the microchannel area A_w includes all four microchannel walls and all heat exchanger sections in the cooler chip, h_c is the average value for the average convection coefficient along the channel length, and η_w is the fin efficiency for the cooler using an extended fin height definition to include the impact of convection through the channel top wall. In this model, the fin height is extended by adding to it half of the channel width. The temperature differential on each side of Equation 6 is cancelled under the assumption that ΔT_{lm} in the left side of this equation is approximately equal to the average temperature differential $(T_{wf} - T_{af})$ in the right side since the wall temperature is already assumed to be constant.

Thus, the fin efficiency for constant cross section microchannel fins is

$$\eta_w = (1/\phi)\tanh(\phi) , \tag{7}$$

with

$$\phi = (H_w + 0.5W_f)[2h_c/(W_w \lambda_w)]^{1/2} . \tag{8}$$

The iterative process is needed because the unknown average convection coefficient, h_c, appears inside and outside the transcendental function given in Equation 7. After reducing Equations 6, 7, and 8 into a single function of the form $F(\phi) = 0$, we used the Newton-Raphson procedure to iterate ϕ, starting with $\phi = 1$ for quick convergence.

The results of this analysis are shown in Figure 8 using dimensionless axes, where the x axis is the inverse of the channel dimensionless length $\mathrm{RePr}(D_h/L_w)$ and the y axis is the Nusselt number defined as $\mathrm{Nu}_c = h_c D_h/\lambda_f$. Also included in Figure 8 are reference lines representing the expected theoretical thermal performance for this particular situation using the analysis provided by Kays (1966) where the reference lines correspond to channels with aspect ratios of 3, 5, and 7. For the tested microchannels, the channel aspect ratio AR ranged from about 2 to 7 with an average value of about 4. Analysis of the thermal data, excluding sample P75/C45/Stag, suggests the following relationship for the Nusselt number $\mathrm{Nu}_c = 3.8 + 0.15\ \mathrm{RePr}(D_h/L_w)$, which is recommended for design purposes. Sample P75/C45/Stag is excluded because its thermal behavior is statistically different from all other samples, suggesting the presence of an unknown experimental bias when the sample was built and tested.

The approximate agreement of experimental data and theoretical lines shown in Figure 8 support the assumptions made in selecting the equations used to characterize the thermal performance of these microchannels. Some of the scatter could be due to variations in the amount of undercut of the fins, which has been mentioned previously.

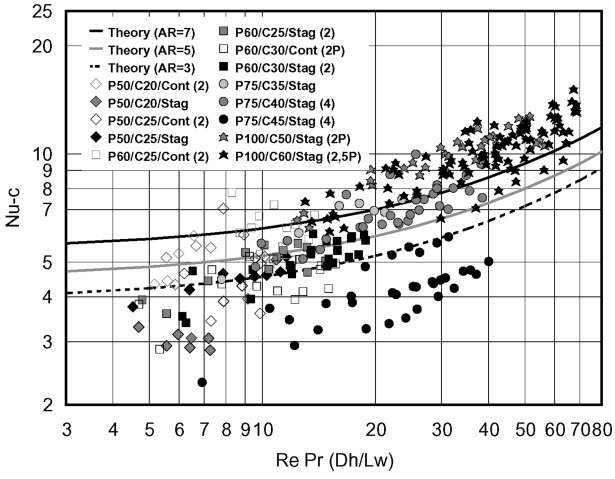

Figure 8. Nusselt number for microchannel coolers with different designs.

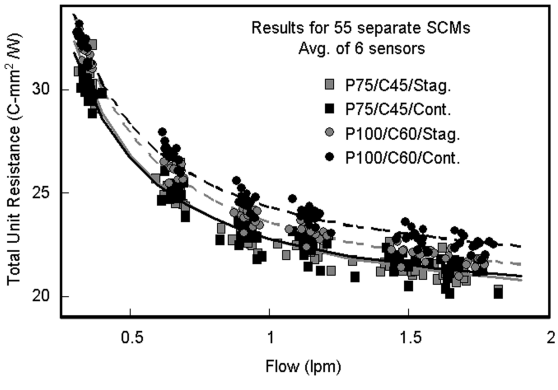

Figure 9. Plot of total unit thermal resistance versus flow for 55 SCMs with four different microchannel cooler designs.

SINGLE-CHIP MODULE RESULTS

The total thermal resistance versus flow results for 55 microchannel SCMs with four different microchannel configurations is plotted in Figure 9. A detailed thermal model of the structure was used to relate the measured thermal resistance (°C/W) to the unit thermal resistance (°C·mm^2/W) indicated in Figure 9. The total unit thermal resistance includes the thermal chip, the Ag epoxy, and the microchannel cooler. Square symbols were used for the 75 micron pitch coolers and circular symbols were used for the 100 micron pitch coolers, where gray was used for staggered fins and black was used for continuous fins. These measurements used the average of six resistive temperature sensors on the front surface of the thermal chip, where two were near the chip center, two were near the diagonal centers, and two were near the chip edge. The measurements were made with four inlets and three outlets, where the chip sensors were closer to the fluid inlet than to the outlet. With a flow of 1.25 lpm, reversing the flow direction causes the measured thermal resistance to increase by 3%. Therefore, the average thermal resistance, (i.e.,

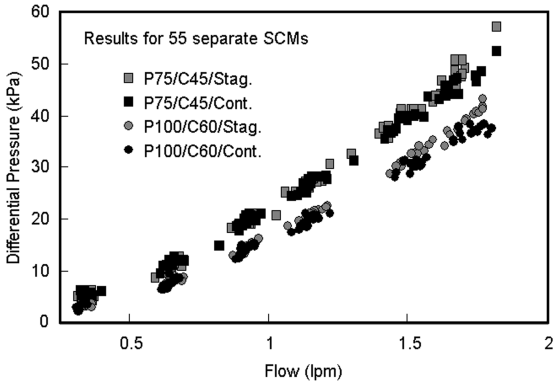

Figure 10. Plot of differential pressure versus flow for 55 SCMs with four different microchannel cooler designs.

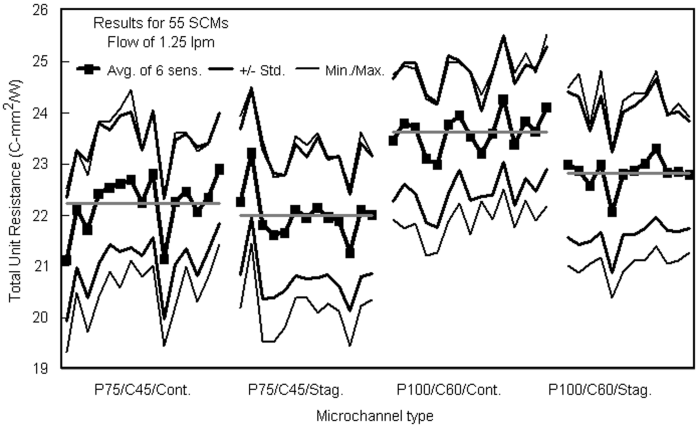

Figure 11. Plot of total unit resistance with a flow of 1.25 lpm for 55 SCMs with four different microchannel cooler designs showing the SCM-to-SCM and within-SCM uniformity.

midway between the inlet and outlet) is about 1.5% larger than the values plotted above. The same type of Ag epoxy was used in the assembly of these SCMs. With a pitch of 100 microns, the staggered fins clearly have a lower total thermal resistance than the continuous fins, but the difference is much smaller with a pitch of 75 microns.

The differential pressure versus flow for the 55 microchannel SCMs is plotted in Figure 10, where the same symbol conventions were used as in Figure 9. The pressure drop was lower for the 100 micron pitch coolers because of the greater channel width used (60 vs. 45 microns). For either a 75 or 100 micron pitch with corresponding channel widths of 45 or 60 microns, with flows of more than about 1 lpm, the pressure drop was slightly higher for the staggered fins than for the continuous fins.

For the 55 microchannel SCMs in Figures 9 and 10, the SCM-to-SCM and within-SCM uniformity was examined. In Figure 11, the average total unit resistance of the six sensors is plotted for the four different types of microchannel coolers with a flow of 1.25 lpm. The minimum and maximum values, along with the average plus and minus the standard deviation, are also plotted.

For SCMs with the same type of cooler and for any one of the six sensors, the average standard deviation of the total unit resistance was about 2%. For the six different sensors on any individual SCM, the average standard deviation of the total unit resistance was about 5% for all the SCMs. The SCM-to-SCM uniformity was very good, especially considering that the parts were built as much as five months apart. The variation across the SCM is related to the relative location of the sensors to the fluid inlet and outlet manifolds and the heaters.

One alternative microchannel cooler design, shown by three-dimensional rendering in Figure 12, was also tested. In this design, the 18.6 × 18.6 mm active area of the Si microchannel cooler is divided into 31 parallel-fed heat exchanger zones and the flow length between the inlet and outlet manifolds is 0.5 mm. This increased manifolding permits finer pitch channels to be used with an acceptable pressure drop but reduces the area occupied by the fins. Alternating rows of fluid vias are used as inlets and outlets (see Figure 12). The fluid vias in the manifold chip were formed as elongated ovals to better couple the flow into the distribution manifolds.

The total thermal resistance versus flow for this alternative design microchannel SCM is plotted in Figure 13, along with data for a 60 micron pitch cooler with 35 micron channels and 500 micron long staggered fins with six heat exchanger zones. For these microchannels, the thermal chip was thinned to 400 microns from the standard 725 microns and the thickness of the channel chip was reduced to 450 microns from the standard 675 microns. As before, the total unit thermal resistance includes the thermal chip, the Ag epoxy, and the microchannel cooler, and the results are for the average of six sensors. Square symbols were used for a 60 micron

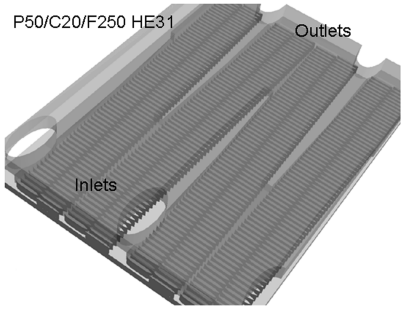

Figure 12. Three-dimensional rendering of a portion of an assembled microchannel cooler with an alternative design having 31 heat exchanger zones.

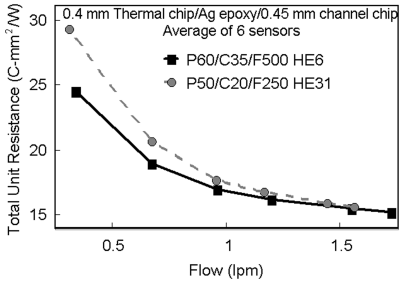

Figure 13. Plot of total unit resistance versus flow for two high-performance microchannel cooler SCMs.

pitch cooler with a 35 micron channel and with 500 micron long fins having six heat exchanger zones similar to the design shown in Figure 2. Circular symbols were used for a 50 micron pitch cooler with a 20 micron channel and 250 micron long fins having 31 heat exchanger zones, as shown in Figure 12. At lower flows, the performance was better for the 60 micron pitch cooler. The corresponding differential pressure versus flow results are plotted in Figure 14, where the same symbol conventions are used as in Figure 13. Except at low flow, the pressure drop is lower with the 60 micron pitch cooler. The low measured thermal resistance values suggest that these coolers are suitable for cooling very high power densities.

The high power performance of these packaged microchannel coolers was also measured. Figure 15 shows results for the 50 micron pitch microchannel SCM with a 20 micron channel and 31 heat exchanger zones for various flow conditions when about 1250 W was applied to the heater resistors. The powered area was 3 cm^2, so the power density was > 400 W/cm^2. The power (dashed line without symbols and right-hand axis) was turned off while stabilizing different flow conditions. The temperature difference between the chip (determined from the average of the six chip sensors) and the inlet water is plotted with square symbols. The temperature difference between the outlet and inlet water is plotted with circular symbols and indicated on the

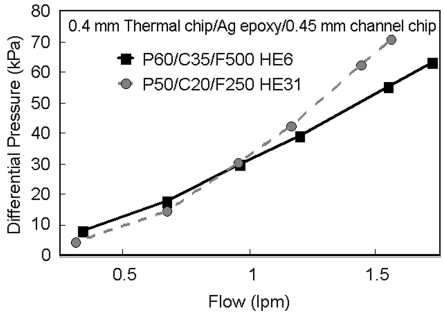

Figure 14. Plot of differential pressure versus flow for two high-performance microchannel cooler SCMs.

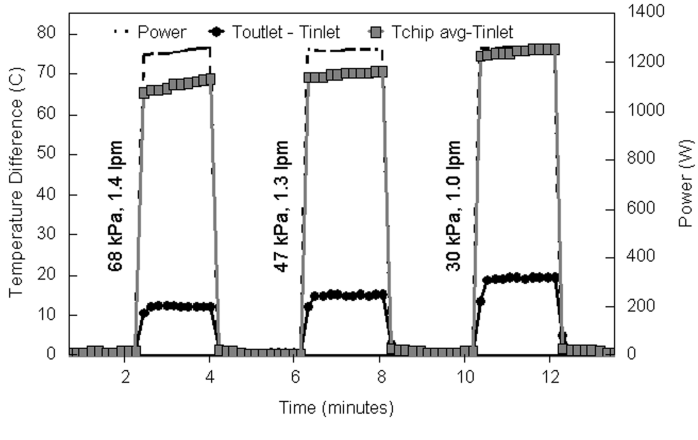

Figure 15. Microchannel SCM with 50-micron pitch and 20-micron-wide channels with 31 heat exchanger zones for various flows and 1.25 kW power.

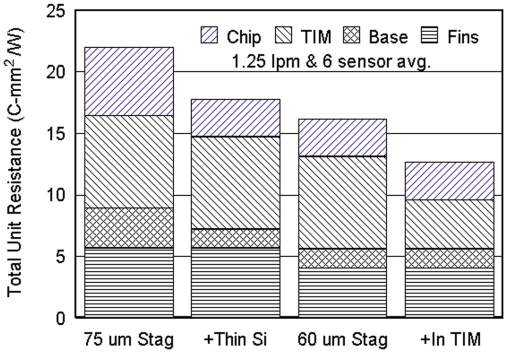

Figure 16. Estimated contributions to the total unit thermal resistance of different microchannel SCM configurations.

left axis. This result demonstrates cooling of > 400 W/cm^2 (total power of ~1250 W) by an Si microchannel cooler attached to a thermal chip in an SCM.

Figure 16 shows graphically the approximate contributions of the various components to the total unit thermal resistance, where the first and third bars are for measured results. With the 75 micron pitch staggered fins (Figure 11) with a flow of 1.25 lpm, the average total unit resistance for all six sensors was 22.0°C·mm^2/W. The second bar indicates the expected reduction if the chip was thinned from 725 to 400 microns and if the channel substrate was thinned from 425 to 200 microns (total reduction of 4.2°C·mm^2/W). With the 60 micron pitch staggered fins (Figure 13) for a flow of 1.25 lpm, the average total unit resistance for all six sensors was 16.2°C·mm^2/W, where the chip was 400 microns thick and the channel substrate was 200 microns thick. The thermal unit resistance can be further reduced by replacing the Ag epoxy TIM (~7.5°C·mm^2/W) with a thin In solder layer (~4°C·mm^2/W), as shown in the fourth bar.

CONCLUSIONS

In this paper we have extended our previous work to include even higher power densities for Si microchannel coolers assembled to chips in SCMs in a laboratory environment. We have further shown very good uniformity from SCM to SCM (±2%) and within a SCM (±5%). With a flow of 1.25 lpm, an average unit thermal resistance of 16.2°C·mm^2/W between the chip surface and the inlet cooling water has been demonstrated for an Si microchannel cooler attached to a 18.5 × 18.6 mm chip using an Ag epoxy in a SCM. Further, cooling 400 W/cm^2 was demonstrated for a microchannel SCM. Coolers of this design should be able to cool chips with average power densities of 500 W/cm^2 or more by replacing the Ag epoxy layer with In solder.

ACKNOWLEDGMENTS

We are deeply indebted to W. Graham, B. Kane, W. Lam, D. Lisounenko, K. McCollough, R. Meyer, J. Newbury, A. Niera, R. Nunes, R. Owen, D. Patsy, D. Posillico, M.B. Rothwell, C. Scerbo, M. Steen, C. Tsang, J. Vichiconti, and B. White in the IBM Yorktown Microelectronics Research Laboratory for fabrication of the silicon wafers and to S. Bradley and F. Pompeo for chip joining. We would also like to thank B. Humphrey of RC Molding and L. Mabbott of Micralyne for technical support in the fabrication of the plastic manifold blocks and the fusion-bonded microchannel coolers.

NOMENCLATURE

A = heat transfer area, m^2
AR = channel aspect ratio
Cp = heat capacity, J/Kg·K
D_h = hydraulic diameter, m
f = friction coefficient
h = heat convection coefficient, $W/m^2 \cdot K$
H = height, m
L = wetted length, m
M = heat flux ratio, defined in Equation 3
Nu = Nusselt number
P = fluid pressure
Pr = Prandtl number
Q = power, W
R = total thermal resistance, K/W
Re = Reynolds number
T = temperature, K
U = overall heat transfer coefficient, $W/m^2 \cdot K$
V = fluid average velocity, m/s
W = width, m

Greek Symbols

Δ = differential
η = fin efficiency
λ = thermal conductivity, W/m·K
ρ = density, Kg/m^3
ϕ = fin efficiency parameter, defined in Equation 8

Subscripts and Abbreviations

af = average fluid
app = apparent
c = average
f = fluid
i = inlet
j = heater
lm = log mean
t = total
sub = substrate
w = fin
wf = fin-fluid interface

REFERENCES

Colgan, E.G., B. Furman, M. Gaynes, W. Graham, N. LaBianca, J.H. Magerlein, R.J. Polastre, M.B. Rothwell, R.J. Bezama, R. Choudhary, K. Marston, H. Toy, J. Wakil, J. Zitz, and R. Schmidt. 2005. Practical implementation of silicon microchannel coolers for high power chips. *Proceedings of the 21st Annual IEEE Semiconductor Thermal Measurement and Management Symposium, San Jose CA, March 15–17,* pp. 1–7.

Harpole, G.M., and J.E. Eninger. 1991. Micro-channel heat exchanger optimization, *Proceedings of the Seventh IEEE Semi-Therm Symposium*, pp. 59–63.

Kays, W.M. 1966. *Convective Heat and Mass Transfer*, ch. 6, 8, and 9. New York: McGraw-Hill.

Kishimoto, T., and S. Sasaki. 1987. Cooling characteristics of diamond-shaped interrupted cooling fins for high power LSI devices. *Electronic Letters* 23(9):456–57.

Laermer, F., and A. Urban. 2003. Challenges, developments and applications of silicon deep reactive ion etching. *Microelectron. Eng.* (The Netherlands) Vol. 67–68, pp. 349–55.

Maranzana, G., I. Perry, and D. Maillet. 2004. Conjugated heat transfer in 2-dimensional mini and micro channels: Influence of axial conduction in the walls. *Proc. 2nd Int. Conf. on Microchannels and Minichannels*, pp. 251–58.

Prechtl, P., and O. Kurtz. 2004. Efficient liquid cooling technologies for computer systems. Advanced Technology Workshop on Thermal Management, *IMAPS ATW Conf., Palo Alto, CA, Oct. 25–27.*

Tuckerman, D.B., and R.F.W. Pease. 1981. High performance heat sink for VLSI. *IEEE Electron Dev. Lett.* EDL-2(5):126–29.

Webb, R.L. 2003. Effect of manifold design on flow distribution in parallel micro-channels. *Proc. IPACK03, International Electronic Packaging Technology Conference, Maui, Hawaii, July 6–11,* paper #35251.