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Wire Variation and Dummy Fill Impacts on RC and Delay

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Wire Variation and Dummy Fill Impacts on RC and Delay

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ABSTRACT

As device sizes continue to shrink, the design is increasingly affected by the variability in the back end of the line. We did a series of experiments to investigate the wire thickness/width variation impacts on RC and delay. The test results reveal that wire thickness and width variations have large impacts on RC and delay. Therefore, it is very important to understand and capture these kinds of variation impacts so as to improve product reliability and yield. In addition, we measure the dummy fill impacts on wire capacitance, and the test data show that the introduced capacitance can be up to 11.5%.

1. Introduction

As CMOS technology continues to scale, the design is increasingly affected by the variability in the back end of the line (BEOL). In order to achieve acceptable design quality, these variations should be well understood so that their impacts can be taken into account in the circuit and layout design flow.

Different manufacturing processes lead to different physical and electrical effects that can significantly degrade circuit performance, yield and robustness. CMP (Chemical Mechanical Polishing) is a primary technique to planarize layer surface in order to establish reliable multilevel copper interconnects [2]. However, the wear-down of the tops of metal wires during CMP process results in uneven wire thickness across a chip. Meanwhile, lithography limits have exerted pronounced influence on nanometer designs. Although RET (Resolution Enhancement Technique) such as OPC (Optical Proximity Correction) [5, 6], PSM (Phase-Shift Mask) [4, 7] are deployed to deal with diffraction-induced distortions, wire width variations are still non-negligible. Therefore, it is very important to understand and capture the parametric variations caused by manufacturing and lithographic wire distortions in order to improve product reliability and yield.

In this paper, we first present data to show interconnect RC and delay changes caused by wire thickness and width variations. The data are in 65***nm*** technology node and obtained by IBM modeling and simulation CAD tool AQUAIA. The wires measured in our experiments are on B1 layer which is a 2X metal layer. Then the CMP dummy fill impacts on wire capacitance are addressed in Section 3.

2. Thickness & Width Variation Impacts on RC & Delay

Intra-chip copper interconnect thickness variation today is on the order of 20~40% [1]. This variation is mainly caused by the interaction of layout features on the chip with the physics of CMP process such as dishing and erosion [3]. At the same time, wire width varies due to etch/litho issues. In this section, we present the data of RC and delay changes when the wire thickness varies within ±30% of the nominal thickness, and the wire width varies within ±10% of the nominal width.

2.1 Resistance Variations

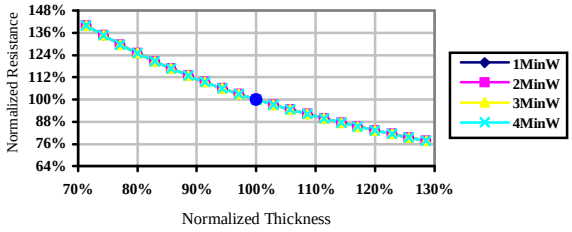


Fig 1. Thickness variation impacts on resistance

As the wire thickness increases, the wire resistance decreases. Figure 1 shows that the wire resistance varies from -22% to +40% when the thickness varies within ±30% of the nominal thickness. The plots are measured for wires of 1, 2, 3 and 4 times of the minimum wire width. ***MinW*** refers to minimum wire width.

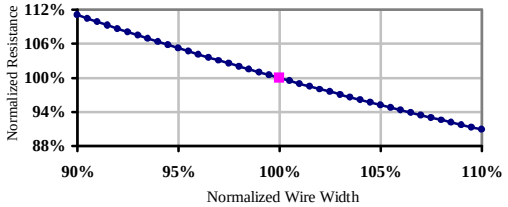


Fig 2. Width variation impacts on min-width wire resistance

On the other hand, when the wire width increases, the wire resistance decreases as well. As illustrated in Figure 2, when min-width wire varies within ±10% of the nominal width, the resistance varies by ±10% compared to the resistance of a wire with the nominal width.

2.2 Capacitance Variations

As the wire thickness increases or the wire width decreases, the wire capacitance becomes smaller. We measure the capacitance changes respect to wire thickness/width variations. The measurement is based on the test structure as shown in Figure 3.

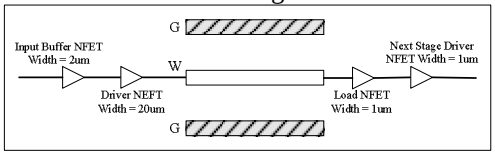


Fig 3. Test structure

One signal wire (W) is placed in the middle of two ground wires (G), and the distance between the signal wire and a power rail is the minimum spacing of B1 layer as specified by IBM 65***nm*** technology. Suppose the density of the upper layer and lower layer is 50%.

As shown in Figure 4 and Figure 5, the wire capacitance changes (±13%) caused by wire thickness variations are much larger than the capacitance changes (±4.5%) caused by width variations.

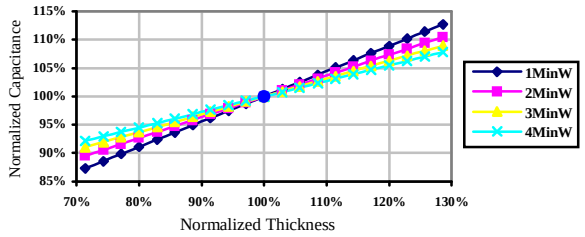


Fig 4. Thickness variation impacts on capacitance

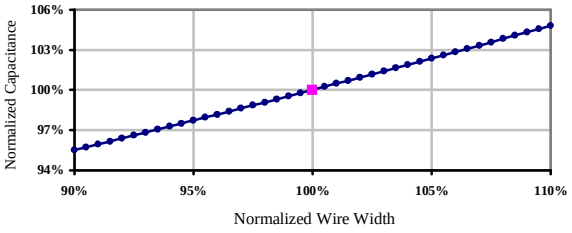


Fig 5. Width variation impacts on capacitance for min width wire

2.3 Delay Variations

Although the resistance and capacitance change in the opposite directions when the wire thickness and width increase/decrease, the interconnect delay still varies a lot as shown in Figure 6, 7 and 8. The delay is also measured on the structure in Figure 3. The wire length is 1***mm***.

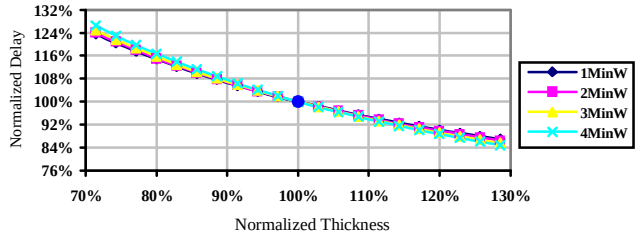


Fig 6. Thickness variation impacts on wire delay

As illustrated in Figure 6, ±30% thickness variation can lead from -14% to +23% delay changes on a min-width wire. The delay impacts on wires with larger wire width are a little bit larger. Figure 7 shows that ±10% width variations can lead to about -5% ~ +7% delay change on a min-width wire. With combined ±30% thickness and ±10% width variations as shown in Figure 8, the delay variation spans from -18% to +32% of the delay of a wire with nominal thickness and width.

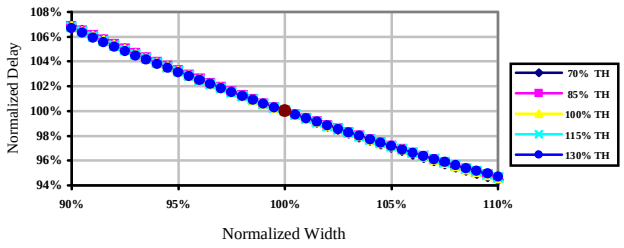


Fig 7. Width variation impacts on delay for min width wire

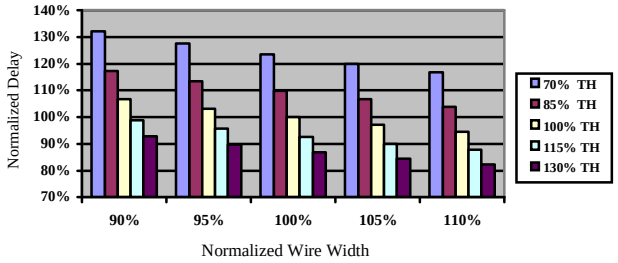


Fig 8. Thickness and width variation impacts on delay (Normalized against the wire delay with nominal thickness & width)

2.4 Delay Simulation for Thickness/Width Variations

The process variations usually have different impacts on different parts of one wire. To simulate the thickness/width variations on one wire, we divide a wire into 20***um*** wire segments. Each wire segment is assigned a randomly generated thickness and width as shown in Figure 9. Suppose the wire thickness and width distribution obeys Gauss distribution. For the wire thickness, let the nominal wire thickness be the mean of the Gauss distribution, and ±30% of the nominal thickness be ±3σ point. Similarly, the nominal wire width is the mean of the wire width Gauss distribution, and ±10% of the nominal width is ±3σ point.

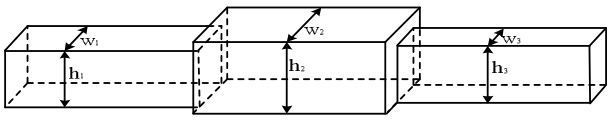
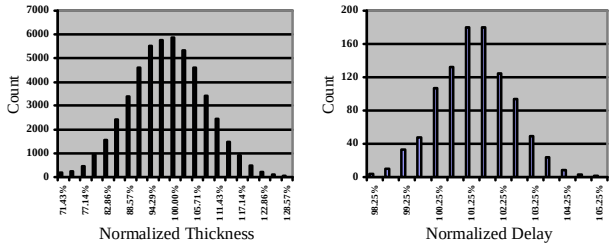


Fig 9. Segments with randomly generated thickness and width

Figure 10 shows the wire delay distribution when the thickness of each wire segment varies as Gauss distribution. The wire width of each segment is still the nominal width. The test is measured on a 1***mm*** wire whose width is two times of the min-width. And the data is based on 1000 trials. (a) shows the distribution of 50,000 wire thickness instances. (1***mm*** wire is divided into fifty 20***um*** segments. Each wire segment is assigned a thickness. Therefore, the total thickness instances are 50x1000.) (b) shows the distribution of 1000 wire delay instances. The delay also follows a distribution very close to a Gauss distribution whose mean is around 2%. The delay variation spans from -2% to +5% of the nominal delay.



(a) Thickness distribution (b) Delay distribution

Fig 10. (a) Gauss distribution of wire thickness (b) Delay distribution

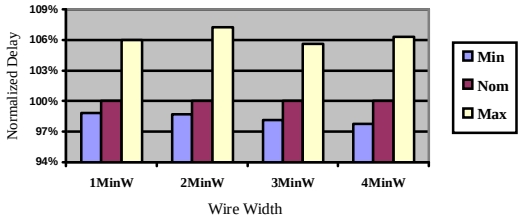


Fig 11. Delay span range when thickness and width vary in Gauss distributions

For width variations and combined thickness and width variations, the delay distribution is also close to a Gauss distribution. The impacts from width variations are much smaller than those from thickness variations. Figure 11 shows the delay span range with combined thickness and width variations. In general, the delay variation can be -2% ~ +6% of the nominal delay.

3. CMP Dummy Fill Impacts on Capacitance

To achieve CMP planarity and yield optimization, foundries usually require an effective metal density to be satisfied, and dummy fills are widely used to adjust local metal density [8]. However, the introduction of large amount of dummy fills also affects wire electrical properties. The impact of dummy fills on wire capacitance is measured on the test structure as illustrated in Figure 12. One signal wire is placed between two power rails, and the dummy features are inserted around the signal wire according to IBM 65***nm*** dummy fill specification. The dummy fills are floating metal squares in IBM Kemerer-5 pattern. The wire length is 500***um***, and ***MinS*** refers to the minimum wire-to-power spacing. Since the spacing between dummy fills and signal wire may vary, the induced wire capacitance increase is also different. Furthermore, different wire locations lead to different amounts of dummy fills.

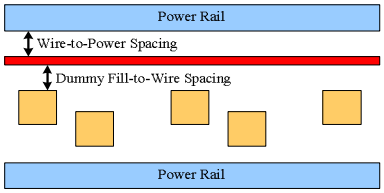


Fig 12. Test structure for dummy fill impacts on capacitance

Figure 13 illustrates the capacitance changes with respect to the wire-to-power spacing changes. The plot shows the maximum and minimum wire capacitance compared to the wire capacitance without dummy fills (denoted as ***Nom***). As shown in Figure 13, the capacitance increase can be up to 10%.

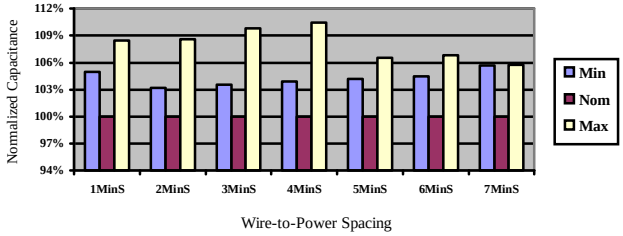


Fig 13. Dummy fill impacts on wire capacitance

4. Conclusion

In this paper, we investigate the wire thickness/width variation impacts on RC and delay. Test results show that ±30% thickness variations can lead to -22%~+44% resistance change, and ±13% capacitance change. Also ±10% width variations can lead to ±10% resistance changes and ±4.5% capacitance changes. Combined ±30% thickness and ±10% width variations can result -18%~+32% delay changes on a 1***mm*** min-width wire. Furthermore, dummy fills, which are widely used for CMP planarization, can also lead to +4%~+11.5% capacitance increase. Since these kinds of RC and delay changes are caused by manufacturing variations, they should be well addressed in layout designs to guarantee performance and manufacturability.

5. References

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