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Gate Oxide Reliability for Nano-Scale CMOS

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Abstract - The reliability of the gate oxide in microelectronics, i.e., the ability of a thin film of this material to retain its excellent dielectric properties while subjected to high electric fields, has been a perennial concern over the last 40-45 years. Two dominant gate oxide failure mechanisms, dielectric breakdown and the negative bias instability, have continued to cause concern as MOSFET devices have scaled to nanometer dimensions.

I. Oxide Breakdown

The effect of gate oxide reliability on nano-scale CMOS circuits may be expressed as the maximum allowable voltage that can be applied to the total gate area on a chip, such that no more than a specified failure rate will result. Fig. 1 shows a compendium of various predictions concerning oxide breakdown from different research groups [1-5] for the maximum operation voltage, V_{max}, as a function of gate oxide thickness (t_{ox}). (For a detailed discussion of this figure see [4] and [6].)

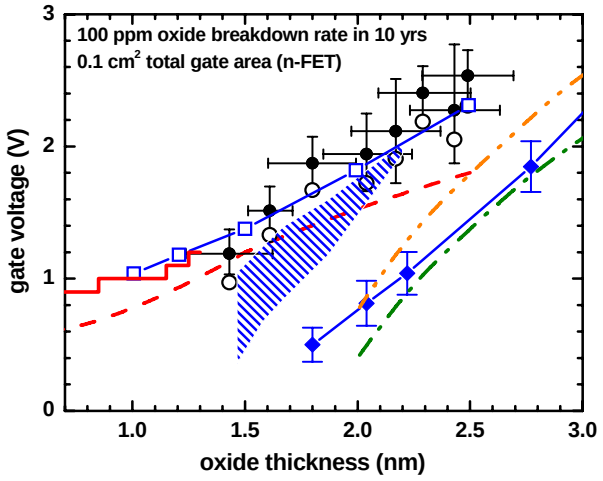

Fig. 1. Oxide breakdown projections from different research groups during the period 1998-2002. This figure shows the maximum allowable voltage that can be applied to the total gate area on a chip, such that no more than a specified failure rate will result. The failure rate in this case is defined as the fraction of chips that will experience one or more oxide breakdown events. Also shown are industry roadmaps for gate oxide thickness and operation voltage from 1999 (dashed) and 2002 (stepped). From [6].

As shown in Fig. 1, the predicted reliability limits due to oxide breakdown have moved toward thinner oxides and higher operation voltage as more data have been collected and new analysis approaches have been applied. Indeed, the most optimistic projection, based on an empirical power-law voltage dependence [7], supports the use of oxynitride gate dielectrics down to ~1nm at 1V. However, more aggressive scaling, or operation at higher voltage for improved speed, makes it increasingly likely that one or several oxide breakdown (BD) events may expected over the life of a chip. The earlier oxide reliability projections were based on the assumption that a single breakdown (soft or hard) on a chip would cause circuit failure, which is no longer believed to be correct. For accurate reliability projections it is necessary to better understand the nature of the BD event [8] and the effect of BD on circuits. Therefore it has become necessary to look in more detail at the nature of the breakdown event and the behavior of devices and circuits after oxide failure [6,9,10].

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A. Progressive Breakdown

Several groups [11-13] have pointed out that "hard" BD is not a sudden, catastrophic process, as previously thought. BD occurs gradually over a measurable time scale. For poly-gate CMOS at present-day oxide thickness, the growth of the gate leakage through the BD spot can be very slow at low stress voltage. This phenomenon is called "progressive" breakdown (PBD) [11]. PBD is a *gradual* hard BD, and is distinct from "soft" BD, which is a stable, low current that is typically not observed in small devices. An example of a current-vs.-time time trace is shown in Fig. 2 [13].

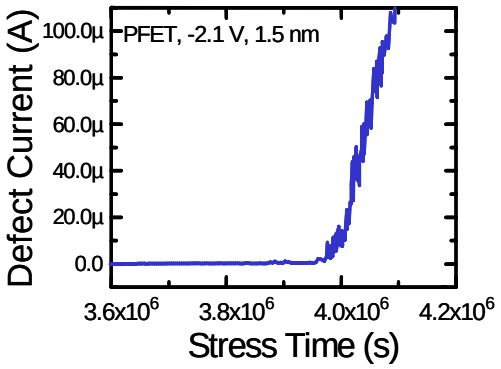

Fig. 2. Breakdown transient for 1.5nm oxide stressed at -2.1V. After [13].

The post-BD leakage growth rate can be quantified in various ways [6,10-14]. Fig. 3 shows the voltage dependence of the progressive breakdown rate, R_D, for t_{ox}=1.5nm [13]. This is similar to the voltage dependence of the trap generation prior to breakdown, suggesting that the same

defect generation process that controls the initial breakdown time also drives the growth of the BD spot.

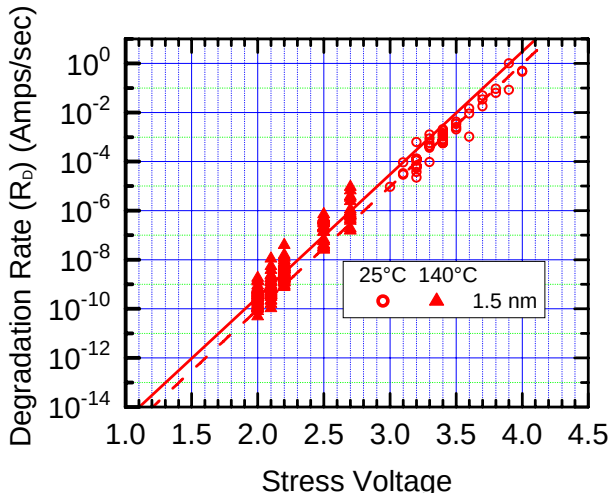

Fig. 3. The rate of increase of stress current for a 1.5 nm oxide after the beginning of breakdown, showing an exponential dependence for 10 orders of magnitude over a wide range of voltages. The degradation rate R_D is defined as the average rate of increase from 10μA to 100μA. After ref. [13].

B. Effect of Progressive Breakdown on Circuit Operation

Because the breakdown process is gradual and continuous, the chip or circuit failure will not coincide with the onset of breakdown, but instead will occur at a later time when a critical breakdown current is reached. Rather than first (soft) BD, the appropriate failure criterion is the leakage current that disrupts circuit operation. This criterion can increase lifetime estimates by several orders of magnitude over traditional projections [15]. The new oxide failure criterion has two key elements: Understanding and characterizing the post-breakdown defect growth, and understanding and characterizing the circuit sensitivity to leakage currents in gates that have experienced BD. Circuit simulations can be used to estimate circuit sensitivity to BD, by adding a voltage-dependent current source between the gate and one diffusion of a transistor as illustrated in Fig. 4 [9,16,17].

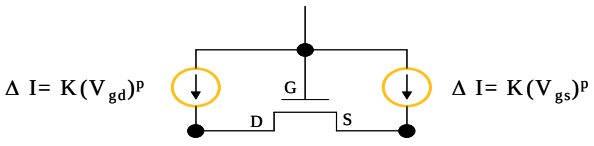

Fig. 4. Circuit model of gate-to-diffusion breakdowns. After ref. [17].

The effect of progressive BD has been studied experimentally using inverters in a 0.13μm technology (t_{ox} = 1.5nm) [17,18]. Constant voltage stress at 2.6–3.9 V of either polarity was applied from input to output, with V_{dd} and ground terminals floating. In this way a BD was made to occur at the drain side of either the n-FET or p-FET. Progressive BD was stopped at various stages by a current compliance [19].

The transfer characteristics of the broken inverters (Fig. 5) exhibit a combination of V_t shifts due to the voltage stress and reduced output swing due to post-BD leakage. The characteristics of the BD spot are different depending on stress polarity and whether the inverter output voltage is higher or lower than the input. In this figure the transfer curves show additional shift in switching point due to threshold voltage shifts in the n-FET and p-FET. These shifts occur prior to the BD event.

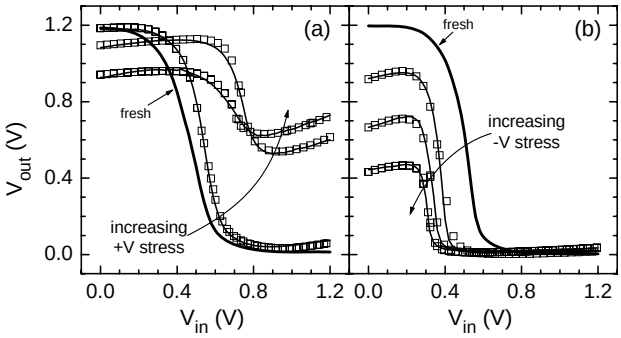

Fig. 5. Transfer curves of inverters after BD to various levels. (a) Positive stress on inverter input. (b) Negative stress on inverter input. Lines are experiment, symbols are model. For positive/negative stress, the leakage is highest when the input is higher/lower than the output. After ref. [18].

Calculated transfer characteristics using the same gate-to-drain leakage current model but without the V_t shift (Fig. 6) illustrate the influence of the oxide BD leakage current alone in the inverter transfer curve, to more accurately represent the effect of early BD under circuit operation conditions. The inverter transfer curves shown in Fig. 6 are the expected characteristics for chips in the field, where the earliest oxide breakdown may occur prior to significant V_t shift.

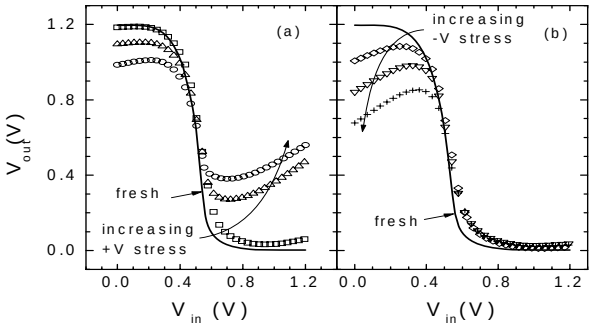

Fig. 6. Simulated inverter transfer curves with oxide leakage currents between the inverter input and output using same leakage as in Fig. 3, but with no V_t shifts (a) positive stress on the inverter input, (b) negative stress. After ref. [18].

Fig. 7 shows calculated transfer curves for two inverters in series with a drain (input-output) breakdown in the second inverter. The output of the first inverter is degraded, even though there is no breakdown in this stage. This is because the BD leakage in the second stage loads the first stage. Subsequent logic stages will restore the correct logical "1" and "0" states as long as the output of the broken stage is on the correct side of the crossover voltage Vco.

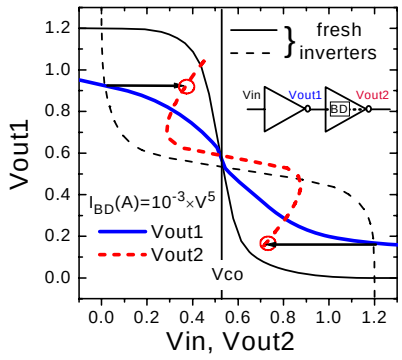

Fig. 7. Transfer curves for two inverters in series, with a drain (input-output) breakdown in the second stage. Small circles indicate the output states of the second inverter. Inverter chains transmit the correct logic state as long as output of broken stage is on the correct side of the crossover voltage. Thin (solid and dash) black lines represent Vout1 and Vout2 respectively without BD. After ref. [18].

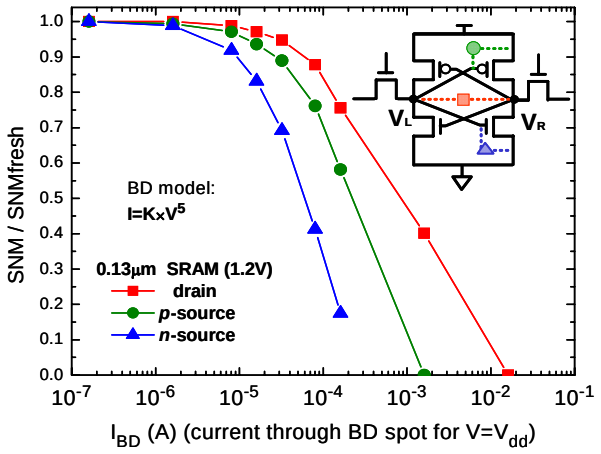

Fig. 8. Normalized SNM from circuit simulations as a function of BD leakage at V_{dd}, for 6-T SRAM cells with various BD locations. Symbols indicate BD locations. After ref. [16].

In an SRAM cell (Fig. 8, inset) oxide BD in either inverter of the cell loads the other inverter. Gate-to-source BD does not affect the transfer curve of an inverter, to first order. However, it does perturb the voltage at the output of the opposite inverter. A p-(n-) source BD raises (lowers) the voltage at the output of the opposite inverter, which must then supply current through the channel resistance of the on-state n-(p-)FET of the intact inverter. In order to quantify the cell stability we extract the worst-case static noise margin (SNM). This is the minimum DC noise voltage necessary to flip the state of the cell during a "read" operation, where the word line is pulled high while the bitlines are pre-charged high.

For fixed leakage, BD at p-source has less effect than n-source, because the opposing n-FET is stronger (relative to the p-FET). Fig. 8 shows the SNM, normalized to the SNM of the fresh cell, as a function of I_{BD} in a 0.13µm technology [16]. These results were obtained from circuit simulations. For the cells considered in this work, a 50% degradation in SNM results from oxide BD when the current through the BD spot reaches ~20–50 µA for the worst-case n-source breakdown [20]. Pass-gate or p-source breakdown may tolerate higher leakage, up to ~500 µA. These values are comparable with the on-currents of the fresh p-FET and n-FET respectively used in this SRAM cell, and may decrease with device widths, *e.g.*, for smaller SRAM cells.

C. Proposal for an Improved Breakdown Terminology

Oxide breakdown events are typically classified as "soft" or "hard" depending on the magnitude of the post-breakdown conduction. There is some confusion in the literature over the characterization of breakdown modes because of the lack of a precise definition of the terms and because for some experimental conditions the detection of one or the other breakdown mode may be difficult. For example, when testing a large area structure or a very thin oxide where the initial current is larger than the breakdown current, a "soft" event could be missed, or a "hard" event could be interpreted as soft. Although some of these problems can be overcome with careful experimental design, the recent understanding of PBD has made these earlier terminologies less satisfactory.

Various schemes have been devised to characterize the BD "hardness," *e.g.*, the post-breakdown resistance (V_{dd}/I_{BD}) or conductance (dI_{BD}/dV), [21-24] however this designation is often ambiguous because there is no universally accepted criterion. The result is that one author may refer to a given post-BD current level as SBD while another might characterize the same event as HBD.

Furthermore, the realization that the initial breakdown event ("first BD") may not disrupt circuit functionality has led to another usage of the terms SBD and HBD depending on the intended operation conditions of the MOSFET [25]. This *operational* definition obscures the *physical* nature of the BD. Here we describe a new view of BD characterization with a simpler, more physically meaningful terminology [8].

The steep voltage dependence of the post-breakdown degradation rate leads to an important implication for the BD characterization. As earlier pointed out by Monsieur, [11] if the oxide is stressed at a high voltage where the post-breakdown degradation rate is fast compared to the

experimental sampling time (typically longer than ~tens of milliseconds) then the breakdown will appear as "hard" according to the typical usage of this term. Likewise, if the oxide is stressed at a low voltage where the degradation rate is slow compared to the experimental sampling time, then the breakdown will appear as "soft".

This implies that there is no distinct physical characteristic which we can use to classify HBD vs. SBD. Rather, it is the exponential voltage and thickness dependence of the PBD growth time τ_D which causes a BD to appear as HBD for thick oxides and/or high voltage and as SBD for thin oxides and/or low voltage. This is illustrated schematically in Fig. 9, where the dashed line corresponds to a constant value of τ_D on the order of the experimental sampling time. Below this line the BD appears soft, while above the line the BD appears hard in a typical experiment. The hatched region corresponds to the domain which is accessible to experiment, *i.e.* within this band the time to first BD is of order seconds to hours. As oxide thickness is reduced the time to BD decreases rapidly because of the rapid increase in tunneling current [1], which requires the use of lower V_{stress} to keep the time to first BD within measurable range.

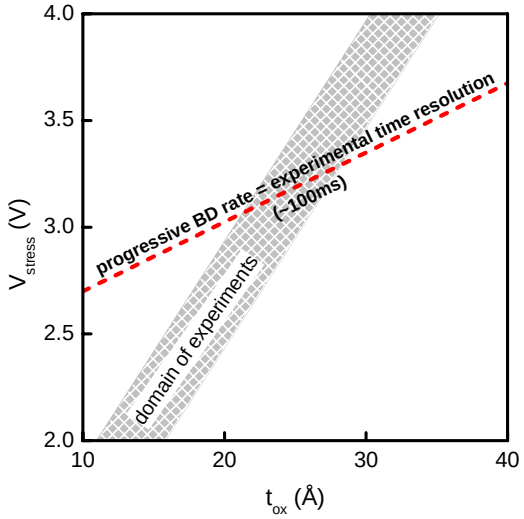

Fig. 9. The dashed line corresponds to a constant value of τ_D on the order of the experimental time resolution, for oxides of thickness t_{ox} stressed at voltage V_{stress}. Below this line the BD appears soft, while above the line the BD appears hard in a typical experiment. The hatched region corresponds to the domain which is accessible to experiment. After a similar figure by Monsieur [11].

This figure explains the observed trend that HBD is more prevalent in thicker oxides, *i.e.* this is really an effect of the changing V_{stress}, more so than t_{ox}. This also provides an explanation for the so-called HBD prevalence ratio which shows a rapid transition from ~0% to ~100% over a narrow voltage range, moving to higher voltage with increasing thickness [10]. The transition from SBD-like to HBD-like is not completely abrupt because of the existence of a statistical distribution in τ_D.

According to the new viewpoint, HBD and SBD are really just different manifestations of the same PBD mode, and the distinction between HBD and SBD depends mostly on measurement conditions. The PBD growth rate depends exponentially on voltage and thickness. This causes a BD to appear as HBD for thick oxides and/or high voltage and as SBD for thin oxides and/or low voltage. Physically, all BD should be described as PBD and characterized by its post-breakdown degradation rate.

We prefer to avoid the terms "soft" and "hard" because of their vague meaning. A more accurate term to describe cases of low or moderate post-breakdown conduction, such as results from removing the stress during the BD transient (either intentionally, *e.g.* by a compliance limit, or unintentionally, *e.g.* by series resistance) is *arrested* BD ("a-BD").

To describe the impact of breakdown on device and circuit functionality, different terminology should be used to clearly distinguish from the physical description. A BD which disrupts device or circuit functionality can be called *disruptive* or *destructive*. Of course, this is an application-specific description [9]. For example, a BD with ~ 50μA leakage at operation condition may be destructive in an SRAM application [16] but not in logic [6,9,26]. It is important to realize also that a less severe BD (*i.e.* non-destructive) cannot be assumed to be completely innocuous, since the initial BD spot may grow progressively into a destructive one. This terminology is summarized in Table 1 [27].

TABLE I
OXIDE BREAKDOWN TERMINOLOGY

Old terminology:	Soft (SBD)	Hard (HBD)
Improved physical description:	Arrested BD	
	Progressive Breakdown, described by post-breakdown rate of current growth	
Improved operational definitions (circuit dependent):	Non-destructive	Destructive

II. NBTI

The threshold voltage (V_t) shift in p-FETs caused by the negative-bias-temperature instability (NBTI) has emerged as one of the more interesting and potentially serious reliability limiters for state-of-the-art CMOS technology [28]. Although recognized for many years [29], NBTI has increasing significance for newer technologies that operate with lower supply voltage, because of the inability to fully scale the device threshold voltage, leading to reduced headroom. In addition, the introduction of nitrogen in the gate oxide, for control of dopant penetration and gate current, causes an increase in NBTI for the same physical oxide thickness and voltage condition [30,31]. The origin

of this nitrogen-enhancement effect is still under investigation. Fig. 10 shows an example of this effect [32].

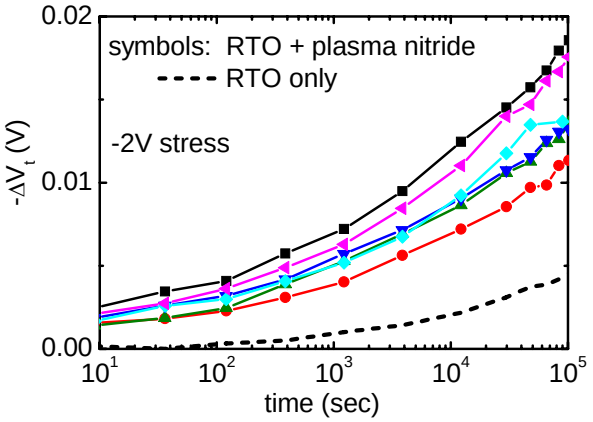

Fig. 10. Threshold voltage shift vs. time for 1.4nm oxide with various nitrogen concentrations. From [32].

Among the many interesting physical phenomena involved in NBTI, one aspect is the relative contribution of interface states and bulk traps to the net V_t shift [33]. The interface states near the middle portion of the Si band gap can be measured by capacitance-voltage, charge pumping, gated-diode, *etc*. These techniques fail close to the band edge, but in ultra-thin oxides the leakage current near flat-band condition (so-called low-voltage stress-induced leakage current, LV-SILC) is sensitive to the interface states at the conduction band edge [34-37]. Figs. 11 and 12 compare the contributions of mid-gap states (measured with gated diode) and conduction band-edge states (from LV-SILC) in pure SiO_2 vs. plasma-nitrided oxides [38].

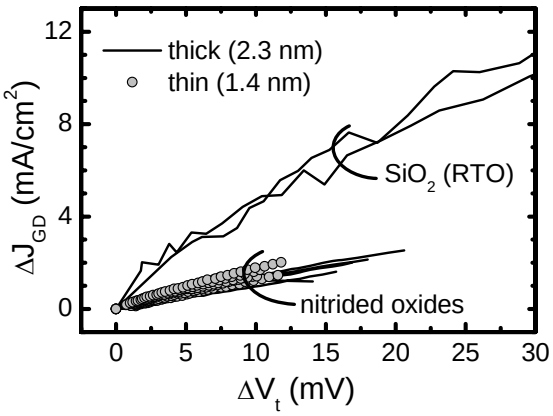

Fig. 11. Mid-gap recombination center density (gated diode current) vs. V_t shift for SiO_2 and oxynitride pFETs under negative bias stress (~10MV/cm). The gated diode current could not be measured in the 1.4nm SiO_2 sample because of high direct tunneling current. From [38].

Fig. 11 shows that the defect density at mid-gap is about four times greater for SiO_2 compared to oxynitride, for the same ΔV_t. Fig. 12 shows that pure oxide has negligible generated interface states at the conduction band edge, in contrast to oxynitride which shows a significant density of stress-induced interface states at this position. Together these two figures demonstrate that the defects associated with the nitrogen-enhanced NBTI [30] are different from those in pure oxide, and in particular that these nitrogen-associated defects have electrical levels in the upper portion of the Si band gap [32,38].

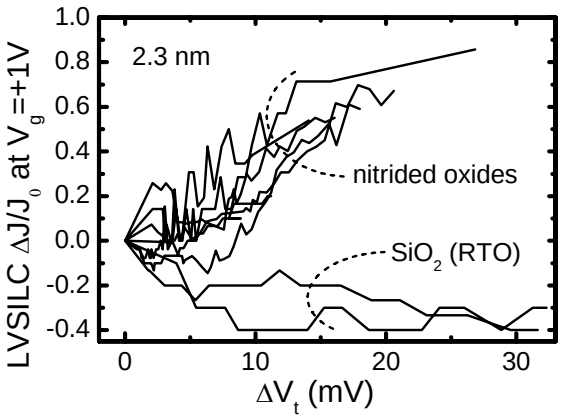

Fig. 12. Conduction band-edge interface state density (LV-SILC) vs. V_t shift for 2.3nm SiO_2 and oxynitride pFETs stressed at -10MV/cm. From [38].

III. Conclusion

Oxide breakdown and NBTI are two physical failure mechanisms in ultra-thin gate oxide which continue to generate interest. Ongoing work in these two subjects is needed to ensure the reliability of nano-scale CMOS circuits.

Acknowledgements

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