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Single-Event-Upset Critical Charge Measurements and Modeling of 65 nm Silicon-on-Insulator Latches and Memory Cells

David F. Heidel, Kenneth P. Rodbell, Phil Oldiges, Michael S. Gordon, Henry Henry H. K. Tang, Ethan H. Cannon*, Cristina Plettner
IBM Research Division
Thomas J. Watson Research Center
P.O. Box 218
Yorktown Heights, NY 10598

*IBM Systems & Technology Group
1000 River Street
Essex Junction, VT 05452

Research Division
Almaden - Austin - Beijing - Haifa - India - T. J. Watson - Tokyo - Zurich

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IBM Research Division, P.O. Box 218 Route 134, Yorktown Heights, NY 10598, USA
[(1)] IBM Systems & Technology Group, 1000 River Street, Essex Junction, VT 05452, USA

Phone: (914)-945-2361
Fax: (914)-945-4020
e-mail: heidel@us.ibm.com

Abstract

Experimental and modeling results are presented on the critical charge required to upset exploratory 65 nm silicon-on-insulator (SOI) circuits. Using a mono-energetic, collimated, beam of particles the charge deposition was effectively modulated and modeled.

I. Introduction

Radiation induced Single Event Upsets (SEU) in logic and memory circuits continue to be a key issue for advanced CMOS technologies [1]. For high performance 65 nm circuits, the critical charge required to upset the circuit can be very small, making both 65 nm latch and memory circuits susceptible to a wide range of ionizing particles striking the device at many angles. Accurately modeling these upsets is necessary for determining the appropriate device parameters required to obtain both high circuit performance and high reliability.

This paper presents an experimental and modeling study of the critical charge necessary to upset 65 nm silicon-on-isolator (SOI) circuits. The experimental data are obtained using a mono-energetic beam of ions (e.g., alpha, lithium, carbon) from a Tandem accelerator. Using the beam at specific energies and angles (relative to the chip) provides an effective method to control the amount of charge that is deposited in the circuit. We have developed new simulation techniques with which we incorporate realistic geometries of the back end of line (BEOL) materials which is important for the calculations of particle energy loss in nano-scale structures. Using this technique, the circuit critical charge can be accurately determined.

Modeling 65 nm SOI latches and memory circuits for radiation effects is very complex. The methodology used for SPICE [2] simulations and the device parameters used in a SPICE model can make significant differences in the results. A detailed discussion of the SPICE simulations of the 65 nm SOI latches and memory circuits is presented in a companion paper [2]. The device modeling discussed in this paper has been done using Fielday [3, 4]. Fielday can be directly compared to the experimental results including charge deposition, angle and location of the striking particle. SPICE modeling is used for accelerated exploration of voltage, temperature, and manufacturing variability analysis [2, 5].

Section II of this paper describes the experimental set-up used to measure the upsets in the latch and memory circuits. Section III shows examples of measured fail data. The analysis of these data is described in Section IV, explaining how the critical charge of the circuit was extracted from the upset rate vs. angle data. Sections V and VI explain, respectively, the simulation methodology (i.e., the extraction of the critical charge) and Fielday modeling results. Finally, this paper is concluded in Section VII.

II. Experimental setup

The IBM T.J. Watson Research Center has a 3 MV Tandem Van de Graaff accelerator that is used for SEU experiments. The lab has 7 beam lines, with one dedicated for SEU exposures. The ion sources for the accelerator consist of a sputter source (SNICS) for ^{1}H, ^{2}H, ^{12}C and other beams as well as an RF source (alphatross) used to produce the alpha particles (^{4}He) used in this study. Inside the SEU exposure vacuum chamber the wire bonded chip is positioned on a goniometer, where the chip's position and rotational orientation can be adjusted with respect to a mono-energetic beam. The beam is defocused at the plane of the chip. With the chip and particle flux detector translated and rotated out of the way, the defocused beam could be observed on a ZnS viewing screen to ensure that the beam was significantly larger than the exposed chip. A silicon (Si) surface-barrier detector with a 0.5 mm diameter Ta aperture was periodically positioned upstream, with respect to the chip, to monitor the particle flux. The average flux was typically 5E6 ions/cm^2-s. Fig. 1 shows the aperture and surface-barrier detector in front, the chip, rotated with respect to the beam. The ZnS viewing screen is at the rear of the photograph.

Latches or SRAMs were initialized with a known test pattern and then exposed to the beam for a few to 10's of seconds. Subsequently, the data were read and any changes in the initial stored pattern, e.g., from 0 to 1 or from 1 to 0, were recorded. The SEU tester repeated this procedure in an automated fashion for each data state (1 and 0), and for the L1 and L2 latches, at several operating voltages. At a given beam energy, this procedure was repeated for a range of angles with the beam flux monitored both before and after each set of exposures. It was estimated that the orientation of the chip, with respect to the beam is known to about +/- 2^{o}. The surface linear energy transfer (LET) was calculated accounting for energy loss through the BEOL using the measured BEOL thickness, the volume fraction of Cu and insulator per BEOL level and their respective stopping powers. The stopping power calculation is described in Section V.

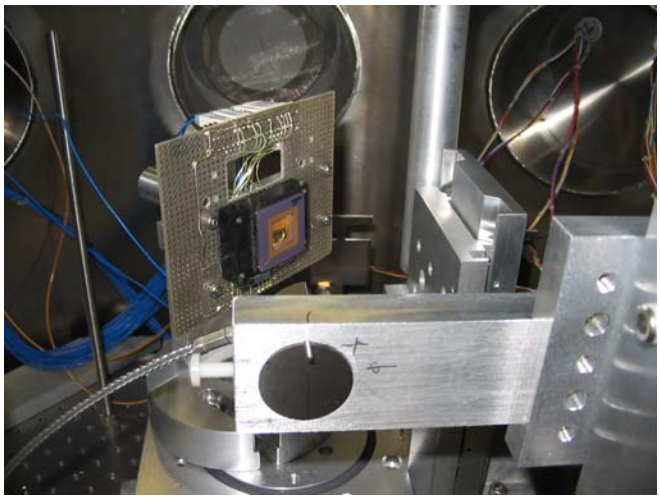

Fig. 1. Device mounted in SEU vacuum chamber.

III. Experimental data

Using IBM's 65 nm SOI technology [6], a series of test sites were built with exploratory latch and array cell (SRAM) designs to study the critical charge needed to upset these circuits. These test sites were built using a limited number of wiring levels with a total BEOL thickness of 11.1 micrometers. The SRAM array data were taken on only one of the 1 Mb array cell designs. More extensive testing was done on the latch designs. Latch data were taken on 16 different latch designs (8 chains, each with an L1 and an L2) in both the data=0 and data=1 state. The data=0 and data=1 states correspond to a ground voltage or a Vdd voltage applied to the scan_in pin of the scan chain. Some of the latch designs were specifically modified to make the circuits very sensitive to alpha particles. Most of these chains consisted of 12,000 L1/L2 latch pairs. Data were typically taken at several voltages ranging from 0.8 - 1.2 V and at several different incident energies.

Fig. 2 is an example of the data obtained on Latch Chain B and shows the fail rate as a function of angle for both data states of the L1 and L2 latches using 5.28 MeV alpha particles. Latch Chain A and Latch Chain B correspond to the low and medium power latches studied in our companion paper [2]. Similar data are shown in Figure 3 using 3.49 MeV alpha particles. These alpha particle energies were chosen to allow for the maximum stopping power of the alpha particle to strike the active region of the device over a narrow range of incident angles. The data shown in Fig. 2, have been normalized with the maximum fail count set equal to 1; the normalization procedure used for Fig 2 was also applied to the data shown in Fig. 3. Higher fail

rates are obtained using the 3.49 MeV alpha particles since these lower energy alpha particles deposit a greater amount of charge in the device Si (at their end of range). As will be explained in the data analysis section, the absolute fail rate is not required to obtain the critical charge of the latch. Tables 1 and 2 show critical angles and the critical charge derived, for two of the latch chains tested in these experiments (Latch Chains A and B). Figures 4 and 5 show some of the data obtained on the SRAM array at normal incidence. Fig. 4 shows fail rates for both data=0 and data=1 as a function of voltage, while Fig. 5 shows the measured fail cross-section (at 0.8 V) as a function of the alpha particle, incident, energy.

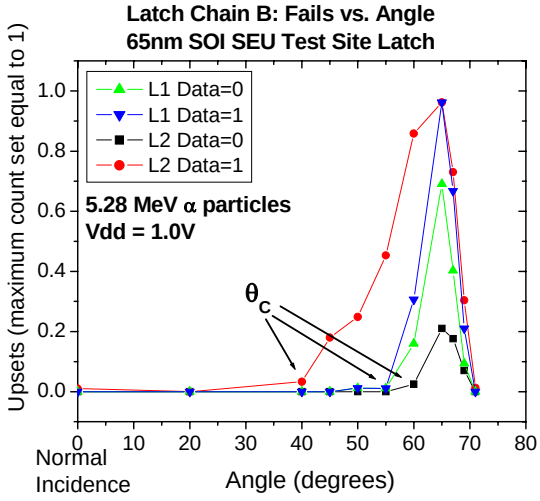

Fig. 2. Latch Chain B - 5.28 MeV alphas.

Data obtained using 5.28 MeV alpha particles		
Vdd = 1 V	Latch Chain A	Latch Chain B
L1 Data = 0	θc = 29 ° Qcrit = 0.5 fC	θc = 57 ° Qcrit = 0.9 fC
L1 Data = 1	θc = 56 ° Qcrit = 0.9 fC	θc = 56 ° Qcrit = 0.9 fC
L2 Data = 0	θc = 53 ° Qcrit = 0.8 fC	θc = 59 ° Qcrit = 1.0 fC
L2 Data = 1	θc = 48 ° Qcrit = 0.7 fC	θc = 42 ° Qcrit = 0.6 fC

Table 1. 5.28 MeV alpha Qcrit.

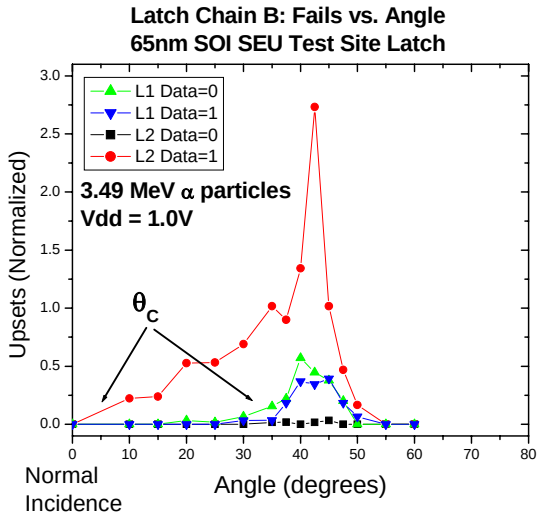

Fig. 3. Latch Chain B - 3.49 MeV alphas.

Data obtained using 3.49 MeV alpha particles		
Vdd = 1 V	Latch Chain A	Latch Chain B
L1 Data = 0	θc = 0 ° Qcrit = 0.6 fC	θc = 27 ° Qcrit = 0.7 fC
L1 Data = 1	θc = 30 ° Qcrit = 0.8 fC	θc = 35 ° Qcrit = 0.8 fC
L2 Data = 0	θc = 27 ° Qcrit = 0.7 fC	θc = N/A
L2 Data = 1	θc = 20 ° Qcrit = 0.7 fC	θc = 17 ° Qcrit = 0.7 fC

Table 2. 3.49 MeV alpha Qcrit.

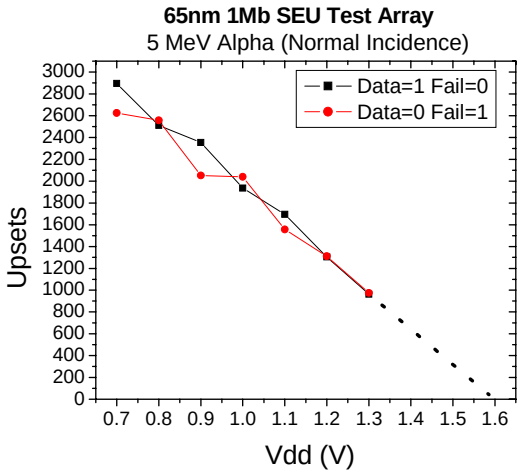

Fig. 4. Upsets in 1Mb SRAM arrays.

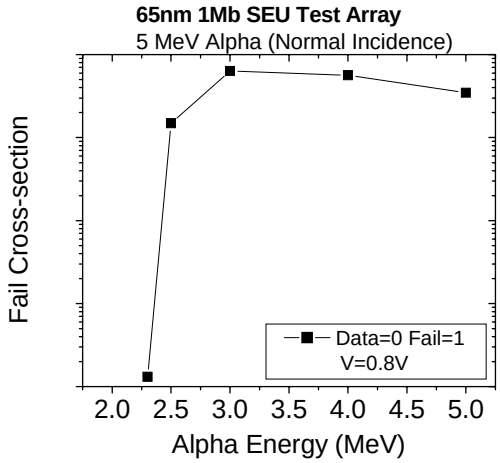

Fig. 5. 1 Mb Arrays; fail cross-section.

IV. Data analysis

For every energy the SEU failure rate (number of upsets per second) was determined for each latch type, data state, operating voltage and angular orientation. The failure rate data were normalized to the beam fluence (flux x exposure time), where the beam flux was determined by the average, just prior and immediately following, an exposure. For reference, $\theta=0^{o}$ means that the beam strikes normal to the chip surface. The failure rate data, for a given beam energy, data state, operating voltage and latch type, were plotted as a function of angle. The critical angle, θc, is defined as the angle at which the failure rate data is about 10% of the maximum value, i.e., where the failure rate data becomes statistically significant. The failure rate data were recorded at several incident energies. In general, at low incident energy, the critical angle is smaller than at larger incident energies. Since the chip itself can be shadowed by the packaging, experiments were not conducted for angles greater than about 75 degrees. Although the critical angle is dependent on the incident energy, the Monte Carlo analysis (Section V) has shown that the critical charge, using these critical angles, is dependent only on the latch type, data state, and operating voltage, i.e., not on the incident beam energy. Tables 1 and 2 show results with significant differences in the critical angle due to the different energy of the alpha particle. However, the critical charge derived from these is very similar.

For the SRAM array data, we observed significant SEU failure rates at zero degrees, *at all incident energies*, so the critical angle analysis as outlined above could not be used. Instead, we plotted the failure rate as a function of operating voltage for both data states. Fig. 4 shows that the failure rate is a decreasing linear function of operating voltage. Our modeling of this device supports this trend. Extrapolating the curve in Fig. 4 to zero fails, one can estimate that this would occur at an operating voltage of 1.6 volts. From the Monte Carlo analysis, one observes the onset of fails at a critical charge of 0.55 fC. One can, therefore, estimate a critical charge of ~ 0.3 fC at the nominal operating voltage of 1.0 volt. Fig. 5 confirms this value of critical charge, since the fail cross-section (fail rate / fluence) rises, from near zero, at an incident alpha energy of > 2.25 MeV (at zero degrees incident angle, the maximum deposited charge from a 2.25 MeV alpha particle beam is approximately 0.3 – 0.4 fC).

V. Simulation Methodology and Extraction of Critical Charge

For a proper estimation of the critical charge from experiments using mono-energetic ion beams, it is essential that the particle transport in the BEOL materials be carefully analyzed. Even though all incident particles have the same initial energy, they start from different, and randomly distributed, points at the top of the irradiated sample due to the large area irradiated with the beam. As such, they move through a variety of paths, due to the complex topologies of the metal wires and other materials above the active Si layer. In reality the ions reach the Si surface with a range of energies because each different path corresponds to a different value of energy loss. Hence each incident angle is, in principle, associated with a distribution of deposited charge in the active node, rather than with a unique value of deposited charge, that one would obtain for a fully homogeneous BEOL. Fig. 6 is a schematic diagram which highlights this situation for a normal incident particle beam.

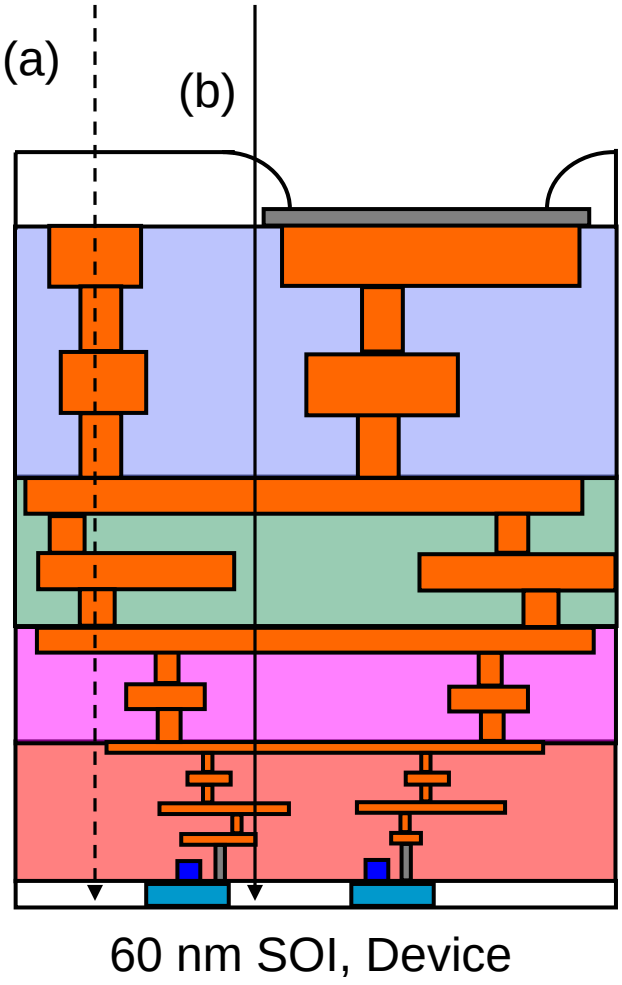

Fig. 6. A typical BEOL, showing metal layers (lines and vias in red) in various dielectric materials. Superimposed are two extreme, normal incident, particle trajectories; (a) a path encountering many metal layers (dashed line) and (b) a path encountering mostly dielectric films (solid line). See text for details.

In the IBM SEU simulation model, SEMM-2 [7], the BEOL is represented by a number of levels, each of which can be either a metal or a dielectric material. However for the analysis of 65 nm SOI devices, for which the critical charge is below 1 fC, such an approach neglects the effects due to the granularity of the metal components, and hence one cannot simulate the deposited charge distribution accurately. To address this issue, a three-dimensional Monte Carlo Heavy Ion Charge Deposition simulator, MCHIDQ [8] was developed. The formulation of the simulation techniques adopted by MCHIDQ will be discussed in detail in forthcoming publications [9]. Here we summarize the main ideas. The MCHIDQ simulation takes into consideration the full BEOL geometry as defined by technology designers. Each level is represented by a number of pixels, the number being typically of the order of 1 million. Each pixel is characterized by a metal fraction parameter. From the coordinates of the pixels and their associated metal fraction parameters one can reconstruct the geometry of each level.

The range of deposited charge as a function of hit angle for a given ion species is estimated in the following manner. Each BEOL level is treated as a homogeneous mixture of metal and dielectric material, with an effective, or mean, LET. The mean LET for each level is computed by invoking the Bragg-Kleeman [10] rule using the metal fractions (per level) from the design. Examples of such calculations are shown by the solid curve in Fig. 7 for 5 MeV alpha particles incident on a 65 nm 1 Mb array. As a first order estimate for the "upper bound" of deposited charge, these calculations are repeated by artificially replacing all of the metal levels with 100% metal. This ensures that the ions travel through the maximum amount of metal. This results in a lower surface energy and, correspondingly, a higher surface LET and deposited charge. An example of an "upper bound" deposited charge is shown by the dashed curve in Fig. 7. As a first order estimate of the "lower bound" deposited charge, the calculation is rerun replacing all of the metal levels with silicon dioxide. This ensures that the ions travel through "soft" paths and results in a higher surface energy, a lower surface LET, and, hence, a lower deposited charge. An example of a "lower bound" deposited charge is shown by the dotted curve in Fig. 7. Combined, the "upper bound" and "lower bound" curves in Fig. 7 give one an estimate of the width of the deposited charge distribution for a given incident particle energy. For the 1 Mb array the deposited charge distribution width is about 0.3 fC for 5 MeV alpha particles and narrows slightly at 7 MeV. The width gradually broadens below 5 MeV. For incident energies between 4.5 MeV and 4 MeV, the "upper bound" curve is lower than the "lower bound" curve. This is because the surface energy is near the Bragg peak of the LET curve (for an alpha particle in Si, the Bragg peak is close to 4.5 MeV). At 4 MeV, the "upper bound" curve in Fig. 7 degenerates to a point at the origin of the plot, which reflects the fact that with a maximum amount of metal in the path, all 4 MeV alpha particles are absorbed in the sample's BEOL.

The Qcrit data entries in Tables 1 and 2 were derived from latch simulations, similar to those shown for the 1Mb SRAM in Fig. 7, with one minor change. The latches were covered with 1.2 um thick pads (20 micrometers on an edge) with an area fill density of 20%. These were purposely ignored from the simulations since alpha particles hitting these blocks of Cu would generally not have enough remaining energy to traverse the BEOL to the device Si. As such, these simulations offer only an estimate of the deposited charge for each incident angle. Once the critical angle was defined the deposited charge was simply read from the graph. In the data Tables 1 and 2 the average deposited charge at a given angle is listed. The approximations used in the calculation the charge deposited are within the experimental uncertainties.

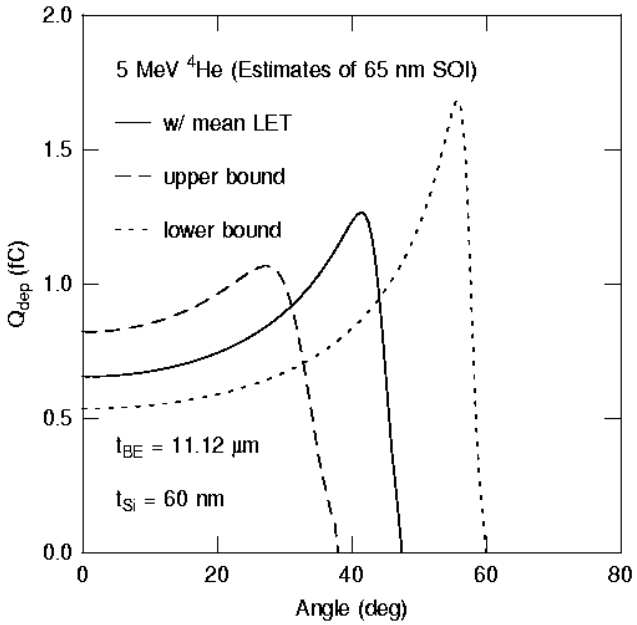

Fig. 7. The calculated deposited charge from 5 MeV alpha particles incident on a 65 nm, 1 Mb SRAM array, as a function of incident angle. The BEOL of this sample has 22 levels of metal and insulator, with a total thickness of 11.12 μm. The thickness of the active Si layer is 60 nm. The solid curve is computed by using a mean LET for each level, see text for details.

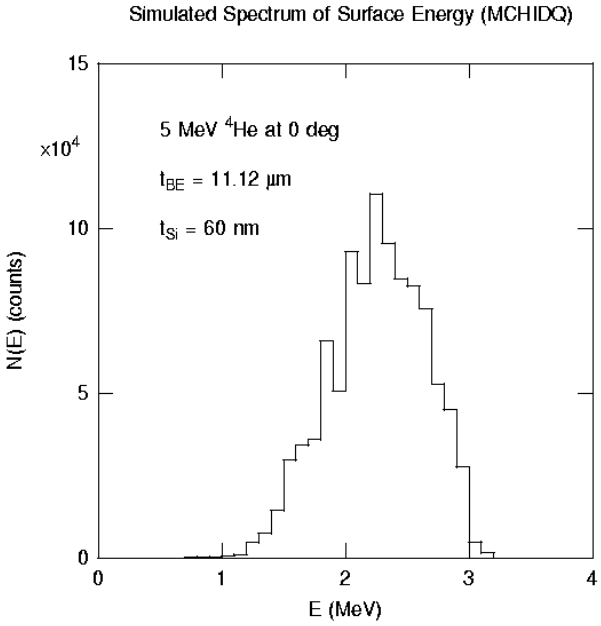

Figure 8. The energy spectrum of alpha particles at the Si surface simulated by MCHIDQ. The irradiated sample is the same as that shown in Fig. 7. The energy of the alpha beam is 5 MeV, and the incident angle is 0 degrees.

An alternative technique, leading to a more accurate answer, involves simulations utilizing the full three dimensional (3-D) BEOL geometry. For these one obtains distributions of both the surface energy and the deposited charge at every incident angle. Fig. 8 shows one such simulated spectrum of the surface energy for normally incident 5 MeV alpha particles on the same SRAM sample described above, in Fig. 7. One million test particles were used. This simulation shows that the energy of the alpha particles at the Si surface has a range of 500 keV (0.5 MeV) to slightly above 3 MeV. Fig. 9 shows the simulated spectrum of the deposited charge for the data in Fig. 8. This 3-D simulation results in a deposited charge range (at normal incidence) of 0.5 fC to 0.85 fC. The mean (or average) deposited charge for this example (at normal incidence) is 0.65 fC. The importance of these results is that there is a real spread in the deposited charge, at a given incident angle, due to the many, different, paths traversed by the high energy particles. The higher deposited charge values (i.e., the high energy tail of these distributions) will cause the initial fails observed when taking data as a function of angle, as shown in Figures 2 and 3.

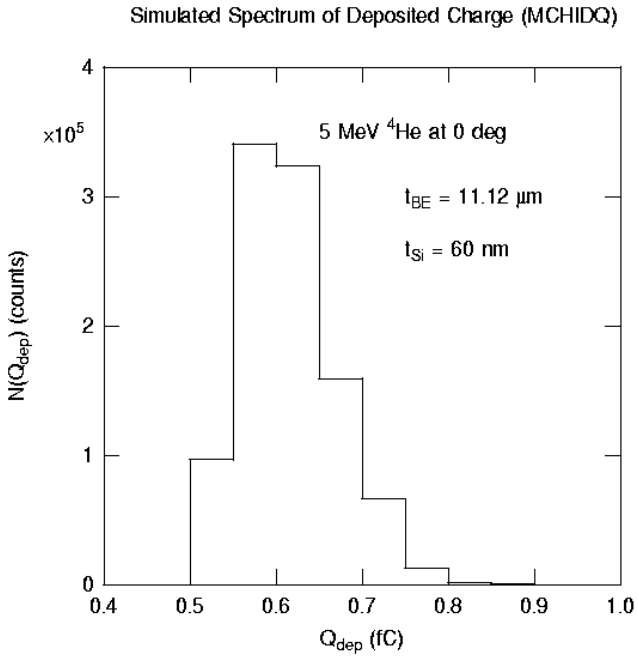

Fig. 9. The spectrum of deposited charge from alpha particles, simulated by MCHIDQ, for the data shown in Fig. 8

VI. Fielday Modeling

Device modeling of single events in small circuits was performed using the mixed-mode capability of Fielday [3, 4]. The L1 latch, as described above, (Chain A) was defined and simulated. The circuit is shown in Fig 10. Device structures were defined using process simulations calibrated to hardware. For most simulations, 2D devices were used and scaled by the device width. The DC operating point of the circuit was first calculated assuming either the data=0 or data=1 state. A transient analysis was then performed of a radiation event in either of the "OFF" devices N03 or P06 for the data=0 state, or devices N06 or P03 for the data=1 state. The radiation event was modeled using an alpha-particle induced charge generation model, calibrated to the data shown in [11]. Typically, simulations such as this require approximately 12-24 cpu-hours to complete on recent vintage AIX workstations.

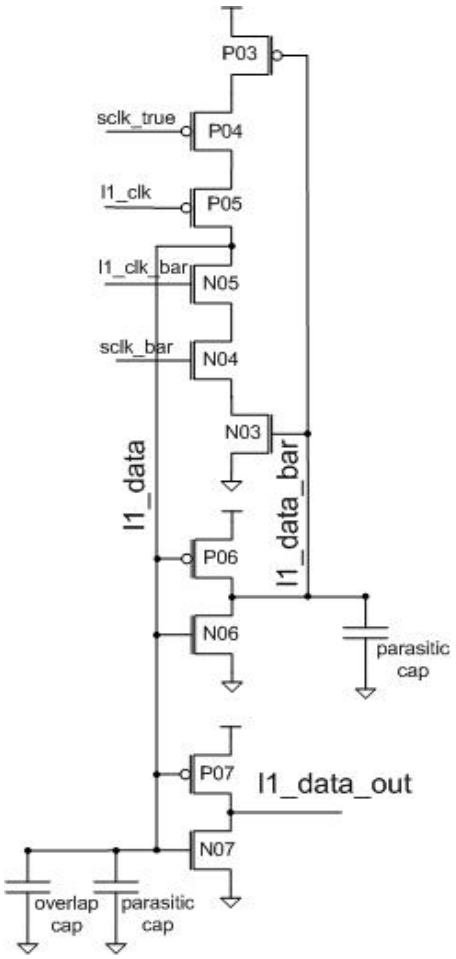

Fig. 10. L1 Latch (Chain A) simulated with Fielday.

The critical charge is determined by assuming that the alpha-particle strikes at normal incidence through the center of the channel. The charge generation model has an adjustable parameter to scale the ionization. A simple binary hunt algorithm is implemented to submit simulation jobs in parallel with different charge scaling factors. Iterations on this scaling factor are performed to determine the charge generation that just causes the logic state to switch. An example of these calculations, for the L1 Latch (Chain A), are shown in Table 3.

Device	Data 0 (fC)	Data 1 (fC)
NFET	0.53	0.98
PFET	1.50	>10.0

Table 3. Critical charge for an L1 Latch (Chain A) at Vdd=1V calculated using Fielday.

The simulation results compare favorably with the measured hardware data (shown in Tables 1 and 2). Using these results, the relative contribution of NFET and PFET strikes to the soft error rate can be quantified using the SEU simulator SEMM2 [7]. These simulation results were further used to help develop a Qcrit model using SPICE, through a detailed comparison of the time evolution of the device contact voltages and internal potentials, as described in [2]. Additional single event simulation studies undertaken were the effects of non-normal incidence strikes including rotation angle, investigation of technology variants, Qcrit in SRAM cells and Qcrit fluctuations due to process variability.

VII. Conclusions

An extensive experimental and modeling study has been completed on special test-site latch designs and SRAM cells built using IBM's 65 nm SOI technology. The circuits were irradiated with alpha beams of various energies delivered by the Yorktown Tandem accelerator. The fail rate was mapped as a function of incident angle and the critical angle inferred. A 3D Monte Carlo model, which incorporates the complex structure of the BEOL and propagates various ion trajectories through this structure, was developed. This model correlates the experimental critical angle with the critical charge needed to upset the circuit. By using a Monte Carlo model, the energy loss was correlated with the critical charge required to upset the circuit. Finally, the SRAM and latch circuits were modeled with the Fielday program. The critical charge determined by these simulations closely matched the experimental results.

The key result of this work is that both SRAM and test-site latch designs built in 65 nm SOI technology can be very sensitive to alpha particles. Many variations of latch designs were tested showing a wide range of critical charge values and sensitivities to alpha particles. With the increasing sensitivity to alpha particles, choosing latch designs consistent with the overall soft error rate for the system will be important.

Acknowledgements

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