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MCM LGA Package with Optical I/O Passively Aligned to Dual Layer Polymer Waveguides in PCB

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Abstract

Over the past 30 years, IBM has provided leadership in high density wiring and high I/O density and I/O count packaging as has been necessary for the high end symmetrical multiple processor (SMP) chips in servers. For example, IBM introduced the multi-chip modules (MCMs) in the 1970s, thermal conduction modules (TCMs) in the 1980s and 1990s, and advanced organic micro-via buildup-layer technology in the 1990s and 2000s [11]. Typical multi-chip modules are necessary to provide the significant increases in bandwidth between chips on the module, compared to the alternative route of lower bandwidth resulting from chip-to-chip bandwidth going through the printed circuit board (PCB) for single chip modules. This results from CMOS chip-to-package pad scaling outpacing the package-to-printed circuit board (PCB) pad scaling. For example, today's mainstream IC–to-package C4 bonding uses 4 mil (thousands of an inch) square pads on 8 mil pitch, with 3-on-6 ramping up, while the package-to-PCB ball- or land grid array (BGA or LGA) pitch uses 1-mm pitch, an areal density as much as 64 times higher. However, even with the larger bandwidth advantage of MCMs, more complex chips such as multi-processor cores and higher bandwidth cache will require a relatively larger number of signal I/Os, as well as more power and ground I/Os. Faster I/O clocks will further exacerbate the need for more package I/O by forcing the transition from previous single ended I/Os to differential signal I/Os to satisfy the higher frequency bit error rate specifications on SMP busses. Our goal is to alleviate the I/O bottleneck at the packaging level in the most cost effective manner, while providing the lowest risk, most flexible development package. To this end, we will present our work on an electrical LGA field replaceable package with optical components. These optical components enable larger I/O bandwidth density between the MCM and PCB than does the electrical I/O bandwidth density.

Motivation for Field Replaceable Optical Modules

The next generation of servers, clusters, supercomputers and switch routers will continue the trend towards higher data bandwidths. Our development of optical interconnects in printed circuit boards (PCBs) is driven by the increasingly severe bandwidth and bandwidth density bottlenecks in these systems [13]. At higher data rates, electrical connections exhibit an increase in crosstalk and attenuation. The usual workaround is to try to optimize everything: the printed circuit board (PCB) material, structure, layout and signal conditioning schemes. Some specific optimizations are: incorporating more uniformly matched and lower dielectric PCB materials; eliminating capacitive reflections from via stubs in PCBs by back-drilling and hidden vias; using differential signaling; increasing trace widths; signal pre-emphasis and conditioning; and forward error correction coding. This strategy only goes so far, however, since it increases unit costs and decreases the electrical signaling density.

In addition, the International Technology Roadmap for Semiconductors (ITRS) also points to the increasing importance of chip packaging and off-chip interconnects. The cost of packaging as a fraction of the overall packaged chip cost has been steadily increasing. Chip packages have increased in pin count at 10% per year while decreasing per-pin cost only 5% per year, yielding a per-chip increase in packaging cost of roughly 5% per year, whereas silicon for mid-level and high end processor systems has provided a performance improvement of four times every three to four years, at a nearly constant cost [13]. These trends illustrate the expectation that many high performance chips will be increasingly limited by off-chip bandwidth, and there will be increasing need for technologies that provide substantially improved chip-to-chip interconnect capabilities. Although multi-chip modules (MCMs) provide significant increases in bandwidth between chips on the module and increased off-module signal I/O count, off-module I/O bandwidth density will eventually be the bottleneck. (MCMs could also be used to package optical components and processor chips together.)

Optical interconnections potentially relieve these intractable bottlenecks. Because of the very great bandwidth and small size of optical waveguides, optical interconnects provide enormously higher bandwidth density. Moving to optics requires the resolution of a number of open questions, however, and these are a major focus of our work. In particular, to address the need of high bandwidth parallel links to I\/O buses, memory buses, and particularly symmetric multiprocessor (SMP) or system buses, we have realized multimode polymer-based waveguides on PCBs that have propagation losses below 0.04 dB/cm at a wavelength of 850 nm and 0.12 dB/cm at 980 nm [12]. Transmission measurements at a data rate of 10 Gb/s over a 1-m-long waveguide show good eye openings, nearly independent of the in-coupling conditions. For the field replaceable optical

MCM investigated here, the transmitter and receiver array assembly utilizes low cost via flip-chip-positioning on the top of the carrier. The coupling concept is based on the collimated-beam approach with microlenses in front of the waveguide and the optoelectronic components. As we aim for large multi-layer two-dimensional waveguide arrays, optical crosstalk and optical efficiency are important parameters to be understood. Accordingly, we have measured optical crosstalk and optical efficiency for several arrays of optical channels coupled via a passively aligned field replaceable MCM down to several layers of polymer waveguide. The influence of misalignment at the transmitter and the receiver side on optical crosstalk and optical efficiency will be presented as a function of the misalignment tolerances between waveguide and transmitter/receiver. Field replaceability is also incorporated into the optical MCM as an attractive attribute to accommodate required field upgrades, needed repairs with minimal downtime, the diagnosing of performance problems. In addition, the ability to remove and replace optical MCMs is ideal in the development environment where the VCSEL diode failure in time (FIT) needs to be established with minimum impact to an SMP bus downtime.

This paper presents a novel electrical MCM LGA package with optical I/O along with mechanical, electrical and optical measurement. In addition, resulting package attributes covered include (1) field replaceabilty, (2) compatible with multi optical layer PCB interconnects, (3) optical transceiver and receiver I/O in the same package (4) close proximity between optical transceiver/receiver and high frequency electrical chip I/O, and (5) low cost compatible passive alignment with electrical LGAs. To our knowledge, this is the first reported field replaceable, electrical MCM with additional optical I/O passively aligned to multi-layer polymer waveguides (PWGs).

Optical Transceiver Packages Coupled to Waveguides

In a previous publication [1,3,7], we reported in more detail on a 1x4 array of either a transceiver or receiver package where the optical coupling resembles the layout of today's commercial transceiver/receiver optical subassemblies as used for fiber based parallel optical interconnects, namely the VCSEL/PD array is butt coupled and in plane with the optical channels. For today's fiber cables, in plane optical coupling is above and parallel to the PCB whereas with PWG, in plane optical butt coupling of the transceiver package may be in the PCB. An electrical polyimide flex allows the 90 Degree electrical bend from a vertical mounted in-board transceiver or receiver package to electrically BGA contact the top horizontal surface of the PCB.

Earlier [2,4,5,6], we reported on various aspects of a 4 x 12 array of either transceiver or receiver package in the DARPA Terabus project. These used downward-looking vertical cavity self emitting laser/photo detector (VCSEL/PD) arrays, each of whose elements has an integrated semiconductor focusing lens whose axis is perpendicular to the board. The PWGs lie in the plane of the board, and each is coupled to its corresponding VCSEL or PD by an individual 45-degree turning mirror. The 985nm wavelength of the GaAs VCSEL/ InP PD allow bottom side optical interfacing with C4 topside electrical contact to the bottom of a Driver/TIA IC. The larger area Driver/TIA IC would allow peripheral bottom side IC C4 bonding to the topside of on organic or silicon carrier, which in turn is BGA to a PCB.

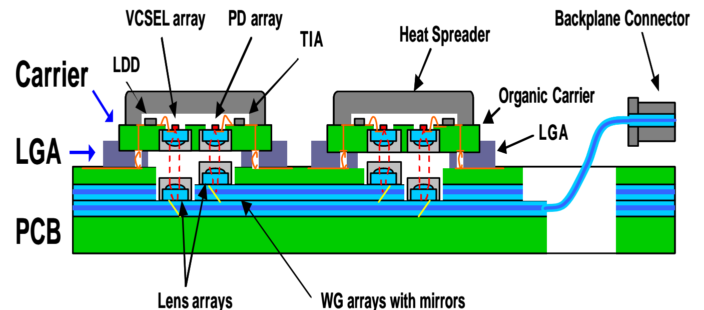
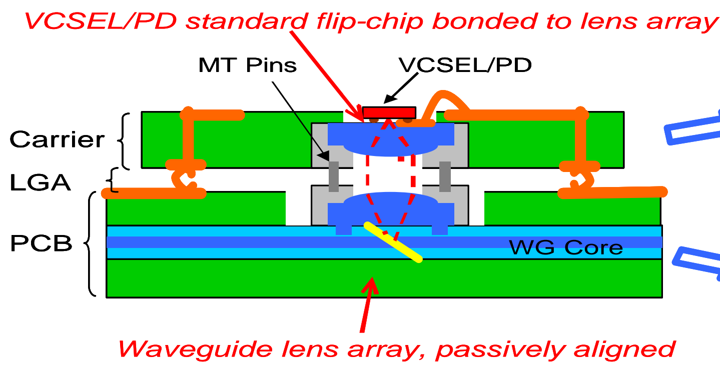


Figure 1: Cross-section of drawing depicting two electronic chip carriers with integrated optical interconnects mounted on PCB with two imbedded (1x12) PWG layers and a backplane connector

Here we report on a third transceiver/receiver package design that consists of an electrical LGA module with integrated optical interconnects, fitting into an LGA socket. Figure 1 shows a cross-section drawing of two such LGA modules in LGA sockets with the integrated optical interconnects consisting of a dual lens array. Each LGA module contains a 1x12 10Gb/s VCSEL array and a 1x12 PD array, thus being able to provide a both transceiver and receiver optical functions. Dual lenses between the E/Os and PWG provide tolerance budget in the *Z* (perpendicular to PCB) dimension of hundreds of microns since the light is collimated between the lenses. Dual layer PWG layers of 250 ?m core pitches were implemented.

The socket presented here is an InterCon Systems model 7731 LGA socket, an off-the-shelf device using metal *C*-spring contacts, modified by adding a central cavity opening of 9mm x 9mm and populating only a subset of the *C*-springs: 3 rows of 19 contacts repeated on four sides for a total of 228 contacts. Each contact requires approximately 500 mN of compression force or a total of 115 N per LGA module.



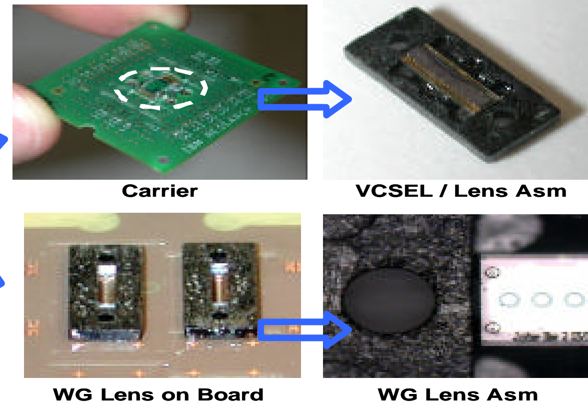
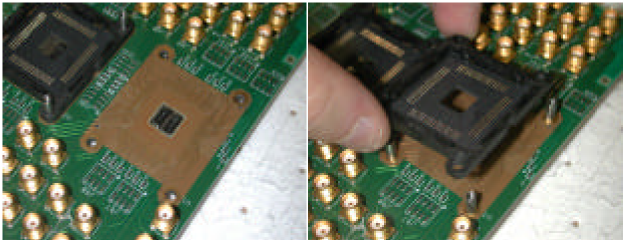
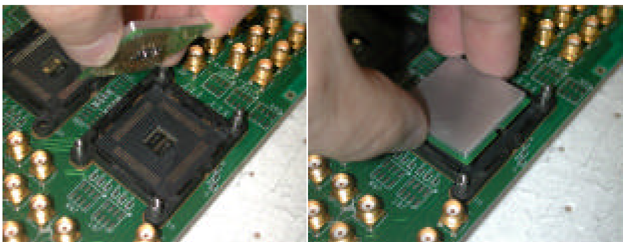


Figure 2: Carrier passive alignment concept implemented.

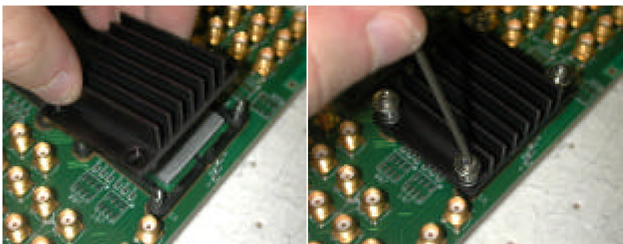
Figure 2 shows the passive alignment concept. First, the VCSEL/PD chips are flip-chip bonded onto a glass lens array that contains metal pads for the flip chip bonding and pad for later wire bonding to the carrier. The lensed assembly is then mounted on the organic carrier by a pick-and-place machine and secured with epoxy. Thirdly, the pads on the assembly and carrier are wire-bonded to each other.



(a) (b)



(c) (d)



(d) (f)

Figure 3: Photographs showing the LGA assembly process starting with (a) the PCB embedded two layers of PWG, (b) pick and place of the ~ 40mm x 40 mm LGA socket, (c) pick and place of the LGA module, (d) heat shield, (e) heat sink and (f) four corner bolts with springs.

After board fabrication, the waveguide mirrors are ablated along with the passive alignment features into the PWG core layer. A second set of lens array assemblies (not containing VCSELs/PDs) are passively aligned by pick-and-place, so that the male alignment features on the lens assembly fit into the female features ablated into the PWG level and are bonded into place with epoxy. The lens/PWG alignment is controlled by the alignment of the ablated features in the PWG level. The laser ablation tool aligns to fiducials photo-patterned directly on the core layer along with the waveguides. Lastly, the LGA socket is picked and placed onto the PCB, and two MT ferrule pins for each lens assembly provide the fine alignment between the carriers contain the E/Os and the PWG attached lens assembly, while the LGA electrical pins provide the coarse alignment.

Figure 3 shows a quick pick-and-place LGA assembly sequence that meets electrical and optical tolerances, starting with a metal stiffener plate beneath the PCB with its two embedded waveguide layers, each containing twelve 35-?m-square cores on a 250-?m in-layer pitch, and upper and lower cladding of 58 ?m with 65 ?m of intermediate (between cores) cladding, yielding a 309-mm vertical pitch, for an areal density of 1300 channels/cm^2. Figure 4 shows the PCB cross-section containing the two PWG layers with staggered waveguide cores.

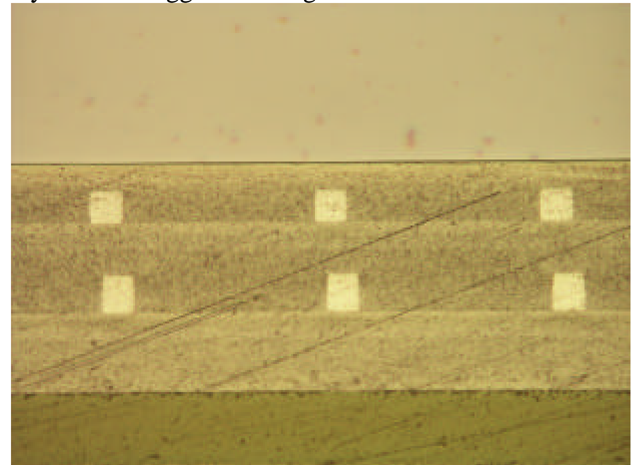


Figure 4: Photograph showing cross-section of PCB containing dual layer PWG, 2 x 12 channels, 35?m cores.

Alignment Sensitivity Test Module and Results

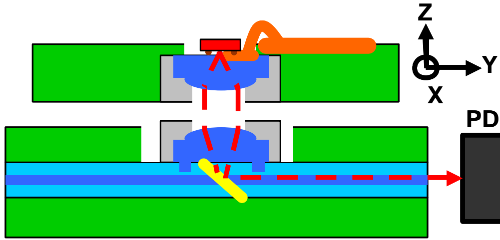


Figure 5: Carrier Alignment Sensitivity Test Set-Up

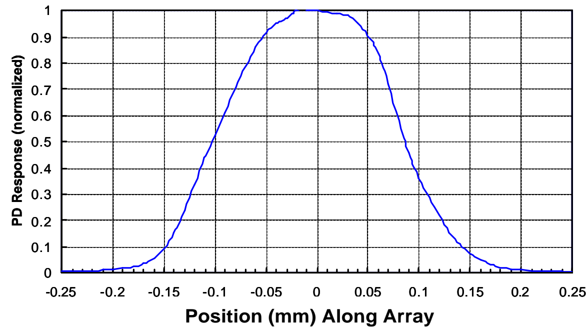


Figure 6: Photodetector Response versus LGA Carrier Position

The dependence of coupling loss on in-plane carrier misalignment was measured by using a translation stage to move the LGA carrier in *Y* (perpendicular to the PWG axis) and measuring the optical coupling efficiency at the PCB edge via a large photodetector. The results of this measurement are summarized in Figure 5. The results of Figure 6 show that a large carrier *Y* offset of +/- 50 ?m leads to a 0.5-dB reduction in coupling efficiency. In actual practice, the MT alignment pins hold alignment to better than +/- 10 ?m., so lateral misalignment is not expected to be a limiting source of loss.

Since the waveguides are square and the packaged optical components are symmetrical, the dependence on misalignment in X should be very similar.

Package Type	Optical Components	Optical Loss (best components fabricated) (dB)
LGA	Lens coupling (Tx)	< 1.0
	Mirror coupling (Tx)	< 0.5
	Lens coupling (Rx)	< 1.0
	Mirrir coupling (Rx)	< 0.5
	Total	< 3.0 + PWG

Table 1: LGA optical link coupling loss

Table 1 shows the measured maximum optical loss from good components. It is important to note that total optical losses can result from several sources, such as any mechanical misalignment of components in the optical path in assembly or over operating temperature, fabrication quality, and material limitations.

Reproducibility Test Module and Results

A test module was built to quantify module to substrate alignment accuracy and repeatability. There are two passively aligned parts that come together, namely (1) the laser ablated test pattern, and (2) the alignment test module. The repeatability procedure requires first that MT alignment holes of 700 ?m diameter are procession-ablated in the PCB. Second, the corresponding test module with reference plate is passively (pick-and-place) inserted into holes in the PCB. Lastly, a vision system measures the test module to PCB relative to position. We find that the MT pins guide the test module to within a few microns of the desired position. The total misalignment budget allowed is +/- 5 to 7 ?m. Individual pick and place results are shown in Figure 7 with statistics shown in Table 2 and demonstrating that the 1-? placement error between the alignment test module and the polymer/metal film is better than 2 ?m.

Board	X-Plane placement		Y-Plane placement	
	Avg. [um]	s [µm]	Avg. [um]	s [µm]
C	0.66	1.30	0.98	0.78

Table 2: Test module placement to PCB/WGs relative position for four sites measured, six locations per site

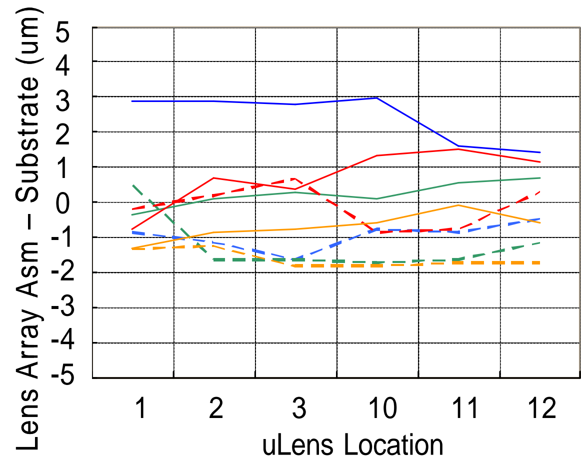


Figure 7: Lens Array Asmembly minus PCB as a function of the 1 x 12 ulens array.

Field Replaceability Robustness Measurements

LGA carrier field replaceability is also of practical interest, and in some systems, a necessity. For some examples in the datacom industry, not only does field replaceability needs to be quick to minimize system downtime, but also needs to be passively aligned since the field replaceable modules do not have the aid of controlled mechanical and temperature environments of known calibrated and stable lab bench-top tooling for alignment. Passive alignment also is more cost effective. Traditionally, adequate compression force was achieved by controlling the tightening torque on the load screws, which ensured low electrical contact resistance between

the gold plated pads on the bottom of the LGA carrier and the top of the LGA socket's metal springs, and between the gold plated pads on the top of the PCB and the bottom of the LGA socket's metal springs. The maximum permissible *X* or *Y* displacement of the pads with respect to the metal spring, after deflection, over the operating temperature range that still ensures electrical contact is on the order of 100 ?m. As noted earlier, 228 spring-to-pad contacts provided the signaling, power and ground, with an applied compressive force of approximately 115 N. No effect from the compressive force on the optical I/O was measurable. We have already seen that the two MT ferrule pins provide the tighter tolerance required to maintain high optical efficiency. It is interesting to note that the electrical contact is a make or break catastrophic change, whereas the optical alignment has more of a gradual optical signal efficiency transmission roll-off, helped in this regard by having the optical beam expanded from about 50 ?m diameter at the VCSEL and WG cores, to 150-200 ?m between the collimating lenses. Results of numerous re-makes (~ 20X) of the LGA carrier re-inserted into the LGA socket frame, and fully-torqued LGA load screws shows no discernible coupled optical power efficiency loss. We speculate that the field replaceability limitation would be the result of the same mechanism wear as electrical LGAs without the optical components, i.e., the LGA metal spring scrubbing contact with the thinner gold electrical pads on the LGA carrier would eventually produce a higher electrical resistance/open contact.

Vector Network Analyzer Measurements

The 10 Gb/s/channel 1x12 Avalon VCSELs and the 1x12 Albis PD arrays had been used [8,9]. To ensure acceptable electrical and optical signal-to-noise and cross-talk server system package specification compliance from our various design parameter choices, it is important to isolate in measurement the individual contributions of various electrical-to optical-to electrical link components. These components include (1) the VCSEL/PD arrays and corresponding driver/TIA ICs with the corresponding flip chip bonding metallurgy and structure, from the package performance.

For proper high frequency electrical characterization, the high frequency path characterized included the total electrical path as shown in Figure 8: (1) the FR4 PCB containing the two layer PWG, i.e., from the PCB edge SMA connectors, over the differential 1 ounce copper signal traces, to the LGA socket pads; (2) the LGA socket that contains the metal springs; and (3) the FR4 LGA carrier, i.e., from the bottom side LGA socket pads, over the differential 0.5-oz (18-?m thick) copper signal traces, through a 0.5-oz copper plated-through via, and the top side VCSEL or PD array anode and cathode pads.

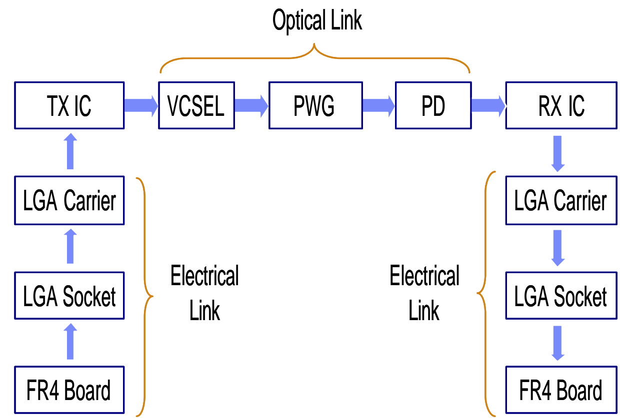


Figure 8: Block diagram of component makeup in electrical-optical-electrical link.

An Agilent E8364A Network Analyzer was employed to carry out the vector network analyzer approach. The first step is to perform 4-port probing measurements on the LGA carrier, followed by the 4-port coaxial measurement on the PCB plus the LGA socket, plus the LGA carrier. There are 24 differential pairs per LGA carrier to represent the anode and respective cathode of the 1 x 12 VCSEL and 1x12 PD array, and two LGA sockets for every dual layer PWG PCB. This total of 48 differential pairs per PCB provided an abundance of opportunity to characterize various tradeoffs affecting the differential strip line properties that result from various PCB, LGA sockets and LGA carrier layout and component technology variations. The E8364A can produce simulated eye diagrams from its measurements, and that capability was used here.

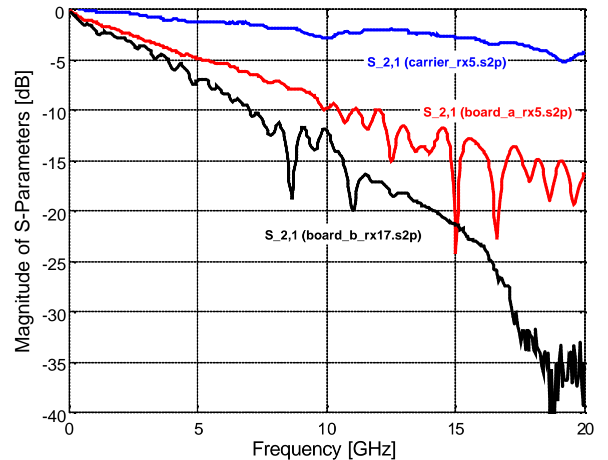


Figure 9: S-Parameter S21 magnitude versus frequency for the carrier plus LGA, and two PCB plus carrier plus LGA.

Figure 9 shows the simulated eye diagram for the carrier at 10Gb/s data rate having > 90% eye opening and < 10ps jitter, and being quite acceptable. Comparing

Figures 10 and 11 shows that most of the eye closure is a result of the PCB and not the package, which is as expected since preserving signal integrity at 10Gb/s in standard FR4 board technology is very challenging.

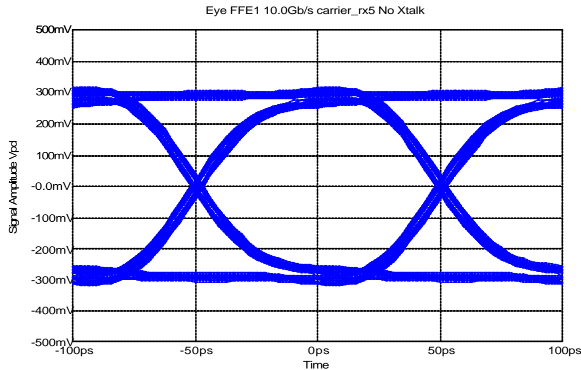


Figure 10 : Calculated eye-diagram based on measured S-parameters for carrier.

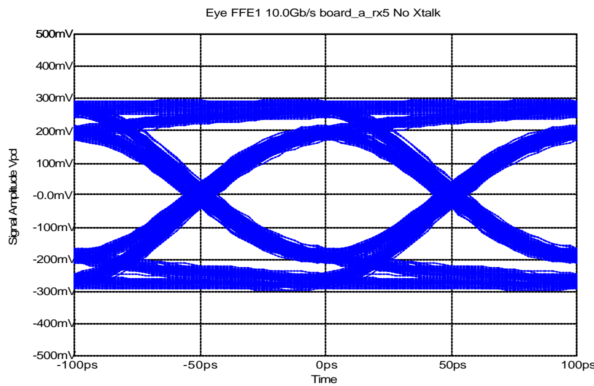


Figure 11: Calculated eye-diagram based on measured S-parameters for PCB, LGA Socket and carrier (entire electrical link, one side).

Time Domain Reflection Measurements

An Agilent 86100B wide-bandwidth oscilloscope was employed to carry out the time domain reflection (TDR) and time domain transmission (TDT) approach. The TDR is an impedance matching and differential channel balance. Two-channel probe measurements were made on the carrier, and two-channel coaxial measurements on the full path of PCB + LGA + carrier, for three different carrier signal layouts. Length of carrier traces from layout are Case 3 < Case 2 < Case 1. Figure 12 shows the calculated impedance mismatch of carrier traces: Case 3 is the best match, while Case 1 is the worst. This calculation assumes that the mismatch is resistive, and resolution is degraded with distance from the probe, since the edges become progressively slower. (This is quite unlike the vector network analyzer, which is phase sensitive, whereas the oscilloscope is not.)

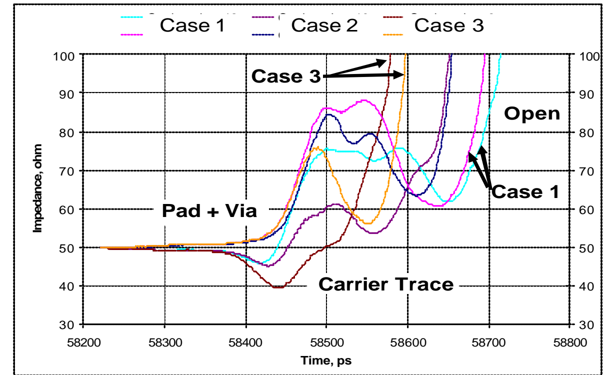


Figure 12: Calculated impedance versus time delay from TDT measurements.

Time Domain Transmission Measurements

The TDT is a transition-time degradation approach. Four-channel probe measurements were made on the carrier, and 4-channel coaxial measurements on the full path of PCB + LGA + carrier. Figure 13 shows measurements on the carrier, consisting of the LGA pad, via, carrier trace to wire-bond PAD show results on three various carrier signal layouts. Carrier double link transition time shows rise and fall times T_r = 258 ps and T_f = 162 ps in Case 1, and T_r = 145 ps and T_f =91 ps in Case 3, roughly as expected from the layout differences mentioned earlier

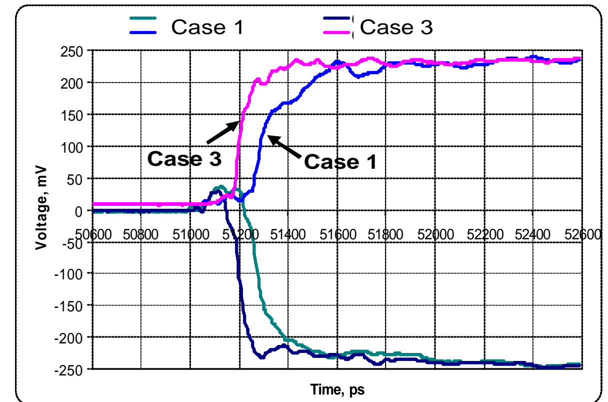


Figure 13: TDT measurements of voltage as a function of time delay for two different carrier signal layouts.

Conclusions

A novel field-replaceable electrical carrier with integrated optical transceiver/receiver function in a single package has been demonstrated. The complete package characterized here is an electrical and optical I/O LGA that incorporates commercially available 1x12-channel, 10-Gb/s/channel VCSEL and photodiode arrays, flip-chip bonded to a glass lens array, passively aligned to a low-cost organic carrier that interfaces to a PCB via a minimally-modified LGA socket. In addition to normal copper traces, the PCB contains two PWG layers of 12 channels each, at a 8-channel/mm density and of 20-cm length, with 45-degree turning mirrors on 125-?m pitch to

couple between the (horizontal) waveguides and the downward-looking lens arrays. The assembled package has an aluminum heat shield and a heat sink, both of which are compatible with normal LGA module practice. The assembly performs well electrically at up to 10 Gb/s/channel, at a 1300 channel/cm^2 density, yielding a calculated raw bandwidth areal density of 13 Tb/s/cm^2. In addition to high performance and high density, the key advantages to our approach are: simple passive alignment; ability to tolerate lateral and vertical placement errors several times worse than those measured; thermal expansion matching; field-replaceability; and potentially low cost due to the use of minimally modified standard PCB and connector technology.

The emphasis was to use high volume existing field replaceable electrical packaging, such as an organic carrier in an LGA socket, and to demonstrate the compatibility when incorporating optical I/O to/from the PWG layer(s) embedded in a PCB. The compatibility is demonstrated in preserving the same LGA packaging parts and assembly, including the desired pick-and-place passive alignment onto the PCB. This result in a multi-chip-module that not only contains traditional electrical ICs, but also contains electrical/optical ICs, such as VCSELs and PDs and the respective drivers and amplifier ICs on the same carrier. This eliminates the additional transceiver and receiver packages and frees up valuable PCB real estate, which becomes more costly in higher end datacom applications

Electro-optical LGA transceiver/receiver interconnect package and several other intra-system optical interconnect programs are an initial step towards a complete technology for chip-to-chip or board-to-board optical buses. The results as summarized above are promising and demonstrate that such interconnects are possible. However, much additional qualification work needs to be carried, such as reliability and aging before a complete commercial technology becomes realistic.

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