RC23914 (W0603-104) March 15, 2006
Electrical Engineering

IBM Research Report

Silicon on Insulator CMOS with Hybrid Crystal Orientation Using Double Wafer Bonding

K. K. Chan, M. Yang, L. Shi, A. Kumar, J. A. Ott, J. Patel, R. Schulz, H. Kry, Y. Zhang, E. Sikorski, W. Graham, B. To, S. Medd, D. Canaperi, J. Newbury, C. Scerbo, R. Meyer, C. D'Emic, M. Ieong
IBM Research Division
Thomas J. Watson Research Center
P.O. Box 218
Yorktown Heights, NY 10598

Research Division
Almaden - Austin - Beijing - Haifa - India - T. J. Watson - Tokyo - Zurich

LIMITED DISTRIBUTION NOTICE: This report has been submitted for publication outside of IBM and will probably be copyrighted if accepted for publication. It has been issued as a Research Report for early dissemination of its contents. In view of the transfer of copyright to the outside publisher, its distribution outside of IBM prior to publication should be limited to peer communications and specific requests. After outside publication, requests should be filled only by reprints or legally obtained copies of the article (e.g., payment of royalties). Copies may be requested from IBM T. J. Watson Research Center , P. O. Box 218, Yorktown Heights, NY 10598 USA (email: reports@us.ibm.com). Some reports are available on the internet at http://domino.watson.ibm.com/library/CyberDig.nsf/home .

Silicon on Insulator CMOS with Hybrid Crystal Orientation Using Double Wafer Bonding

K. K. Chan, M. Yang, L. Shi, A. Kumar, J. A Ott, J. Patel, R. Schulz, H. Kry, Y. Zhang, E. Sikorski, W. Graham, B. To, S. Medd, D. Canaperi, J. Newbury, C. Scerbo, R. Meyer, C. D'Emic, and M. Ieong
IBM Semiconductor Research and Development Center,
Research Division, T. J. Watson Research Center, Yorktown Heights, NY 10598
Email: kkchan@us.IBM.com, Phone : (914) 945-3166, Fax : (914) 945-2141

Carrier transport depends critically on MOSFET channel orientation, with electron mobility highest on the conventional Si (100) surface while hole mobility is more than 2x enhanced on the Si (110) surface [1]. CMOS on substrates composed of multiple surface orientations have been demonstrated—nFETs on the (100) surface orientation and pFETs on the (110) surface orientation –yielding pFET drive current enhancement of 30% at 45nm channel length [2]. However, in most of the previous publications on Hybrid Orientation Technology (HOT), nFETs were fabricated on silicon-on-insulator (SOI), but pFETs were bulk-like. The implementation of this HOT technology is therefore limited by the design changes during technology transfer. Furthermore, it is known that CMOS on SOI provides higher performance than conventional bulk device due the elimination of area junction capacitance (C_{ja}), the lack of a reverse body effect in stacked circuits and the slightly forward biased SOI body under the nominal operating voltage range. In this paper, we present a novel SOI CMOS structure on hybrid orientation substrates through double wafer bonding.

The fabrication process of a hybrid orientation substrate for SOI CMOS using double wafer bonding is illustrated in Fig. 1. A 40 nm thick oxide were grown on a (100) SOI wafer (wafer B), with the final SOI thickness of 55 nm. Then a (110) SOI wafer (wafer A), which thickness was thinned down to 25nm by thermal oxidation, was flip-bonded to wafer B at room temperature and then annealed at a high temperature to strengthen the bonding. The entire handle substrate of wafer B was removed by grinding and wet etching in KOH solution. The buried oxide on wafer B provided as an etch-stop for the silicon etching and was removed afterwards. The final substrate consists of a 55 nm (100) SOI film and a 25 nm (110) SOI film with a 40nm thick oxide in between. Fig. 2 shows the x-ray diffraction measurement on a hybrid orientation substrate with 56nm (100) SOI and 25nm (110) SOI. The fabrication of SOI CMOS on a hybrid orientation substrate is similar to that reported in Ref. [1] (see Fig. 3). Following the patterning of substrate, reactive ion etching was used to delineate a trench, stopping on Si (110) surface. A spacer was formed and defect-free silicon was grown from (110) silicon surface. Then, the surface of (110) epi-Si was planarized and recessed to the (100) silicon surface by chemical-mechanical polishing and oxidation/stripping. A high resolution TEM micrograph (Fig. 4) shows no oxygen residue at (110) SOI and epitaxial silicon interface. The process of SOI CMOS was resumed with shallow trench isolation, 1.1nm gate oxide thickness, around 80nm channel length, Ni silicide and Cu metal level. The final structure is shown in Fig. 5 with nFETs on 55nm (100) SOI and pFETs on 120nm (110) SOI.

Improvement of pFET drive current is observed. Fig. 6 gives the I_{on} vs. I_{off} characteristic of SOI CMOS fabricated on a hybrid orientation substrate at 1.0V supply voltage. At 10nA/μm off current, pFET drive current is 370μA/μm on the (110) SOI, and 230μA/μm on a control wafer fabricated simultaneously. nFETs fabricated on the same wafer on (100) SOI shows drive current of 920μA/μm at I_{off}=10μA/μm. The output and subthreshold characteristics of these SOI CMOS on a hybrid orientation substrate are shown in Fig. 7. The subthreshold slope is 89mV/dec and 96mV/dec for pFET and nFET, respectively.

In summary, we have demonstrated a novel SOI CMOS structure on hybrid orientation substrates using double wafer bonding technique. At 80nm channel length, pFET drive current is improved by 60% at 10nA/μm off current and 1.0V supply voltage.

---

[1] M. Yang, *et. al.*, *IEDM Tech. Dig.*, pp453 (2003). [2] C. Sheraw, *et. al.*, *Symp. on VLSI Tech. Dig.*, pp12 (2005).

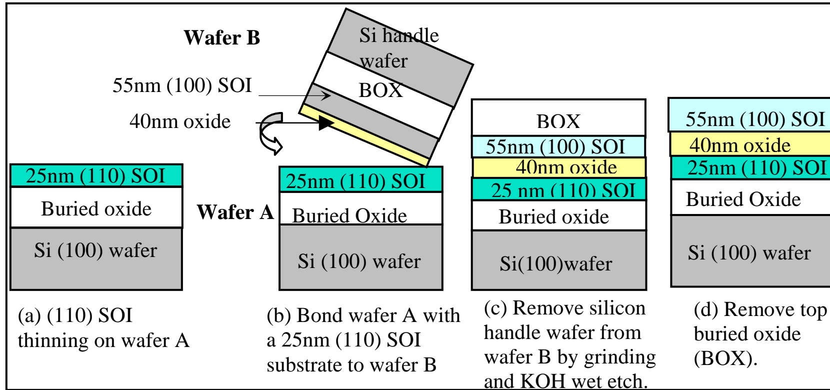

Fig. 1 Fabrication of a hybrid orientation substrate for SOI CMOS using double wafer bonding.

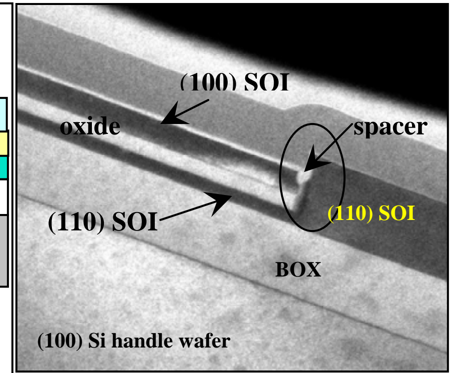

Fig. 4 Cross-sectional TEM micrograph of SOI CMOS with hybrid orientation after silicon epitaxy and CMP.

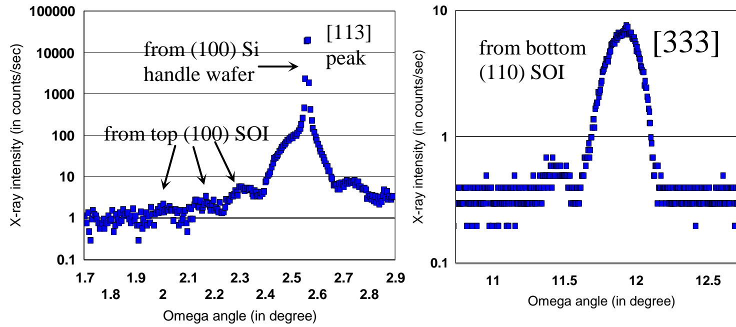

Fig. 2 X-ray diffraction measurement from a double bonded hybrid orientation substrate with a 56nm (100) SOI on top and a 25nm (110) SOI at bottom.

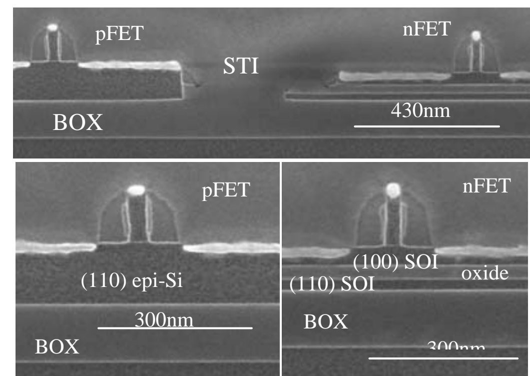

Fig. 5 Cross-sectional SEM of SOI CMOS on a HOT substrate using double wafer bonding technique. Note that pFETs are on 120nm (110) SOI and nFETs are on 55nm (100) SOI.

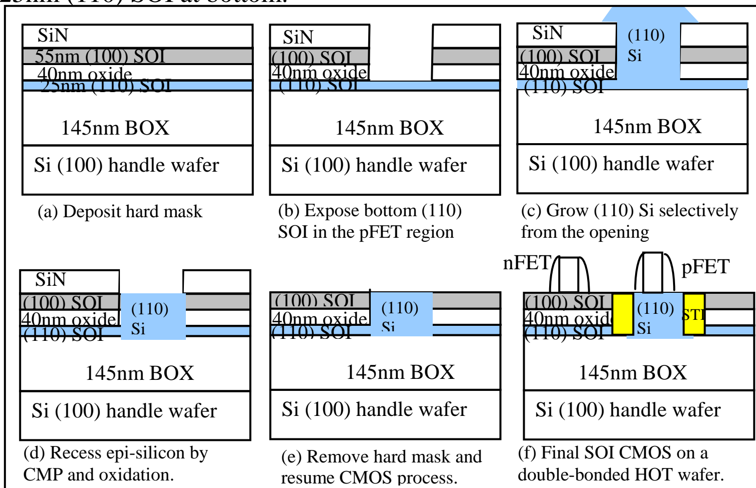

Fig. 3 Process flow of SOI CMOS fabricated on a hybrid orientation substrate.

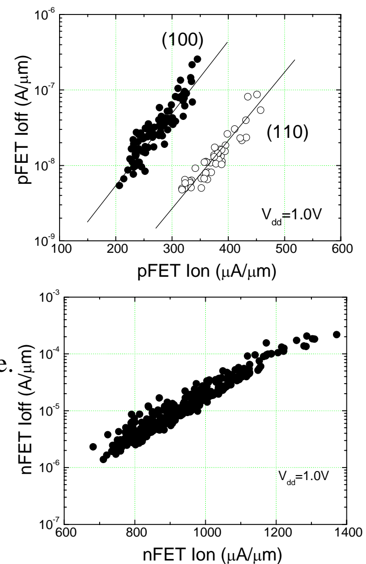

Fig. 6 I_{on} vs. I_{off} characteristics of SOI CMOS fabricated on a hybrid orientation substrate using double wafer bonding.

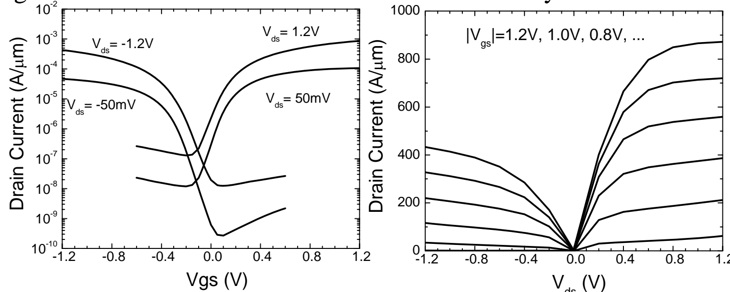

Fig. 7 Output and subthreshold characteristics of SOI CMOS fabricated on a hybrid orientation substrate using double wafer bonding.