RC23932 (W0604-041) April 10, 2006
Materials Science

IBM Research Report

High Mobility Channels for Ultimate CMOS

D. K. Sadana, S. Koester, Y. Sun, E. Kiewra, S. W. Bedell, A. Reznicek, H. J. Hovel, J. Ott, K. Fogel
IBM Research Division
Thomas J. Watson Research Center
P.O. Box 218
Yorktown Heights, NY 10598

D. J. Webb, J. Fompeyrine, J.-P. Locquet, M. Sousa, R. Germann
IBM Research Division
Zurich Research Laboratory
Säumerstrasse 4
Posfach, CH-8803 Rüschlikon
Switzerland

Research Division
Almaden - Austin - Beijing - Haifa - India - T. J. Watson - Tokyo - Zurich

LIMITED DISTRIBUTION NOTICE: This report has been submitted for publication outside of IBM and will probably be copyrighted if accepted for publication. It has been issued as a Research Report for early dissemination of its contents. In view of the transfer of copyright to the outside publisher, its distribution outside of IBM prior to publication should be limited to peer communications and specific requests. After outside publication, requests should be filled only by reprints or legally obtained copies of the article (e.g, payment of royalties). Copies may be requested from IBM T. J. Watson Research Center , P. O. Box 218, Yorktown Heights, NY 10598 USA (email: reports@us.ibm.com). Some reports are available on the internet at http://domino.watson.ibm.com/library/CyberDig.nsf/home

High Mobility Channels for Ultimate CMOS

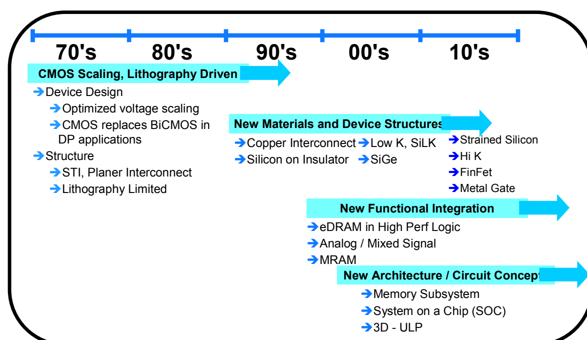
D.K. Sadana[1], S. Koester[1], Y. Sun[1], E. Kiewra[1], S. W. Bedell[1], A. Reznicek[1], H.J. Hovel[1], J Ott[1], K. Fogel[1], D. J. Webb,[2] J. Fompeyrine,[2] J.-P. Locquet,[2] M. Sousa,[2] and R. Germann[2]
[1]T.J. Watson Research Center, Yorktown Heights, NY 10598,
[2] IBM Zurich Research Laboratory, Säumerstrasse 4 / Postfach , CH-8803 Rüschlikon, Switzerland

Email: dksadana@us.ibm.com

Performance enhancement in successive CMOS technology generations in the past was driven by device scaling and lithography. In the 90s, however, new materials and device structures became the key enablers for CMOS performance enhancement (in conjunction with scaling). Figure 1 lists the key performance enablers for various generations of CMOS technology from the past to the present.

Presently, CMOS scaling is facing a formidable challenge due to a number of factors including increasing gate leakage current, rising active power due to non-scaled voltage, band-to-band tunneling at high body doping levels, and insufficient source-drain doping for series resistance reduction. Meeting performance targets of deeply scaled CMOS (32 nm and beyond) will require innovative solutions at every level including front end/back end integration, device architecture/circuit layout, and new channel materials. In this presentation the latter topic will be covered in some detail.

Figure 1. Innovation driven CMOS Technology



Currently, CMOS performance in both 90 and 65 nm nodes is being enhanced by straining the Si channel. Compressive strain in the pFETs channel is created byselective growth of pseudomorphic SiGe in the recessed source/drain regions surrounding the channel. Additional strain in both n and p-channels is provided by stress liners. This trend of applying higher and higher strain to CMOS channels is expected to continue for 45 nm CMOS products as well. Successful growth of selective Si:C (with > 1% substitutional C) in recessed source/drain regions of an nFET will provide an additional knob to boost the performance of 45 nm and beyond technologies.

It should be noted that the strain engineering techniques described above can not be extended indefinitely. As gate to gate pitch continues to shrink and the available real estate for strain engineering (whether via source/drain or stress liners) decreases with each successive technology generation, new non-Si materials with much higher carrier mobility may be required for CMOS channels.

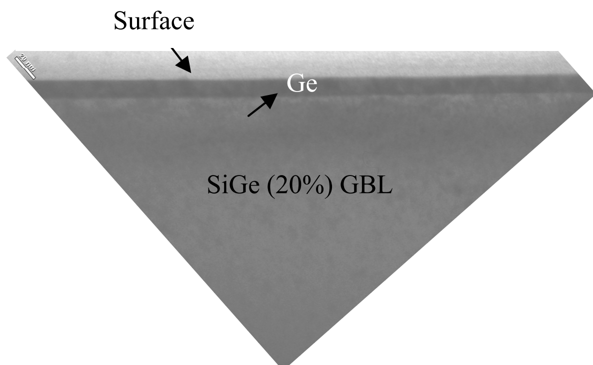
There is a consensus among the scientific community that a thorough investigation of deeply scaled Ge for pFET channel and III-Vs for nFET channel is imperative in order to scale CMOS beyond the 22 nm node. However, it is not clear how much of the known mobility enhancement in these materials will actually result in higher drive current at 22 nm and beyond nodes. Research funding for non-Si CMOS channels is on the rise from many government agencies and industrial consortiums worldwide.

Even in the best case scenario where high mobility non-Si channels do demonstrate the expected performance enhancement and are considered suitable for future CMOS, their integration into Si technology will be formidable at almost every process level. This will include material growth, unit process development (junction engineering, self-aligned contacts, gate stack etc), device design modifications, and not to mention contamination issues.

The success of any future CMOS with non-Si channels will depend on its compatibility with the contemporary Si IC infrastructure. Therefore, the wafer diameter of any non-Si solution has to match the wafer diameter of Si. This implies that epitaxial techniques that will allow high quality growth of the channel on a Si wafer will play a vital role in future.

Epitaxial growth of both Ge and III-V channels on Si poses two major challenges: (i) a large lattice mismatch (> 4%), and (ii) a non-planar growth of thin films. The residual compressive strain in a Ge film grown on Si as a function of its thickness is described by Bedell et al (this conference). It is clear from this data that critical thickness of Ge to create dislocations on Si is just a few mono layers thick. High density of defects are shown to be present in a Ge film as thin as 30A even when it is grown over a relaxed SiGe (20%) graded buffer layer (GBL) rather than Si (1). Nevertheless impressive progress has been made in the last few years in achieving planar epitaxial growth of thin Ge on Si and/or SiGe. Figure 2 show an example of such planar growth of Ge on a 300 mm Si substrate with a relaxed SiGe GBL.

Figure 2. Cross Sectional TEM of Ge grown on 300 mm SiGe graded buffer layer showing a planar growth at low temperatures



Epitaxial growth of a GaAs-containing III-V channel on a Si wafer via Ge poses additional complexity, i.e., the growth of anti phase boundaries (APD). The biggest processing challenge for both Ge and III-Vs involves their surface passivation prior to gate dielectric deposition. A practical approach to achieve the passivation on non-Si semiconductors is to create a Si-like surface, i.e., deposit a very thin layer (< 20A) of Si prior to depositing the gate

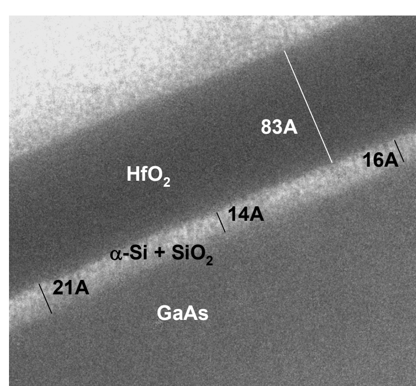


Fig 3. GaAs with α-Si/SiO_2/HfO_2 gate stack

dielectric (Fig 3). Figure 4 shows data from MOS capacitors with GaAs/α-Si/SiO_2/HfO_2 gate stacks of Fig 3. This approach allowed surface inversion in III-Vs for the first time (2). Much lower D_{it} and improved thermal stability compared to HfO_2 films directly on GaAs was obtained. Inversion was verified in the MOS capacitors using low-frequency ac capacitance measurements.

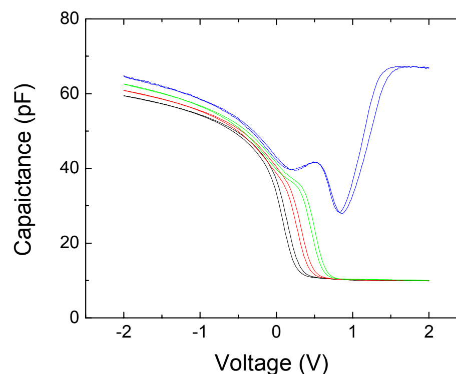


Fig 4. Demonstration of carrier inversion in GaAs with a α-Si/SiO_2/HfO_2 gate stack by C-V measurements.

Recent developments in the area of non-Si channels will be discussed in detail.

References

1. S.W. Bedell et al, ECS 2006, to be published
2. S.Koester et al, DRC Meeting, June 2006