

IBM Research Report

A 6-bit, 1.6-GSample/s CMOS Flash Converter for Multi-Gigabit Wireless Communication

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A 6-bit, 1.6-GSample/s CMOS Flash Converter For Multi-Gigabit Wireless Communication

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Abstract—A 150-mW, 6-bit, 1.6-gigasample/second (GS/s) flash converter in 0.13- μm CMOS technology is described. The analog section uses an input track-and-hold and comparator preamps with resistive output averaging for > 5.5 ENOB un-calibrated performance up to 1.6-GS/s with DC input. The digital section, designed using standard cells, contains a one to four deserializer, bubble error correction circuit, on-chip storage of thermometer data and 128 6-bit binary samples for off-chip FFT computation. A three wire serial interface is used to configure the part and read data stored on-chip. A 6-bit 16 to 1 decimated output is also provided for spectral study.

I. INTRODUCTION

The recent success of an integrated transmitter and receiver for several-hundred-megabit to multi-gigabit wireless communication in the 60-GHz ISM band[1] has fueled the demand for a digital baseband chip and accompanying ADC running at these data rates. For omni-directional links using OFDM modulation, there is a need for low-power high-sampling-rate converters to translate the analog I and Q channel outputs from a receiver into binary data. A CMOS ADC allows integration of the full digital baseband and ADC into a single chip, reducing the cost of highly-integrated millimeter-wave radios. There is also the possibility of integrating the RF front-end, ADC, and digital baseband into a single chip.

The 6-b resolution of the ADC was selected to provide ample dynamic range for broadband, multi-carrier OFDM at 2Gb/s. Resolutions of 5-b are common in UWB systems [2], and the increased 6-b resolution targeted here was a conservative choice to account for higher data rates and more OFDM sub-channels; 5-b may ultimately prove adequate for this application as well.

A 6-b, > 1 GS/s ADC is a challenging design in 0.13- μm CMOS because it pushes the speed limits of the technology while simultaneously demanding low-offset comparators. The offsets required cannot be obtained by using long-channel devices without slowing down the comparators too much. This design addresses the problem by using comparator preamps with resistor-ladder output averaging, obtaining > 5.5 ENOB performance without calibration at DC input and sampling frequency of 1.6GHz.

Beyond the circuit design challenges in analog front end, there are a variety of issues in the design of digital blocks, the most important being the latency. Fast automatic gain control implementation in digital domain requires very low latency ADC architecture. Low latency further drives the need for simple bubble error correction schemes [3] which require small combinational logic at increased risk of missing bubbles. Another selection criterion for correction scheme is to define a subset of error patterns to correct for. Error patterns in thermometer code are representation of number of bubbles and how they are dispersed at any given instance of time in thermometer code. The addition of diagnostic circuits to store thermometer code can help refine the selection of bubble error correction circuit in future designs.

Apart from design challenges, there are multitudes of test challenges involved in accurate characterization of gigasample A/D converters. For DC analysis these range from generation of low-noise DC ramps for input data to capture of multi-bit output binary code at extremely high data rates. Even in DC analysis the output code has to be captured at full output clock rate to allow the study of adjacent code jumps. None of commercially available logic analyzers can handle such high data rates. This requires design of additional test circuits to capture high speed digital data. In dynamic analysis the conventional problems of coherent versus incoherent sampling gets aggravated at these frequencies. The low frequency drift between clock and data sources causes amplitude modulation in the output digital code resulting in dispersion of fundamental component in the output spectrum.

II. CIRCUIT DESCRIPTION

A. Analog Section

A block diagram of the analog section is shown in Fig. 1. A track-and-hold circuit (T/H) is used to reduce the sampling error caused by asynchronous clock arrival at the 63 comparators. The T/H output drives 63 preamplifiers, each with a gain of approximately 3. Resistive averaging is applied at the preamplifier outputs to reduce DNL and INL due to offsets in the preamplifiers' input FETs. To allow highest speed, the regenerative comparators use minimum channel length NFETs in the input stage, which is made possible by

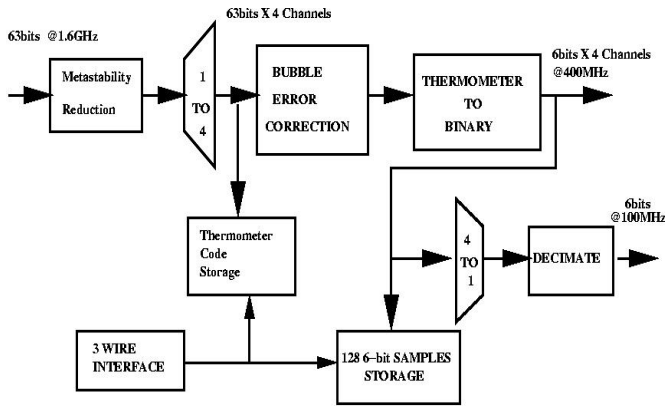


Fig. 4. Block diagram of digital section

A facility to store four blocks of thermometer code at the deserializer output was also added. To compute FFT, consecutive 128, 6-bit binary samples are also stored on chip. To reduce the size of FFT bin, the number of samples must be increased. To capture more samples, an off-chip data capture and storage facility is required. The output data rate needs to be reduced so that a multi channel logic analyzer can capture and store it. A 16:1 down sampler was added to data path to provide this feature. This limits the input frequency to Nyquist rate divided by sixteen for an alias free spectrum.

III. CHIP IMPLEMENTATION

The ADC is implemented in a 0.13- μm SiGe BiCMOS process. However, only the thin-oxide FETs, MOS capacitors, and polysilicon resistors are used in this design, so it is compatible with a variety of CMOS foundry processes. The total chip area is 2.5mm x 3mm, limited by pads. The analog section is 800 μm x 350 μm and the digital core area including the test circuit is 730 μm x 710 μm . The analog section uses 2.5V power supply for clock generator, T/H and preamp. It also uses 1.2V power supply for comparators and clock drivers. The digital core uses 1.0V and IO buffers use a 2.5V power supply.

IV. MEASUREMENTS

Initial screening tests were performed at wafer level using Cascade probe station. On verifying DC behavior, chips were wire-bonded on a printed circuit board as shown in Fig. 5.

For DC analysis the differential data input is generated by two voltage sources, which are controlled by a PC through GPIB interface. A frequency synthesizer generates a single ended clock, which is then used to generate a differential clock using a phase splitter. The three wire interface is controlled by the pattern generator/logic analyzer system to configure the ADC & read on-chip data. The decimated digital output is further divided by Xilinx ML401 development board to 10-KHz and fed into a National Digital Input Output (DIO) card. The DIO card is connected to PC through a PCMCIA interface. Labview software running on PC steps each voltage source by 0.5-mV, thus generating a 1-mVpp differential step. It then adds a wait for one second for the source outputs to settle and reads the binary code at the A/D output through

PCMCIA interface. Thus the PC stores a table of input differential voltage versus output 6-bit binary code for entire input dynamic range for a particular sampling frequency. The measurement is repeated for several sampling frequencies and wafers.

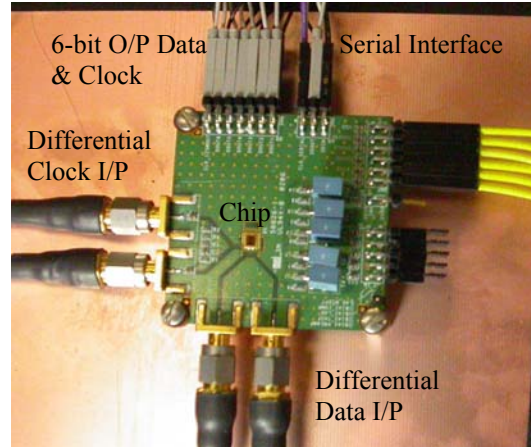


Fig. 5. ADC wire-bonded to PCB

Fig. 6 shows the differential and integral non-linearity (DNL/INL) plots for sampling frequencies ranging from 100MHz to 1.6GHz. Both INL and DNL remain below 0.5LSB. INL was computed using the best curve fit method. Beyond 1.6GHz, code jumps were observed forcing DNL/INL to increase beyond 0.5LSB.

In dynamic analysis both clock and data are generated using frequency synthesizers. The synthesizers are reference locked for coherent sampling and left independent for incoherent. The output binary code and the on-chip stored data are read by the logic analyzer through the serial interface.

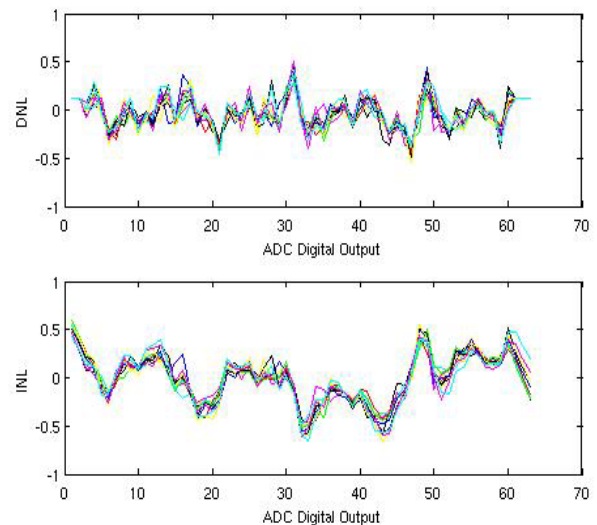


Fig. 6. DNL/INL plots for sampling freq. ranging from 100MHz (Black) to 1.6GHz (Cyan).

Fig. 7 shows quantized sine wave generated by plotting 128 on chip samples for sampling frequency of 1.28GHz and input frequency of 100MHz. This reconfirms that DNL is below 0.5LSB as no code jumps are observed.

Fig. 8 shows 128-point FFT analysis of data obtained by coherent and incoherent sampling. In both cases input frequency of 100MHz and sampling frequency of 1.28GHz is applied. The signal to noise plus distortion ratio (SNDR) for coherent sampling is 30.6dB. For incoherent sampling the SNDR is 30.4dB. This marginal difference in spectral response indicates that the clock and data sources have very low short term drift. But when decimated data is studied, allowing 180,000 samples to be taken, incoherent sampling shows dispersion of the fundamental component, resulting in drop in SNDR to 17dB. This indicates a low frequency drift in two sources. As this dispersion can mask the study of non linear behavior of converter, it was chosen to perform the rest of analysis with the two sources reference locked to each other.

For sampling frequency equal to 1.536GHz and input frequency of 12MHz, SNDR of 31.2dB was obtained implying effective number of bits (ENOB) to be equal to 4.88. The ENOB gradually degrades to 3 bits as the input frequency is raised to 700MHz. For sampling frequencies below 1.28GHz and input frequencies below 400MHz, the ENOB stays greater than 4.8 bits, with total harmonic distortion below 35dB and spurious free dynamic range above 36dB.

Fig. 9 shows the variation of SNDR with input amplitude for input frequency of 12MHz and sampling frequency of 1.536GHz. At lower input voltages the fundamental component in spectrum is comparable to noise floor resulting in poor SNDR. Input differential voltage greater than 700mV saturates the dynamic range of converter causing the fall in SNDR. On-chip grounding problems cause the noise floor to increase at frequencies beyond 1.28GHz. Also slew problems in clock drivers and nonlinearities in track and hold cause further performance degradation.

ADC power consumption at 1.6GHz sampling frequency is 150mW. The digital core excluding the test circuitry consumes 25mW. The T/H and preamps consume 75mW. The clock generators and drivers consume 50mW. The power consumption can be further improved by designing custom latches for clock dividers and deserializers in the digital section.

V. CONCLUSION

Design and measurement challenges for low power CMOS ADCs have been presented. Detailed analysis shows INL/DNL less than 0.5LSB for static inputs, while dynamic analysis shows ENOB > 4.8 for a 1.28GHz sampling frequency and input frequencies less than 400MHz. This performance level will support a 60GHz WPAN running at > 500 Mb/s, and represents a step on the way toward an integrated millimeter-wave digital baseband chip.

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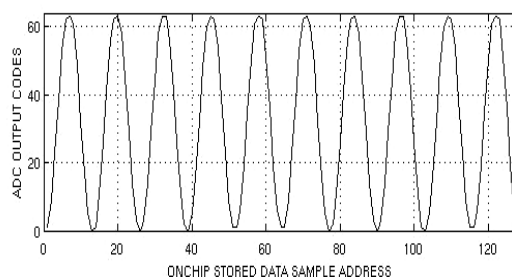


Fig. 7. Measured binary output codes for Input frequency = 100MHz, Sampling frequency = 1.28GHz

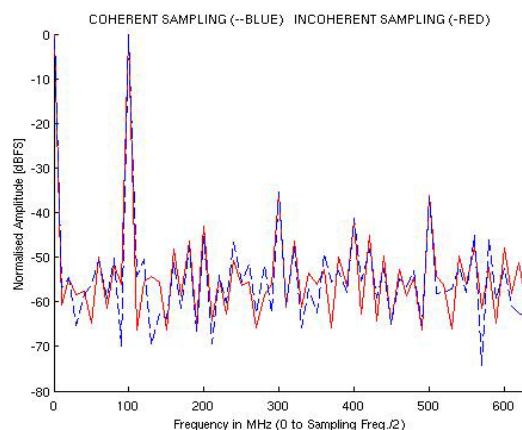


Fig. 8. 128-point FFT analysis done on data obtained by coherent (Blue) and incoherent (Red) sampling. Input Frequency = 100MHz, Sampling Frequency = 1.28GHz

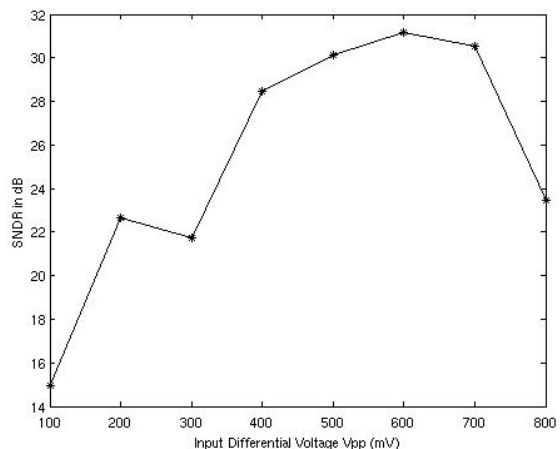


Fig. 9. Variation of SNDR with input differential amplitude for Input frequency = 12MHz, Sampling Frequency = 1.536 GHz.

REFERENCES

- [1] B. Floyd et al., "A Silicon 60-GHz Receiver and Transmitter Chipset for Broadband Communications," *ISSCC Dig. Tech. Papers*, pp. 184-185, Feb. 2006.
- [2] T. Aytur et al., "A Fully Integrated UWB PHY in 0.13um CMOS", *ISSCC Dig. Tech. Papers*, pp. 124-125, Feb. 2006.
- [3] C. W. Mangelsdorf, "A 400-MHz Input Flash Converter with Error Correction," *IEEE J. Solid-State Circuits*, vol. 25, no. 1, pp. 184-191, Feb. 1990